Thermal Issues in Next-Generation Integrated Circuits

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***Abstract*—The drive for higher performance has led to greater integration and higher clock frequency of microprocessor chips. This translates into higher heat dissipation and, therefore, effective cooling of electronic chips is becoming increasingly important for their reliable performance. In this paper, we systematically explore the limits for heat removal from a model chip in various configurations. First, the heat removal from a bare chip by pure heat conduction and convection is studied to establish the theoretical limit of heat removal from a bare die bound by an infinite medium. This is followed by an analysis of heat removal from a packaged chip by evaluating the thermal resistance due to individual packaging elements. The analysis results allow us to identify the bottlenecks in the thermal performance of current generation packages, and to motivate lowering of thermal resistance through the board-side for efficient heat removal to meet ever increasing reliability and performance requirements.**

***Index Terms*—Chip-centric cooling, chip-to-ambient thermal resistance, electronic cooling, International Technology Roadmap for Semiconductors (ITRS).**

I. Introduction

THERMAL issues are becoming increasingly important for high-end microelectronic chips whose performance is becoming increasingly limited by the maximum power that can be dissipated without exceeding the maximum junction temperature dictated by reliability guidelines. In addition, increasing level of integration, faster clock frequency, higher heat generation in interconnects, and introduction of new materials, often with poor thermal properties, add to the challenge of effective thermal management.

According to the International Technology Roadmap for Semiconductors (ITRS) projections, the number of on-chip interconnect levels is expected to rise from eight in 2002 to 11 for the 22-nm node in 2016 [1], with volumetric heat generation rates approaching $\sim 3.3 \times 10^4$ W/mm^3 within the interconnect (assuming a current density $j = 3.9 \times 10$ MA/cm^2 and a resistivity $\rho = 2.2\ \mu\Omega \cdot$ cm as specified in [1], the volumetric heat generation is given by $j^2\rho$). New low-k dielectrics are being introduced to alleviate the interconnect delay problem. These materials in general have much lower thermal conductivity than SiO_2 or Si_3N_4, which would further exacerbate the thermal problem of on-chip interconnects [2]. Table I lists the projected values for the maximum junction temperature, ambient temperature and heat dissipation (power) in the near term and long term for cost-performance and high-performance market segments, which are of main interest in this study. One can compute the required junction-to-ambient thermal resistance as the ratio of the difference between junction and ambient temperatures and the chip power. Thermal resistance values thus computed are listed in the last two rows of Table I. These resistance values represent the required overall junction to ambient thermal resistance. For a given heat dissipation rate, a lower chip-to-ambient resistance assures a lower package operating temperature and thus a longer failure free operating period from thermally driven mechanisms.

TABLE I
ITRS Near- and Long-Term Projections for the Years 2003–2016. The Desktop Personal Computers Fall in the Cost-Performance Segment and the High-End Servers and Workstations Fall in the High-Performance Segment

Year of Production	Near-term				Long-term			
	2003	2004	2005	2006	2007	2010	2013	2016
Maximum junction temperature (°C)								
Cost performance	85	85	85	85	85	85	85	85
High performance	85	85	85	85	85	85	85	85
Ambient temperature (°C)								
Cost performance	45	45	45	45	45	45	45	45
High performance	45	45	45	45	45	45	45	45
Power (W)								
Cost performance	81	85	92	98	104	120	138	158
High performance	150	160	170	180	190	218	251	288
Required thermal resistance (°C/W)								
Cost performance	0.49	0.47	0.43	0.41	0.38	0.33	0.29	0.25
High performance	0.27	0.25	0.24	0.22	0.21	0.18	0.16	0.14

The maximum operating temperature has implications both on the chip and package level reliability and performance. At the chip level, the nonuniformity in temperature leads to a clock skew [3]. Also, higher interconnect temperatures accompanied with high current densities lead to enhanced electro-migration. At the package level, higher absolute temperatures accelerate thermally driven failure mechanisms including intermetallic growth, corrosion, metal migration and void formation [4]. Higher operating temperatures can also lead to greater cumulative fatigue per cycle for certain materials like solder. ITRS therefore suggests that junction temperature will be maintained constant at 85 °C for future technology nodes (Table I).

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In the present study, the limits of heat removal from a bare chip are first computed in two hypothetical configurations. In the first, the chip is embedded in an infinite solid medium and heat is dissipated by conduction only. In the second, the chip is fully immersed in unbounded liquid, leading to convective heat dissipation. The packaging constraints imposed on heat flow from chip to ultimate ambient are analyzed next by considering a typical microprocessor package. The thermal resistances of interface materials, air-cooled heat sink, substrate and printed wiring boards (PWBs) are briefly reviewed and are estimated with appropriate boundary conditions. The analysis reveals that with the present day approach to electronic cooling, in which only one side of the chip is used for heat rejection, it would be very challenging to effectively reject the power dissipated at the level projected by the ITRS roadmap. The low heat resistance path between the chip and board via chip-to-board global interconnects may hold the key to meet the cooling requirements in the future generation processors. Using this example, the need for chip-centric cooling solutions is motivated.

II. Bare Chip Heat Removal Limits

This section discusses the case of heat removal from a bare chip with pure conduction and pure convection boundary conditions.

A. Chip Embedded in an Infinite Solid Medium: Pure Conduction Limit

Fig. 1 shows a configuration in which a chip is embedded in an infinite solid medium. A uniform volumetric heat generation is assumed inside the chip. This problem was solved using a finite-element solver (ANSYS) with the outer dimension of the bounding medium taken sufficiently large so that the computed value of thermal resistance was due to conduction only. The outer surface of the solid medium was assigned ambient temperature. The thermal interface between the chip and the medium was assumed perfect (free of any interfacial thermal resistance). The physical quantity of interest is the thermal resistance, defined as the ratio of the difference in chip surface and ambient temperatures to total heat generation rate in the chip. The thermal resistance value thus obtained is plotted in Fig. 2, as a function of the ratio of thermal conductivity of the medium to that of the chip. As expected, the value of thermal resistance decreases with an increase in the thermal conductivity of the surrounding medium. This result further motivates the ongoing investigations of high thermal conductivity composites for thermal management [5].

B. Chip Immersed in Fluid: Pure Convection Limit

Fig. 3 shows a chip completely immersed in a fluid. The physical quantity of interest again is the thermal resistance between the chip surface and ambient. For this case, temperature at the chip surface can be computed using analytical techniques [6], considering the chip as a cuboid with uniform heat generation subjected to convective boundary condition on all faces. The analytical solution is listed in Appendix A. The computed value of thermal resistance is plotted in Fig. 4, as a function of heat transfer coefficient applied at the chip surface. Typical heat

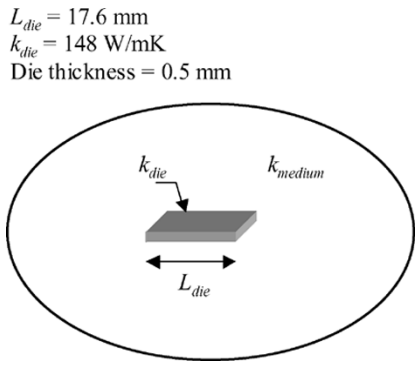

Fig. 1. A chip embedded in an infinite solid medium. A uniform volumetric heat generation is assumed inside the chip whereas a constant-temperature boundary condition is applied at the outer boundary.

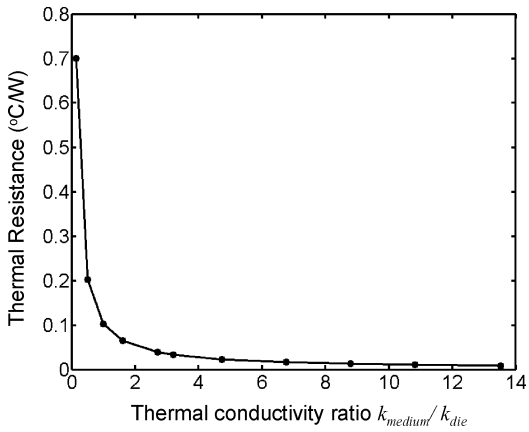

Fig. 2. Plot of conduction thermal resistance as a function of the thermal conductivity ratio.

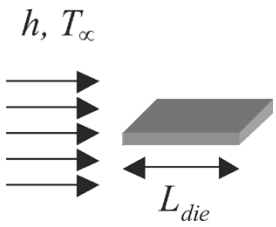

Fig. 3. A chip immersed in liquid. A uniform volumetric heat generation is assumed inside the chip.

transfer coefficients for various regimes are given in [7]. Total thermal resistance, which is the sum of the conductive resistance (inside the chip) and the convective resistance (at the chip surface) decreases with an increase in convective heat transfer coefficient at the surface of the chip. Physically, the value of heat transfer coefficient is related to the thermophysical properties of the external fluid and corresponding flow regimes. The possible ranges of heat transfer coefficient and the corresponding requirement on the external flow field are indicated in Fig. 4. Forced and natural convection of liquids provide higher values of convective heat transfer coefficient than that of gases, respectively. Phase change (boiling) provides the highest values of heat transfer coefficient. It is important to note that this analysis corresponds to a bare chip and does not include any enhancement in the heat transfer, which may be achieved with a heat sink or surface area enhancements.

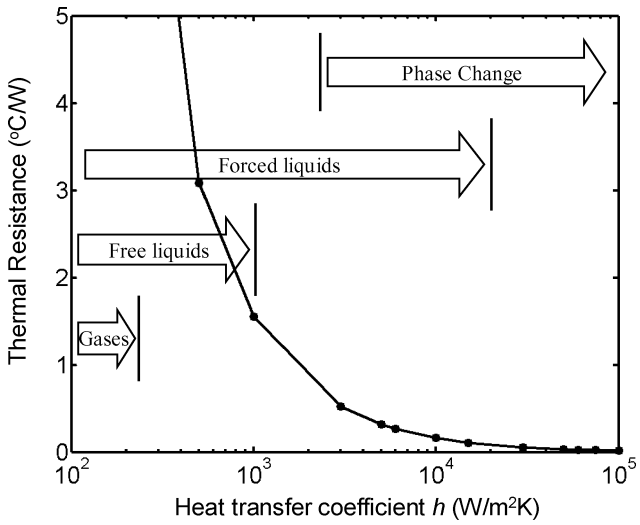

Fig. 4. Plot of total thermal resistance with an increase in convective heat transfer coefficient.

The above analysis shows that it is physically possible to remove heat corresponding to even the most severe projected requirements (0.14 °C/W for high-performance chips at the end of 2016) if all the sides were available for heat rejection to ambient. However, a microelectronic chip must be connected to the outside world in order for it to be useful and it must also be protected from the environment in order for it to operate reliably. These are the two additional requirements, which an electronic package must fulfill, apart from providing a means for effective cooling. Any thermal management solution and its performance are constrained by these additional requirements on the package. These constraints can be understood by considering the thermal resistance across individual package elements. This is accomplished in the next section by considering a typical current day microprocessor package.

III. Chip With Packaging Components

Fig. 5 shows schematic of a typical current day microprocessor package with the chip attached to the package in flip-chip configuration. The active side of the chip is attached to the substrate which in turn is attached to the printed circuit board (PCB) using substrate to board interconnects. A spreader plate is attached to the backside of the chip on which a heat sink is mounted. The thermal resistances due to the package elements at the top (backside) and bottom (active side) are effectively connected in parallel between the chip and the ambient. In this section individual packaging elements are considered and thermal resistance across them is computed with appropriate boundary conditions.

A. Spreader Plate

Fig. 6 shows the schematic of a copper spreader plate attached to a chip. The top surface of the spreader plate is assigned a heat transfer coefficient between 1000–5000 $\mathrm{W/m^2 \cdot K}$. The assigned value of heat transfer coefficient, which determines the thermal resistance between the top surface of the spreader plate and the ambient can be realized either with forced liquid or with

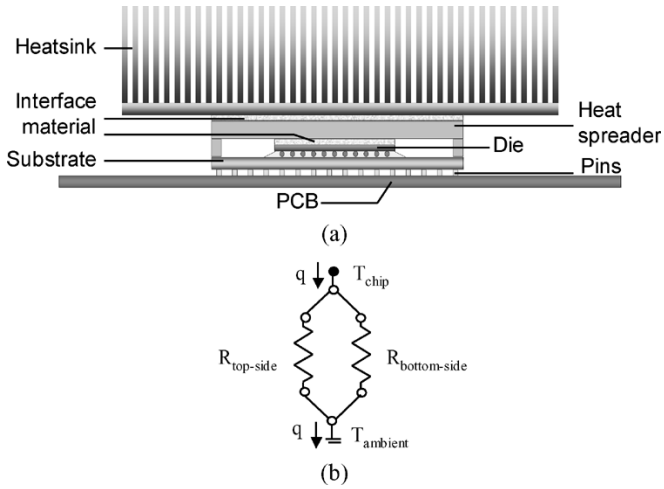

Fig. 5. (a) A typical electronic package. At the top we have spreader plate, thermal interface material, and heat sink, and at the bottom we have solder balls, substrate, and printed wiring board. (b) The thermal resistance due to package elements at top and bottom of the chip are effectively in parallel between the chip and the ambient.

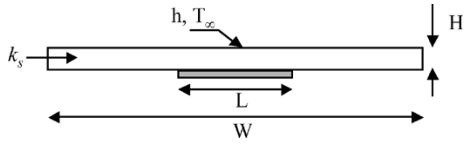

Fig. 6. Copper spreader plate attached to the chip. A constant heat transfer coefficient is assumed on the top face of the spreader plate and the other faces are assumed adiabatic. A uniform volumetric heating is assumed in the chip.

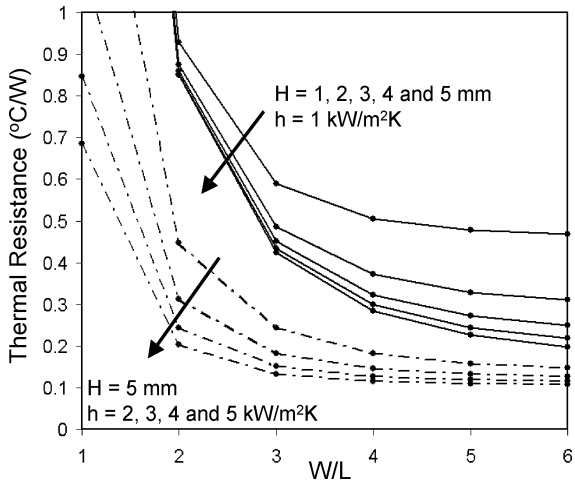

Fig. 7. Thermal resistance due to a copper spreader plate attached to a chip. The resistance includes both the spreading resistance and the one-dimensional conduction resistance as a function of the ratio of spreader plate to chip dimensions.

liquid/vapor phase change (see Fig. 4). Alternatively, it can be realized indirectly by attaching a heat sink with an equivalent thermal resistance. The thermal resistance computed using the analytical solution [8] for this configuration is plotted in Fig. 7, as a function of ratio of width of the chip to that of the spreader plate, with the spreader plate thickness and the heat transfer coefficient as parameters. The thermal resistance asymptotically approaches a lower limit, depending on the thickness of the spreader plate and the convection coefficient specified at the top.

TABLE II
TYPICAL THERMAL RESISTANCE OF THERMAL INTERFACE MATERIALS

Interface Material	Thermal resistance ($cm^2 - {}^oC/W$)	Thermal resistance* (${}^oC/W$)	Pressure (kPa)
Chomerics T454 (PCM)	0.258	0.083	340
Eutectic Attach	0.04 – 0.17	0.013 – 0.055	---
Arctic Silver (Thermal Grease)	0.018	0.006	82

*For an area of 310 mm^2

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Increasing the convection heat transfer coefficient leads to a decrease in the thermal resistance, as expected. For lower convection coefficients, an increase in the spreader thickness reduces the thermal resistance, which implies that there may exist an optimal thickness. This analysis ignored any interfacial thermal resistance between the spreader plate and the die, which is inevitable in a real package.

B. Thermal Interface

The microscopic asperities and nonplanarity of the surfaces prevent the two from forming a perfect thermal contact at the mating plane. Thermal interface materials are therefore used to provide a reliable heat conduction path between two solid surfaces. The three main types of thermal interface materials are thermal pad, thermal grease and phase change materials (PCM's). These were reviewed by Vishwanath *et al.* [9]. PCMs conform to surfaces better and have superior wetting characteristics. They were less prone to pump-out than thermal greases. The study by Vishwanath *et al.* concluded that PCM's are most suitable for application in cost performance segment of microprocessors. Intel's P4 microprocessor package is reported to use Chomerics T 454 (with a thickness of 0.125 mm), which is a phase change material and remains in liquid form under the steady-state chip operating conditions [10]. Table II lists some representative interface materials and corresponding thermal resistances associated with them [9], [11]. It has been recently suggested that adding highly conductive nanoparticles or nanotubes may result in novel high-performance interfacing techniques [12].

C. Heat Sink

The heat sink rejects heat to the ambient air inside the cabinet of the computer. It can be attached either to a spreader plate (as in the case of an Intel Pentium 4) or directly to the chip. Reducing the thermal resistance of heat sinks has been one of the primary objectives of recent and past thermal management research. Numerous studies were performed on design and optimization of forced air-cooled heat sinks [13], [14]. It appears that the typical heat sink resistance values of 0.36 °C/W in the desktop (cost performance) segment and 0.27 °C/W in the servers and workstations (high performance) segment, as reported in [9] may be well near the limit of practical air-cooled heat sink technology for microprocessor cooling.

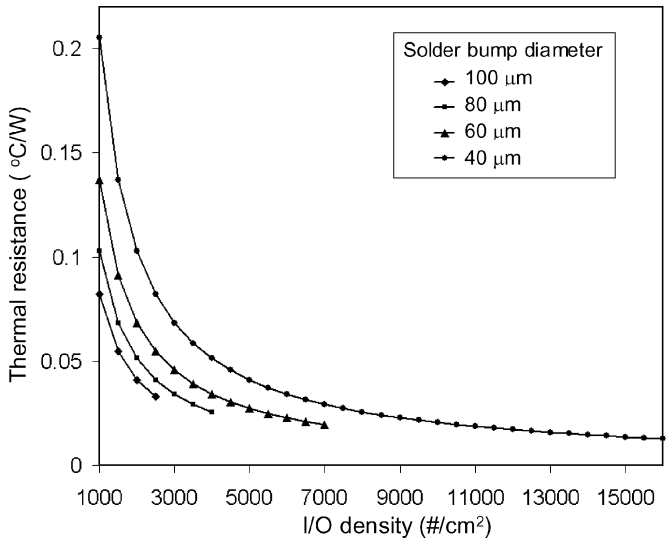

Fig. 8. Thermal resistance between the chip and the substrate with increasing number of I/Os (assuming a cylindrical shape for solder bump of same height and diameter and a thermal conductivity of 50 W/mK).

D. Chip-to-Package Interconnects

In the flip-chip packages, the electrical I/O (input/output) connection is realized with solder balls. From the thermal perspective, the solder balls form a configuration of parallel heat conduction paths between the chip and the substrate. Adding an extra solder ball is equivalent to adding a thermal path in parallel to the existing ones and thus leads to a reduction in the thermal resistance. In Fig. 8, the total thermal resistance due to solder bumps is shown for a 310-mm^2 die as their density increases for different bump sizes. The curves end at a number density that is equivalent to a pitch of twice the bump diameter. As the density of the solder balls increases, the thermal resistance decreases.

E. Substrate Architecture

Microprocessors substrates have evolved considerably and their architectures affect chip performance considerably. Organic substrates have become the choice for current Pentium series microprocessors [15]. A polymer-matrix laminate peripheral Ball Grid Array (BGA) package in the cavity down configuration (Super BGA) was analyzed by Guenin *et al.* [16] and a thermal resistance of 1.9 °C/W was reported. Parry *et al.* [17] developed compact models for Motorola's PowerPC processors in a 21×21 mm^2 Ceramic Ball Grid Array (CBGA) package. Based on the effective properties used for the ceramic substrate layer and solder balls the respective resistances were computed to be 0.12 and 0.14 °C/W. In some cases, the package may be attached to the motherboard through a socket, which may lead to additional resistance.

F. PWB

PWBs consist of multiple layers of copper circuitry sandwiched between layers of glass epoxy composites. Thermal conductivity of copper is about 700 times that of the glass epoxy composite and this difference imparts high anisotropy ($k_{||}/k_{\perp}$) to the thermal conductivity of the board. Azar and

Graebner [18] report the values of $k_\perp$ (cross-plane thermal conductivity) and $k_\parallel$ (in-plane thermal conductivity) for different samples of PWB's from direct measurements. For the samples studied, the value of $k_\perp$ is reported to be between 0.32–0.36 W/mK, whereas the value of $k_\parallel$ lies between 8 and 36 W/mK. The higher values of in-plane conductivity correspond to the samples with greater total thickness of continuous copper layers. The thermal resistance for a 1.5-mm-thick PWB with $k_\parallel$ of 20 W/mK and $k_\perp$ of 0.5 W/mK is about 6.45 °C/W. This resistance includes the spreading component from the square heat source[1] and one dimensional conduction through the board. It is the highest thermal resistance in the heat flow path from the active side of the chip to the ambient through the PWB. From the PWB to ambient the heat may be rejected by convection and radiation. The amount of heat rejection would depend on the specifications on the board population and system level flow field.

IV. Summary and Conclusion

Analysis of a bare heat-generating chip subjected to pure conduction and convection cooling boundary conditions is presented. In a typical package, the two possible parallel heat-flow paths between the junction and the ambient are through the top (heatsink) and bottom side (substrate to board) of the chip. In the current day microprocessor the heat sink attached to the backside of the chip rejects major fraction of heat generated inside the chip. A very small fraction of the heat flows through the active side to substrate to PWB to the ambient. Thermal management research in the past has focused mainly on reducing the resistance through the backside of chip, by lowering the thermal resistance of heat sink which is currently near its practical limits. Further improvements require effective utilization of the board-side heat removal pathway. This entails effective channeling of heat from the chip to the board and its efficient rejection to the ultimate ambient.

In the present day architectures, the required number of electrical I/Os decides the number of solder balls. By using additional solder balls (thermal interconnects) a lower thermal resistance path can be realized between the chip and board/substrate. Heat can then be removed from the board efficiently through several possible means, including heat spreaders and board-integrated liquid cooling. Effective utilization of chip/substrate/board as a significant heat flow path can potentially lead to a reduction in package attached heat sink size, or its total elimination. Such cooling solution designs call for concurrent electrical and thermal design of the chip/substrate/board architecture.

Appendix A
Uniformly Heat-Generating Cuboid in a Convective Medium

Consider a cuboid of side $2a, 2b, 2c$ along x, y, z respectively with convection heat transfer coefficients h_x, h_y, h_z on faces perpendicular to x, y, z axes, respectively. Using standard techniques of separation of variables [6] we can obtain an expression for temperature distribution in the solid. Due to symmetry, the analytical solution for temperature $T(x, y, z)$ in an octant in the positive xyz space is given as

$$T(x,y,z) = T_\infty + \frac{\dot{q}'''a}{h_x} + \frac{\dot{q}'''}{2k}\left(a^2 - x^2\right) + Y(x,y,z) + Z(x,y,z)$$

where

$$Y(x,y,z) = -\sum_{m,n}^{\infty} \frac{\dot{q}''' h_y \sin(\alpha_{ym}a)\sin(\beta_{yn}c)}{k\alpha_{ym}^3 \beta_{yn} N(\alpha_{ym}) N(\beta_{yn})} \cdot \frac{\cos(\alpha_{ym}x)\cos(\beta_{yn}z)\cosh(\gamma_{ymn}y)}{[h_y \cosh(\gamma_{ymn}b) + k\gamma_{ymn}\sinh(\gamma_{ymn}b)]}$$

$$N(\alpha_{ym}) = \frac{a\left(h_x^2 + (k\alpha_{ym})^2\right) + h_x k}{2\left(h_x^2 + (k\alpha_{ym})^2\right)}$$

$$N(\beta_{yn}) = \frac{c\left(h_z^2 + (k\beta_{yn})^2\right) + h_z k}{2\left(h_z^2 + (k\beta_{yn})^2\right)}$$

$$Z(x,y,z) = -\sum_{m,n}^{\infty} \frac{\dot{q}''' h_z \sin(\alpha_{zm}a)\sin(\beta_{zn}b)}{k\alpha_{zm}^3 \beta_{zn} N(\alpha_{zm}) N(\beta_{zn})} \cdot \frac{\cos(\alpha_{zm}x)\cos(\beta_{zn}y)\cosh(\gamma_{zmn}z)}{[h_z \cosh(\gamma_{zmn}c) + k\gamma_{zmn}\sinh(\gamma_{zmn}c)]}$$

$$N(\alpha_{zm}) = \frac{a\left(h_x^2 + (k\alpha_{zm})^2\right) + h_x k}{2\left(h_x^2 + (k\alpha_{zm})^2\right)}$$

$$N(\beta_{zn}) = \frac{b\left(h_y^2 + (k\beta_{zn})^2\right) + h_y k}{2\left(h_y^2 + (k\beta_{zn})^2\right)}$$

$$\gamma_{ymn} = \sqrt{\alpha_{ym}^2 + \beta_{yn}^2}; \gamma_{zmn} = \sqrt{\alpha_{zm}^2 + \beta_{zn}^2}.$$

In the above expressions, k is the thermal conductivity, $\dot{q}'''$ is the volumetric heat generation rate, and T_∞ is the ambient temperature. The eigenvalues $\alpha_{ym}, \beta_{yn}, \alpha_{zm}$ and β_{zn} are the solutions of the following transcendental equations and take on an infinite number of values enumerated by indexes m and n

$$\alpha_{ym}\tan(\alpha_{ym}a) = \frac{h_x}{k}$$

$$\beta_{yn}\tan(\beta_{yn}c) = \frac{h_z}{k}$$

$$\alpha_{zm}\tan(\alpha_{zm}a) = \frac{h_x}{k}$$

$$\beta_{zn}\tan(\beta_{zn}b) = \frac{h_y}{k}.$$

Appendix B
Thermal Resistance of Isoflux Rectangle on a Substrate

Consider a rectangular isoflux heat source of dimensions $2a$ and $2b$ along x and y axes, respectively, on a substrate of dimensions $2c$ and $2d$ along x and y axes respectively. For a convec-

[1]Square PWB with heat flux source over a (17.6×17.6) mm^2 area and PWB length six times the source size. Bottom face maintained at constant temperature and all other sides insulated.

tion heat transfer coefficient h on the bottom and all other faces insulated, the thermal resistance is given by [8]

$$R_s = \frac{1}{2a^2cdk}\sum_{m=1}^{\infty}\frac{\sin^2(a\delta_m)}{\delta_m^3}\cdot\phi(\delta_m) + \frac{1}{2b^2cdk}\sum_{n=1}^{\infty}\frac{\sin^2(b\lambda_n)}{\lambda_n^3}\cdot\phi(\lambda_n) + \frac{1}{a^2b^2cdk}\sum_{m=1}^{\infty}\sum_{n=1}^{\infty}\frac{\sin^2(a\delta_m)\sin^2(b\lambda_n)}{\delta_m^2\lambda_n^2\beta_{m,n}}\cdot\phi(\beta_{m,n})$$

$$\delta_m = \frac{m\pi}{c};\lambda_n = \frac{n\pi}{d};\beta_{m,n} = \sqrt{\delta_m^2+\lambda_n^2};$$

$$\phi(\varsigma) = \frac{\left(e^{2\varsigma t}+1\right)\varsigma - \left(1-e^{2\varsigma t}\right)\left(\frac{h}{k}\right)}{\left(e^{2\varsigma t}-1\right)\varsigma + \left(1+e^{2\varsigma t}\right)\left(\frac{h}{k}\right)}.$$

In the above expression k is the thermal conductivity and t is the thickness of the substrate. The eigenvalues δ_m and λ_n take an infinite number of values.

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