HARDWARE DEVELOPMENT OF M4088 DIGITAL CAMERA SYSTEM CONTROL

1. Objective

Present lab session's objective is the design of the control hardware for the digital camera used as input image sensor in the proposed application.

2. Introduction

M4088 is a monochrome digital camera that supplies the grabbed images in digital form. The heart of the camera is the Omnivision CMOS sensor OV5017 that combines CMOS technology with a suitable digital interface. Its high grabbing speed of 50 images/s makes M4088 a good low cost solution for high quality applications.

Digital video port supplies, in a continuous form, 1 byte data format of image pixels. Sensor device can be configured to adapt to external image conditions. Exposure time, bright compensation and gamma value are some of the available options. Camera configuration input and image information output are register based, making both operations as simple as write to and read from a single memory address, as will later be shown.

Camera outstanding characteristics are: small size of only 35 x 29 mm, different lens options, digital output with 8 bits per píxel, pixel dimension of 11 x 11 μm, analog output (75Ω) and continuous image capture. Its power consumption is less than 100mW with a single supply voltage of 5V±0.5 (DC). Signal to noise ratio is better than 42dB. Other capture and processing options are available which will be introduced later.

Aside from digital output, the device has three sync signals to identify the start of a new image, new line or new pixel. The correct use of these sync signals allows a coherent image capture that will follow from a correct synchronization between camera and processing system.

Figure 1 shows outlines and aspect of M4088 camera.

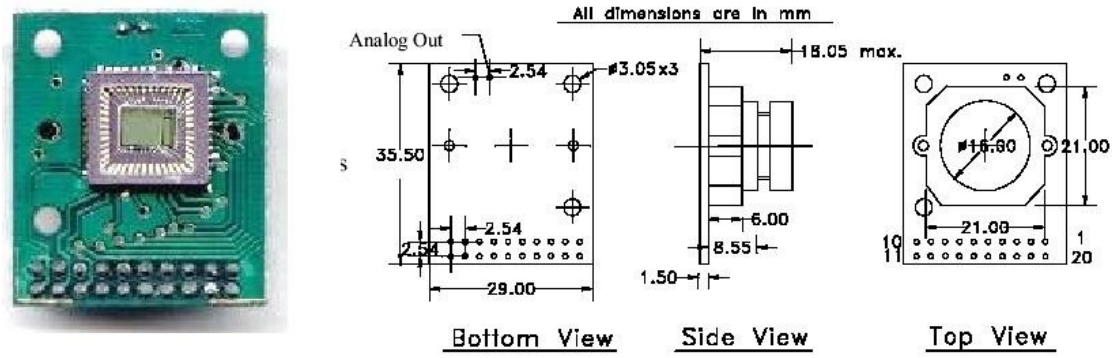

Figure 1. Physical outlines of M4088 camera.

Camera pin-out is listed in the following table:

Pin	Signal	Description
1-8	D0-D7	Bidirectional Data Bus
9	VCC	Supply Voltage
10	GND	Ground
11-14	A3-A0	Register Address Bus
15	OEB	Data Bus Output Enable
16	WEB	Data Bus Write Enable
17	CSB	System Chip Select
18	HREF	Start of Line Sync Signal
19	PCLK	New Pixel Sync Signal
20	Vsync	Start of Image Sync Signal

As has previously been said, both pixel read and parameter write are register based, under control of A3-A0 and D0-D7 camera busses.

Pixel Output Register outputs a new pixel on D0-D7 immediately after it is available. Accordingly, the system reading this information has to do it at a speed that is at least equal to that of pixel supply by the camera, unless we want to loose some and then capture a wrong image. Therefore, it is important to know the value of that minimum speed. Considering the maximum capture speed of 50 images/s and that they contain 384 x 288 píxels each, we have:

T(1 píxel)= 1 / (50 fps * 384 * 288) = 180.85 ns.

This value leads to a minimum frequency of 5.5 MHz. Although not very high, this value clearly states the need of a dedicated hardware system to cope with image capture successfully.

Next Table lists the M4088 register address.

A[3:0]	Register	R/W	Description	Default Value
10XX	VPORT	R	Pixel Data	xxxxxxxx
0000	STATUS	R	Status Register	00xxxxxx
0001	FCTL	W	System Control	00xx0000
0010	EXCTL	R/W	Manual/Auto Exposure	11111111
0011	GCTL	R/W	Gain	xxxxx000
0100	FRCTL	R/W	Image Capture Speed	00000000
0101	MCTL	R/W	Miscellaneous Controls	00000000
0110	HWCTL	R/W	Image width Control	00000000
0111	VWCTL	R/W	Image height Control	00000000

Some of the camera options that can be programmed through these registers are the following:

- Internal colour calibration.
- Stand-by.
- Software reset.
- Exposure time setting (from 1/50s to 1/12800s).
- Gain value after image capture (from 0dB to 18dB).
- Image capture frequency setting.
- Gamma value (0.45 or 1).
- Mirror image (i.e., to read text).
- Indoor or outdoor light selection.
- Bright compensation after image capture.
- Image size.

To read from or write to the registers, standard memory access by means of DATA[7:0], A[3:0], WEB, OEB and CSB signals is used. As shown in figures 2 and 3, read cycle can be Chip Select (CSB) controlled or address (A[3:0]) controlled. Write cycle can in turn be Chip Select (CSB) controlled or Write Enable (WEB) controlled. It is important to outline that register access is totally asynchronous with pixel timing.

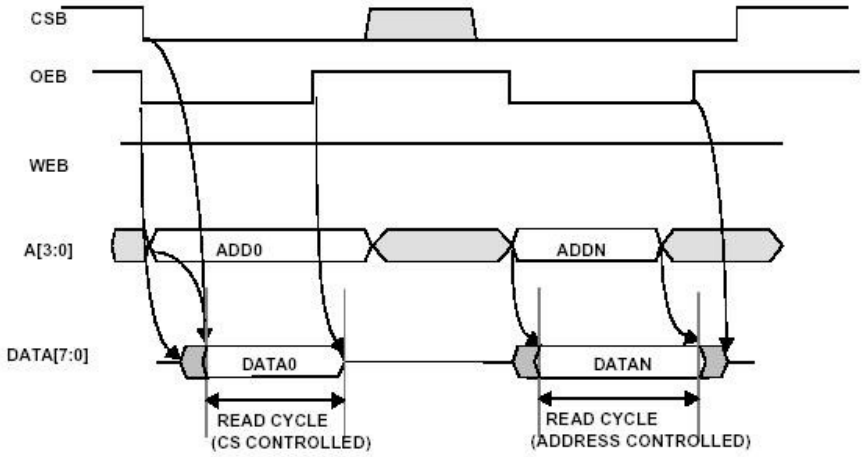

Figure 2. Register Read Timing for M4088.

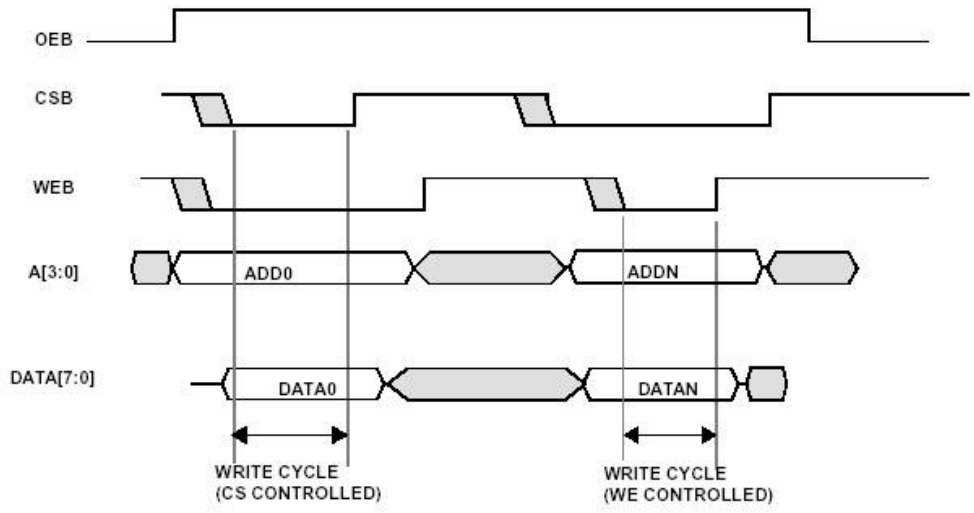

Figure 3. Register Write Timing for M4088.

Pixel read on the M4088 data bus is not much different. However, we have to use the sync signals (PCLK, HREF, Vsync) offered by the camera to synchronize pixel, line and image capture. Figure 4 shows how to use these sync signals.

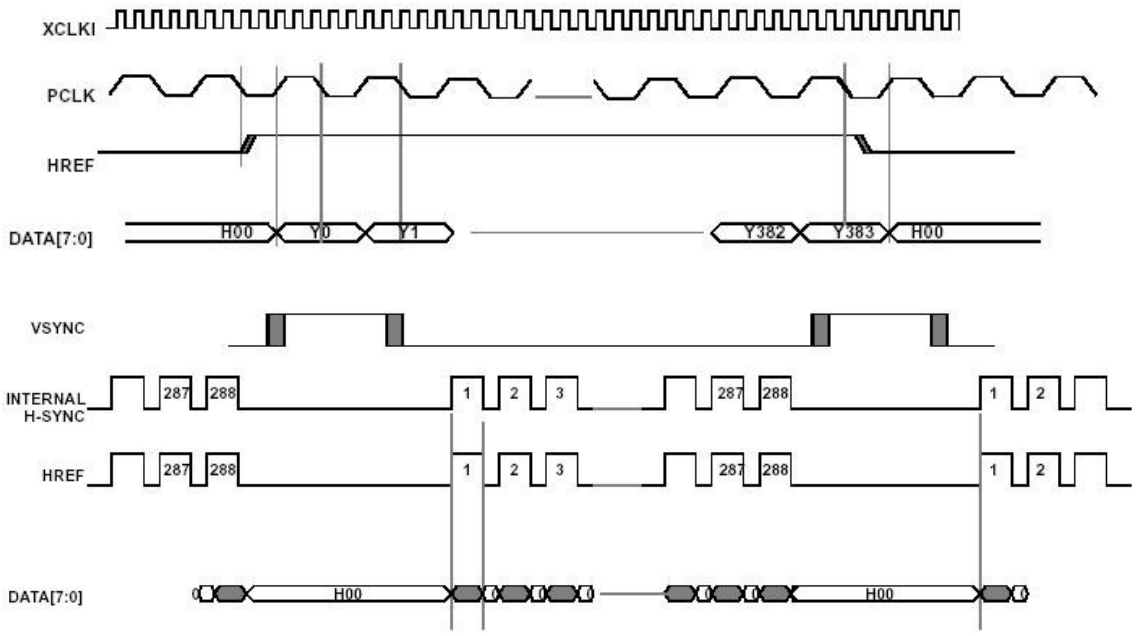

Figure 4. Pixel capture sync signals.

As can be seen from figure 4, if register VPORT is selected (A[3:0] = 10XX), a new pixel will appear on data bus at every raising edge of signal PCLK. Also, manufacturer guarantees that pixel value will be stable at the falling edge of PCLK. Thus, by means of this PCLK signal we can correctly synchronize pixel acquisition. Pixel synchronization, however, is not enough. Line and frame have also to be synchronized through signals HREF and Vsync.

As indicated in figure 4, when signal HREF is high pixel data are valid and belong to the same image line. When HREF goes low, the bus has a constant value of 0x00 indicating that no valid pixel is present in the bus. Therefore, aside from indicating a line start or end, HREF also signals if the pixel in the data bus is valid.

On the other side, Vsync is valid low, a transition from 0 to 1 indicating the end of an image. A transition from 1 to 0 marks the start of a new image on the M4088 data bus.

3. Development specification.

Control system to be designed will be described within an entity named ***control_camera***, which in turn is called from a higher hierarchy design. This control system will have to manage all the signals available at the camera input/output interface. Inputs to this system will be the address of register to be configured and the value to write into it. Moreover, two more input signals named ***configure*** and ***capture*** will indicate if a parameter is to be configured or image capture is enabled.

Of the control signals our system has to produce to control the camera, the Write Enable signal ***WEB*** has to have a duration of 5 clock periods. The Output Enable signal ***OEB*** can remain valid all the time during an image capture. However, during the configuration phase this signal has to remain false during one clock period after the ***WEB*** goes false to guarantee data stability.

Summarizing, the system to be designed will have 9 inputs named ***clk***, ***clearn***, ***Vsync***, ***HREF***, ***PCLK***, ***cam_reg(3 downto 0)***, ***instruction(7 downto 0)***, ***configure*** and ***capture***, and also 8 outputs named ***CSB***, ***OEB***, ***WEB***, ***address(3 downto 0)***, ***pixel(7 downto 0)***, ***new_pixel***, ***new_line*** and ***new_image***. Apart from that, it will have a bidirectional input/output port named ***data(7 downto 0)*** that has to be connected to the camera data bus. The meaning of these signals is as follows:

- **clk:** System clock signal with a frequency of 50 MHz and active at its rising edge.
- **clearn:** System synchronous reset signal, valid low.
- **Vsync:** Camera image sync signal. It is valid low, a transition from 0 to 1 indicating the end of an image whereas a transition from 1 to 0 marks the start of a new image on the M4088 data bus.
- **HREF:** Camera line sync signal. When this signal is high pixel data are valid and belong to the same image line. When HREF goes low, the bus has a constant value of "00000000".
- **PCLK:** Camera pixel sync signal. A new pixel will appear on data bus at every raising edge of signal PCLK and its value will be stable at the falling edge.
- **cam_reg(3 downto 0):** This input holds the address of the camera register to be configured.
- **instruction(7 downto 0):** This input will contain the value to be written in the camera register pointed by input ***registre***.
- **configure:** When this signal is low, a camera configuration process is underway. Due to the long signal duration compared to system clock period, we'll need to detect its falling edge to make sure that only one configuration process is realized every time that this signal goes active.
- **capture:** When this signal is high, image capture is enabled. In that case, the signal ***OEB*** will be active and the signal ***WEB*** inactive. Moreover, output signal ***address(3 downto 0)*** will hold the value "1000". On the other side, when image capture is disabled, signals ***OEB*** and ***WEB*** will be inactive and output signal ***address(3 downto 0)*** will hold the value "0000
- **data(7 downto 0):** Camera bidirectional data bus.
- **CSB:** Camera enable signal active low. This signal can be permanently active if wished.
- **OEB:** Camera output enable signal active low. When at '0' camera will be able to output data on its bus. Otherwise, camera bus will be in high impedance state.
- **WEB:** Camera write enable signal. When low, camera registers may be written into.
- **address(3 downto 0):** Camera address bus.
- **pixel(7 downto 0):** This 8 bit bus will hold the last pixel value supplied by the camera.

- **new_pixel:** This signal marks the occurrence of a new valid pixel. It has to go '1' with the falling edge of ***PCLK*** and go back to '0' with the rising edge of ***PCLK***.
- **new_line:** This signal indicates that the camera is providing pixel data of a new line. It has to go '1' with the rising edge of ***HREF*** and go back to '0' with the falling edge of ***HREF***.
- **new_image:** This signal indicates that the camera is providing pixel data of a new image. It has to go '1' with the falling edge of ***Vsync*** and go back to '0' with the raising edge of ***Vsync***.

The design under way has to be a component of an entity named ***test_camera***. This entity instantiates the entity of our design as well as another entity named ***sim_camera***, containing a functional model of the camera used in this application. At the same time, entity ***test_camera*** is in charge of the definition of input/output interface allowing our design to be verified onto the available prototype board.

The 8 switches on the prototype board will be used to input the commands to be executed by control system. ***SW1*** (the rightmost on the board) corresponds to signal ***capture***, while ***SW2*** corresponds to ***configure***. ***SW8*** to ***SW3*** will input the command to be executed, as done in sessions P2 and P3. Switch state will also be indicated by the LED's above them ('1' lit, '0' off).

Entity ***test_camera*** will translate the corresponding ***SW8*** to ***SW3*** command into the right values of ***cam_reg*** and ***instruction*** inputs to control system. This same entity will also average the pixel values provided by the camera model to easy the display of system final results for evaluation. In particular, this entity will average the value of every first pixel over 256 lines.

The four 7 segment displays on the board will show the design results as follows: The two leftmost digits will show, at 1s intervals and in hex format, the contents of the three camera registers implied (MCTL, EXCTL and GCTL), while the two rightmost digits will show, at 1s intervals and in hex format, the averaged pixel values. If design is OK, the sequence of values after reset begins by: **0x79, 0xF3, 0x6C, 0x1D, 0x97, 0x10, ...**