Chapter 3

Parallel Comunication

SYSTEM = ELEMENTS + INTERCONNECTS

BUS = SET OF INTERCONNECT LINES

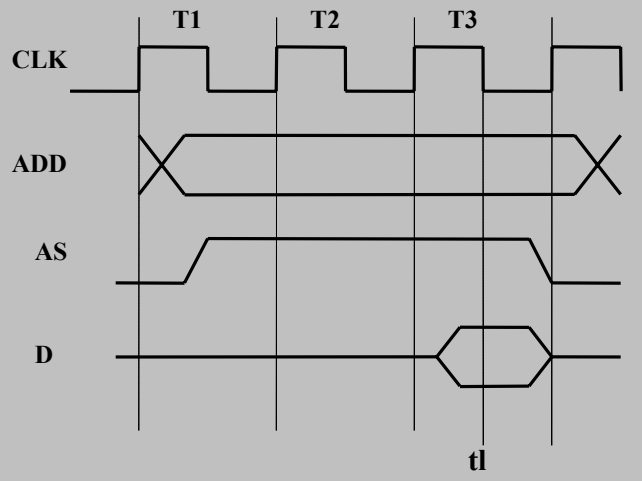
To SYSTEMATIZE, this set of lines or BUS is made HOMOGENEOUS. Accordingly, we are lead to different CLASIFICATIONS in relation to the ASPECTS CONSIDERED.

BUS CLASSIFICATION

- ✓ **CONNECTIVITY**
  1. One Transmitter & Many Receivers (1TXR)
  2. Many Transmitters & One Receiver (XT1R)
  3. Many Transmitters & One Receiver (XTXR)
- ✓ **FUNCTIONALITY**
  1. DATA Bus
  2. ADDRESS Bus
  3. CONTROL Bus
- ✓ **SYNCRONIZATION**
  1. SYNCRONOUS Bus
  2. SEMISYNCRONOUS Bus
  3. ASYNCRONOUS Bus
- ✓ **TOPOLOGY**
  1. STAR Bus
  2. DAISY-CHAIN Bus
  3. SHARED LINE Bus

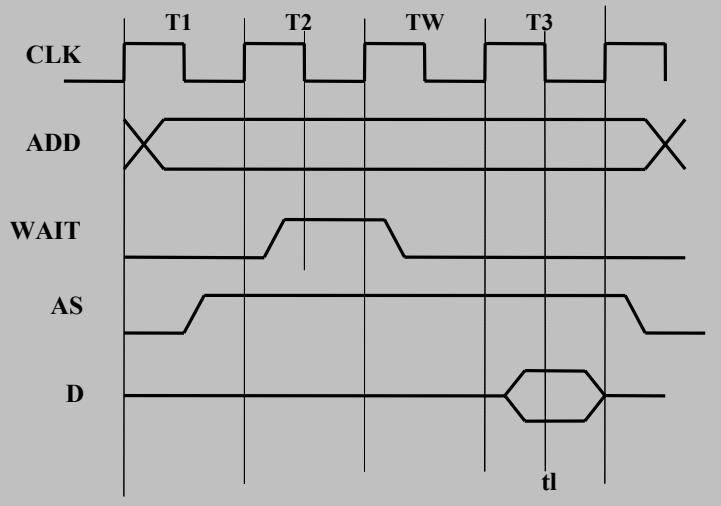
STRICTLY SYNCRONOUS

INFORMATION is INTERCHANGED at PREDETERMINED instants of time, with a single CLOCK (CLK).



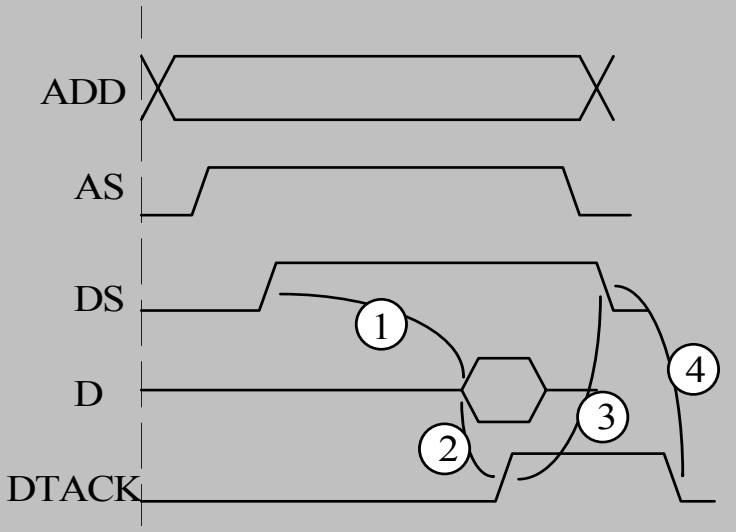
SEMISINCRONOUS

instants are PREFIXED, but can be DELAYED by means of a control signal (WAIT ó READY)

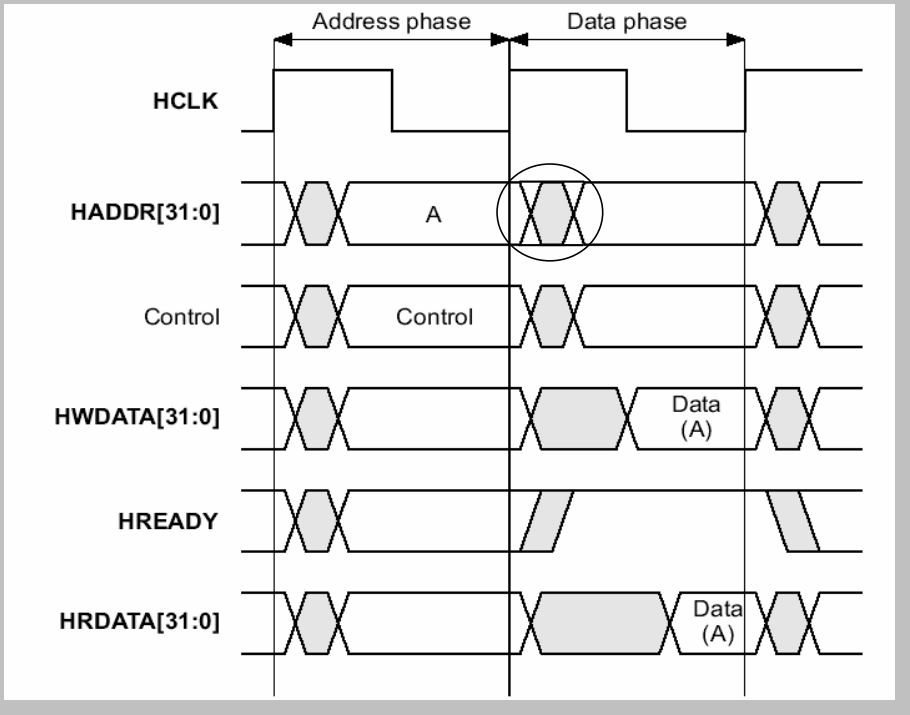


ASINCRONOUS

instants are not prefixed. THERE IS NO CLOCK.



BASIC TRANSFER WITH PIPELINE

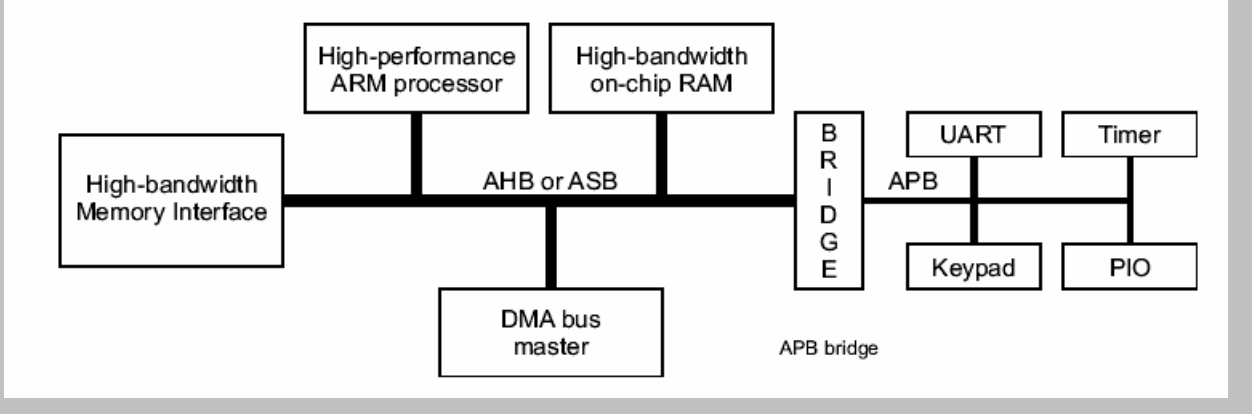


AMBA Bus

(*Advanced Microcontroller Bus Architecture)*

AMBA BUS : APLICATION

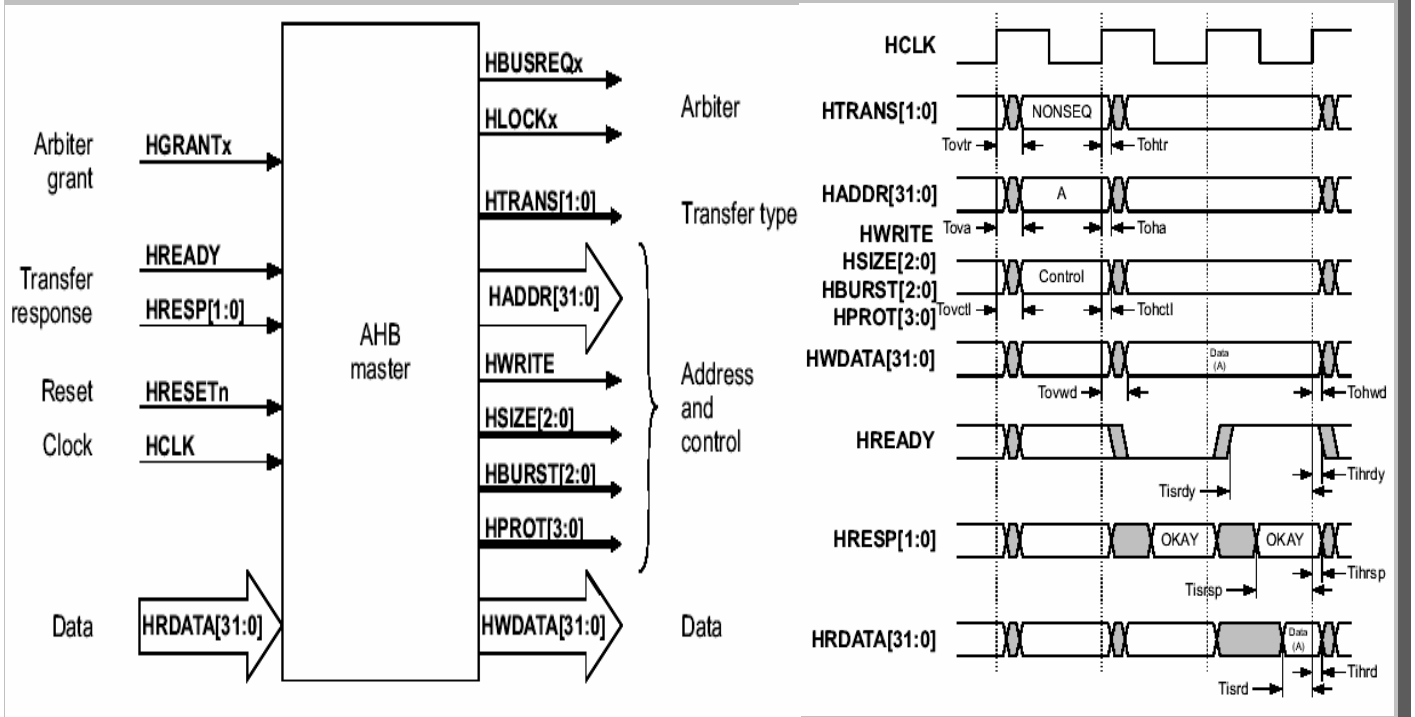
HIGH PERFORMANCE BUS FOR MICROCONTROLERS (ON CHIP)



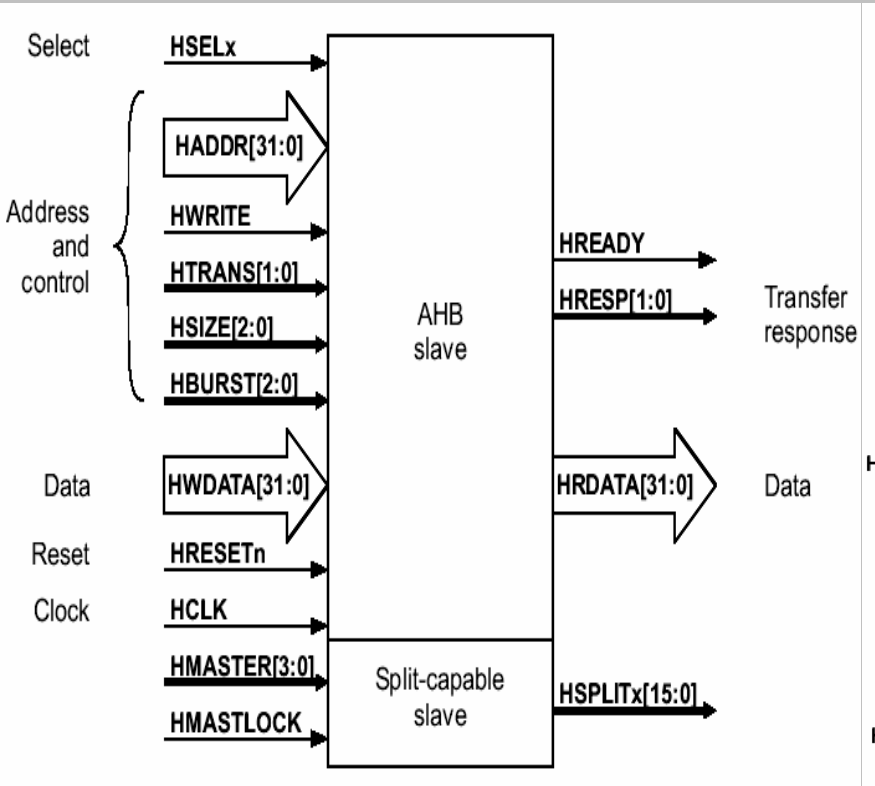
AHB: HIGH PERFORMANCE (UNIDIRECTIONAL DATA BUS)
ASB: MEDIUM PERFORMANCE (BIDIRECTIONAL DATA BUS)
APB: FOR PERIFERALS (SIMPLE TRANSFERS)

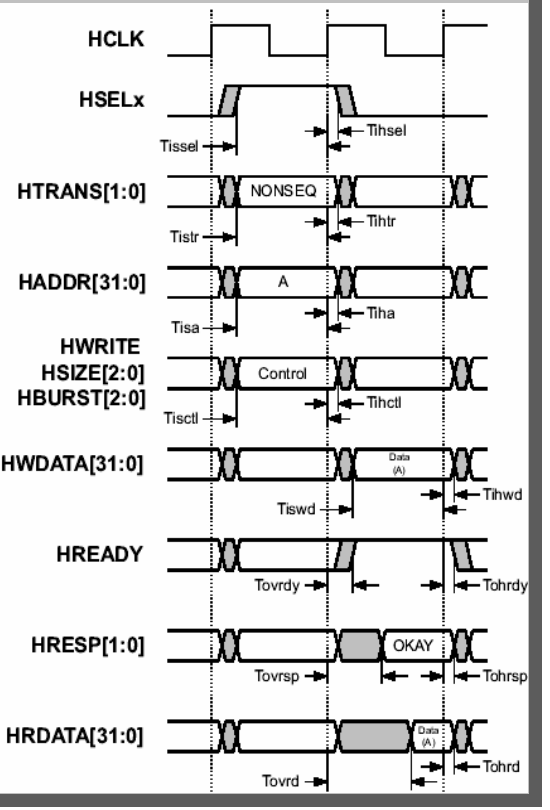
AHB Bus

AMBA AHB: *MASTER*

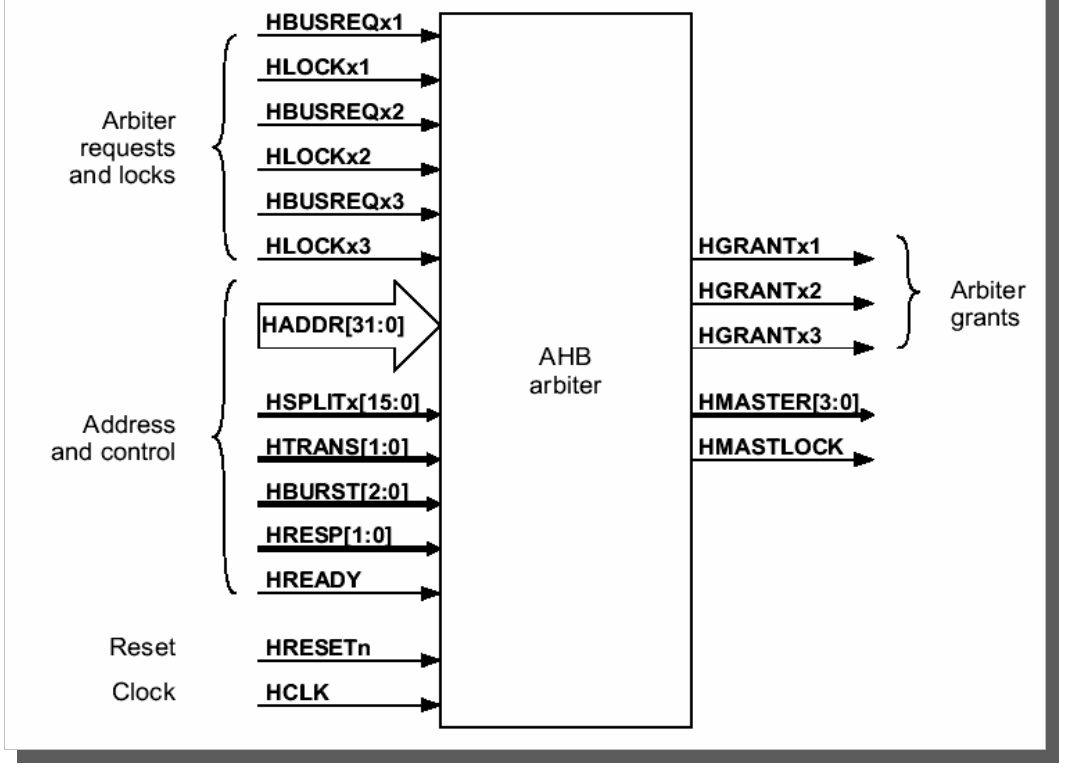


AMBA AHB: *SLAVE*

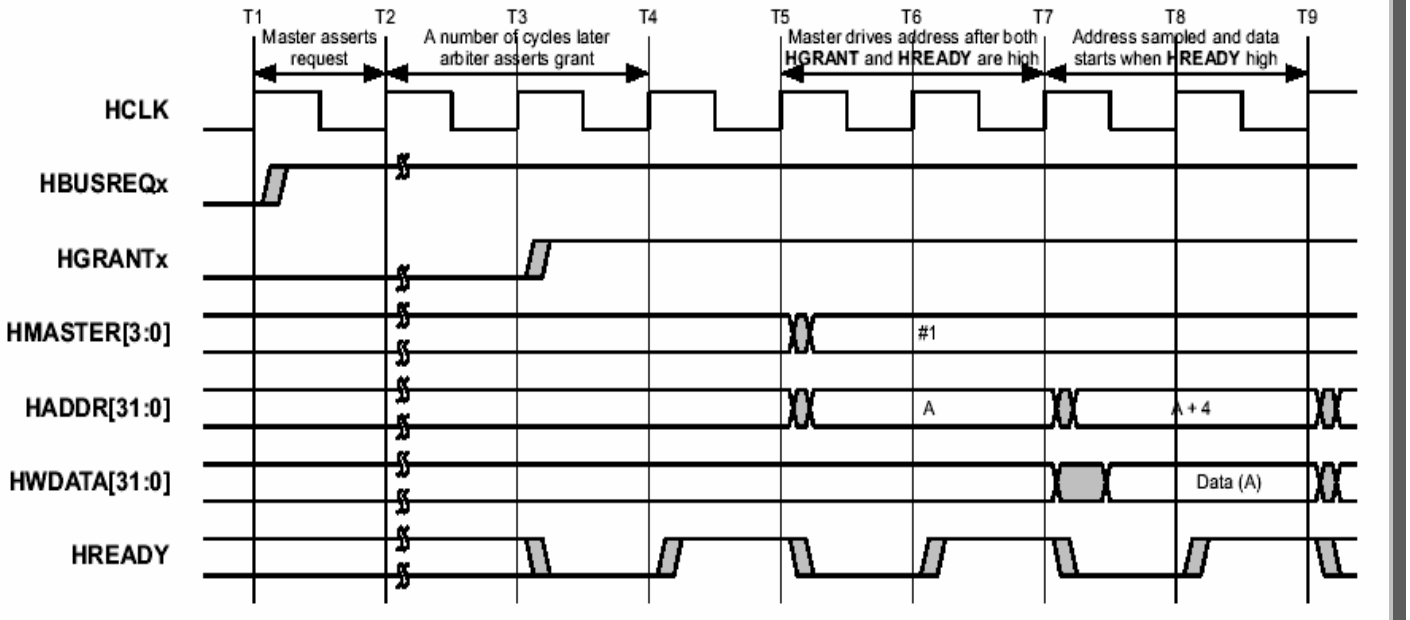




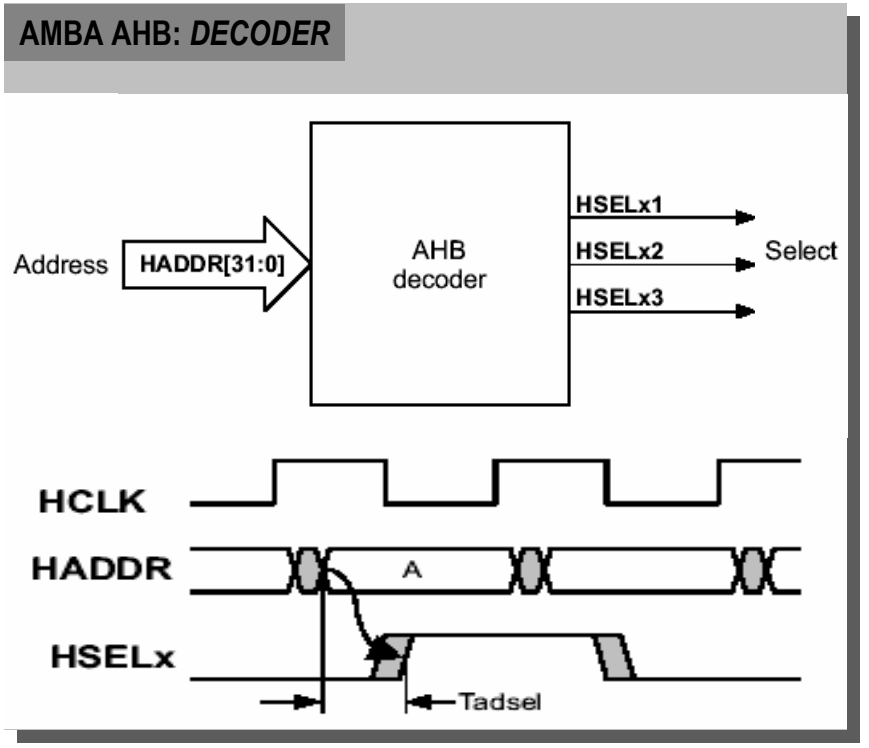
AMBA AHB: *ARBITER*



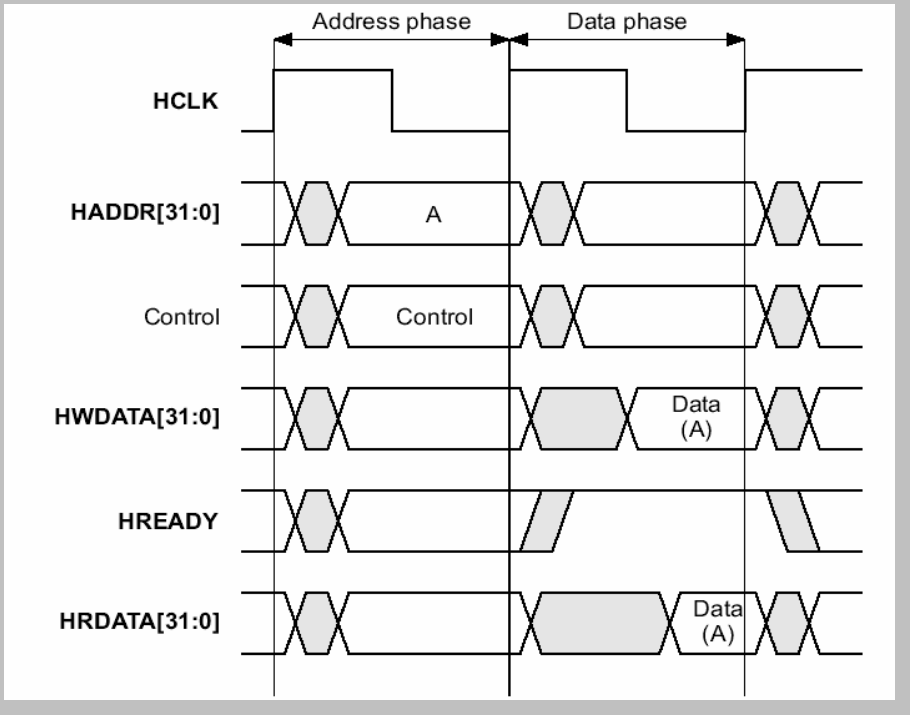
AMBA AHB: ARBITRATION CYCLE



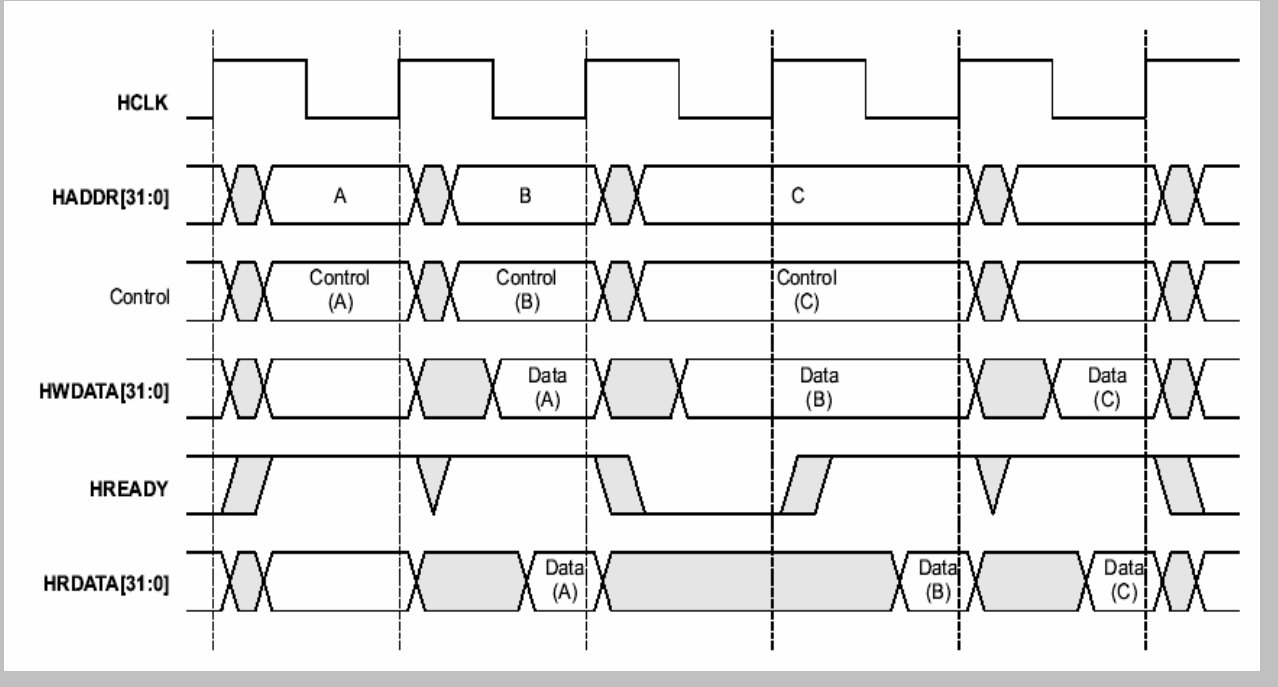
AMBA AHB: *DECODER*



AMBA AHB: BASIC TRANSFER



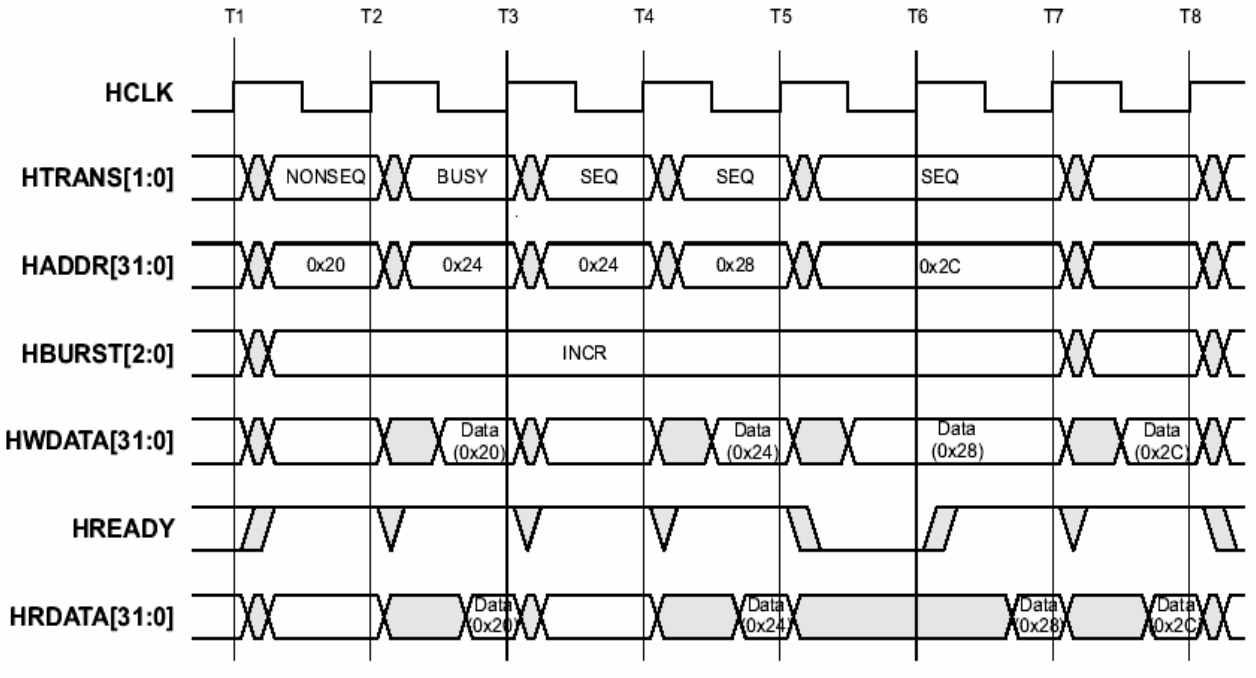
AMBA AHB: TRANSFER WITH *WAIT*



AMBA AHB: TRANSFER TYPES

HTRANS[1:0]	Type	Description
00	IDLE	Indicates that no data transfer is required. The IDLE transfer type is used when a bus master is granted the bus, but does not wish to perform a data transfer. Slaves must always provide a zero wait state OKAY response to IDLE transfers and the transfer should be ignored by the slave.
01	BUSY	The BUSY transfer type allows bus masters to insert IDLE cycles in the middle of bursts of transfers. This transfer type indicates that the bus master is continuing with a burst of transfers, but the next transfer cannot take place immediately. When a master uses the BUSY transfer type the address and control signals must reflect the next transfer in the burst. The transfer should be ignored by the slave. Slaves must always provide a zero wait state OKAY response, in the same way that they respond to IDLE transfers.
10	NONSEQ	Indicates the first transfer of a burst or a single transfer. The address and control signals are unrelated to the previous transfer. Single transfers on the bus are treated as bursts of one and therefore the transfer type is NONSEQUENTIAL.
11	SEQ	The remaining transfers in a burst are SEQUENTIAL and the address is related to the previous transfer. The control information is identical to the previous transfer. The address is equal to the address of the previous transfer plus the size (in bytes). In the case of a wrapping burst the address of the transfer wraps at the address boundary equal to the size (in bytes) multiplied by the number of beats in the transfer (either 4, 8 or 16).

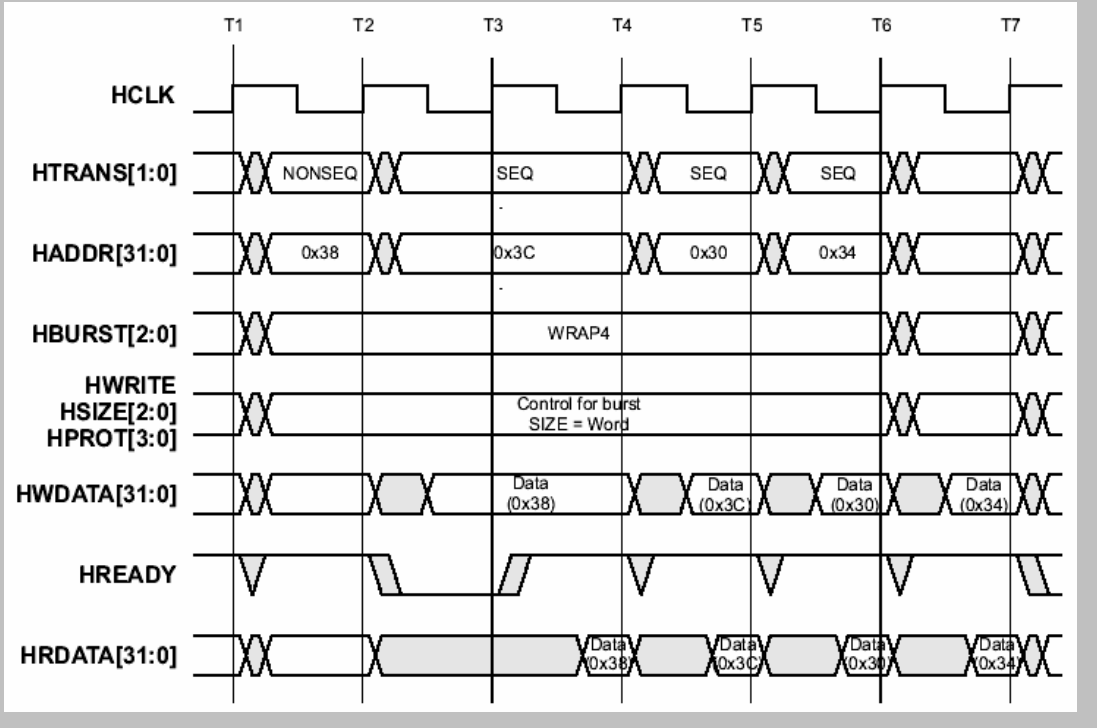
AMBA AHB: TRANSFER TYPES



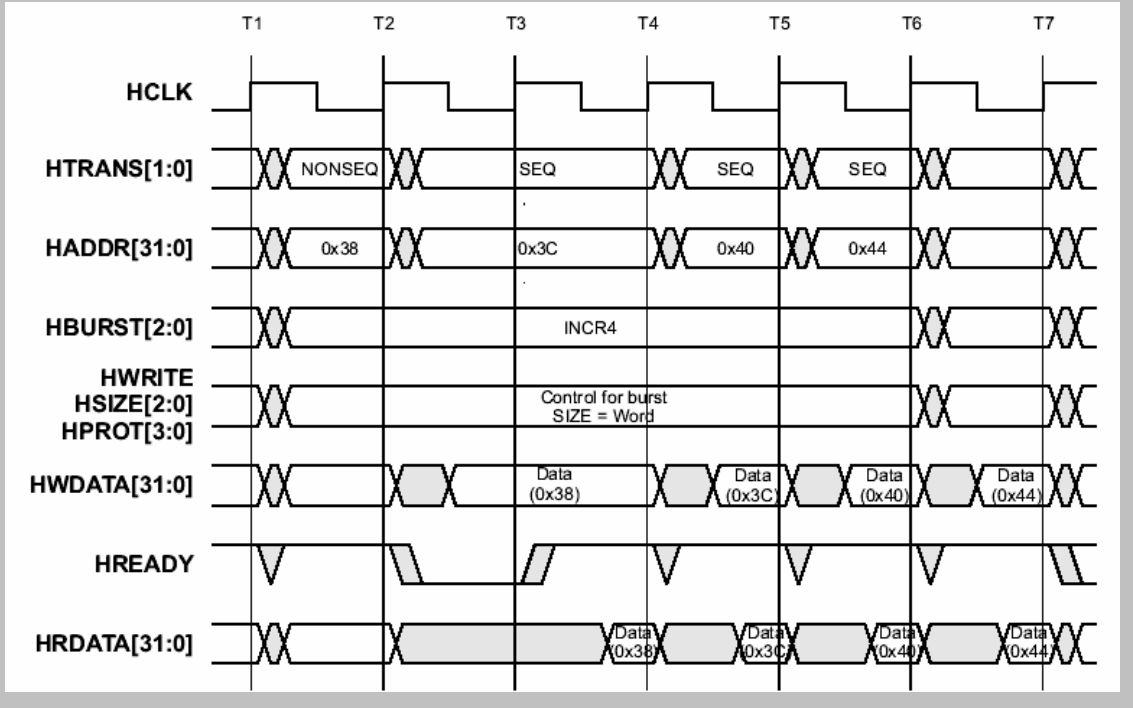
AMBA AHB: BURST TRANSFER TYPES

HBURST[2:0]	Type	Description
000	SINGLE	Single transfer
001	INCR	Incrementing burst of unspecified length
010	WRAP4	4-beat wrapping burst
011	INCR4	4-beat incrementing burst
100	WRAP8	8-beat wrapping burst
101	INCR8	8-beat incrementing burst
110	WRAP16	16-beat wrapping burst
111	INCR16	16-beat incrementing burst

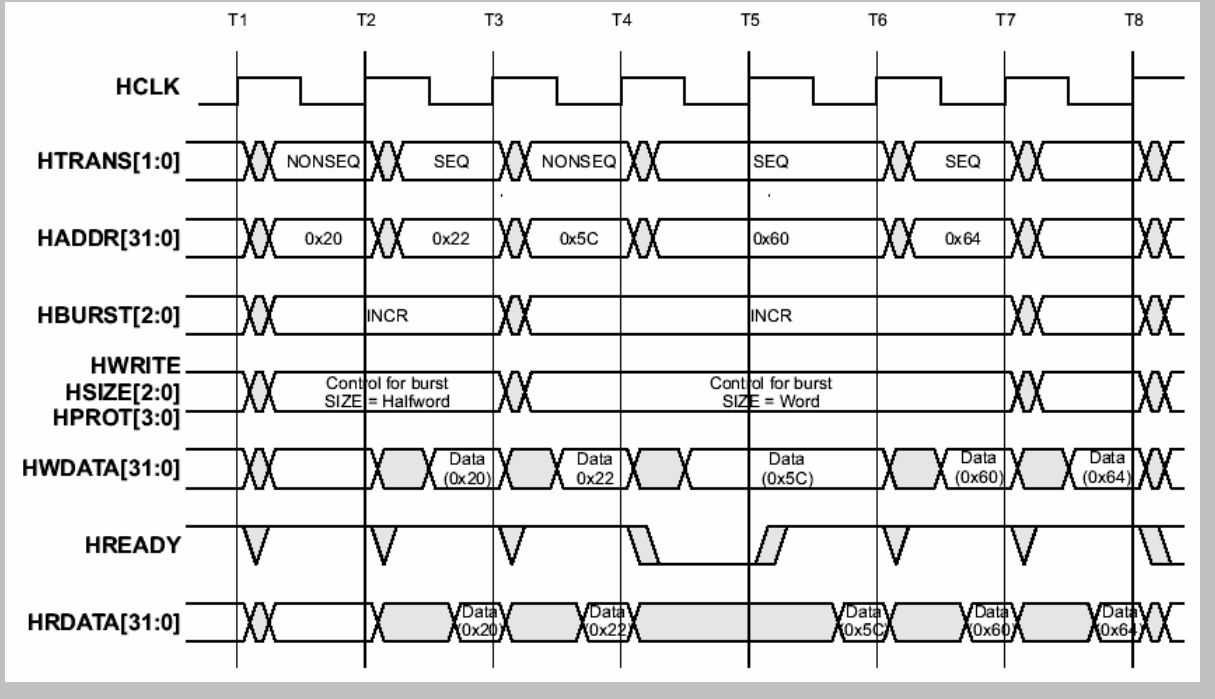
AMBA AHB: BURST TRANSFER TYPES : WRAP AROUND



AMBA AHB: BURST TRANSFER TYPES: INCREMENTAL



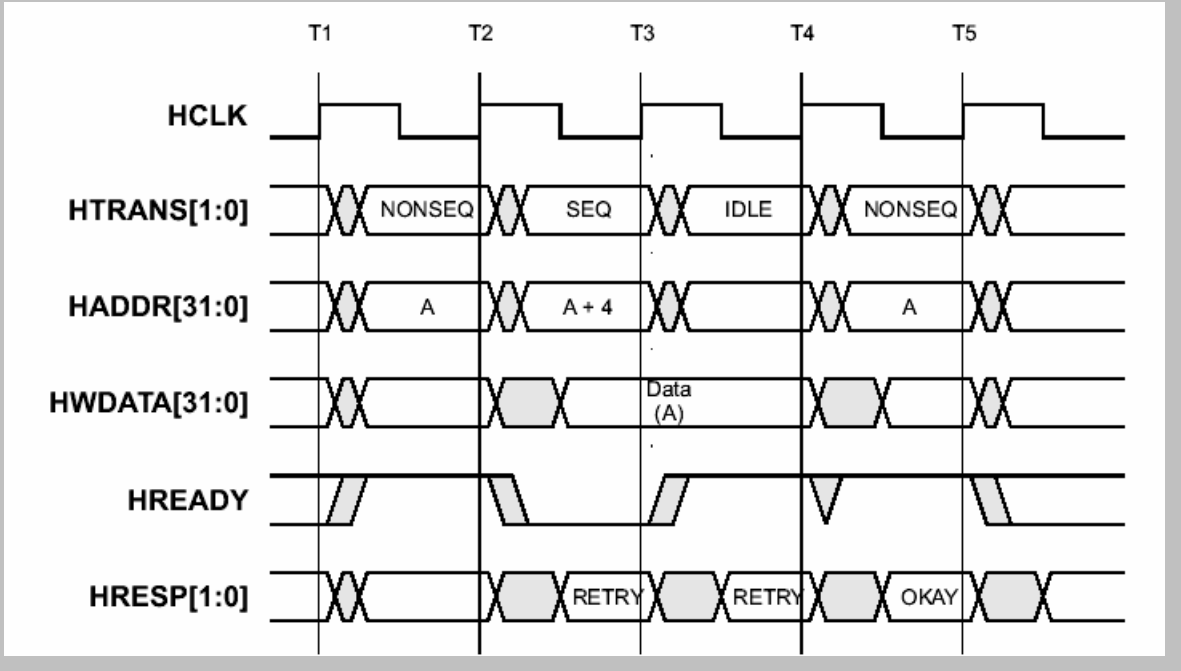
AMBA AHB: BURST TRANSFER TYPES : UNDEFINED



AMBA AHB: SLAVE RESPONSES

HRESP[1]	HRESP[0]	Response	Description
0	0	OKAY	When **HREADY** is HIGH this shows the transfer has completed successfully. The OKAY response is also used for any additional cycles that are inserted, with **HREADY** LOW, prior to giving one of the three other responses.
0	1	ERROR	This response shows an error has occurred. The error condition should be signalled to the bus master so that it is aware the transfer has been unsuccessful. A two-cycle response is required for an error condition.
1	0	RETRY	The RETRY response shows the transfer has not yet completed, so the bus master should retry the transfer. The master should continue to retry the transfer until it completes. A two-cycle RETRY response is required.
1	1	SPLIT	The transfer has not yet completed successfully. The bus master must retry the transfer when it is next granted access to the bus. The slave will request access to the bus on behalf of the master when the transfer can complete. A two-cycle SPLIT response is required.

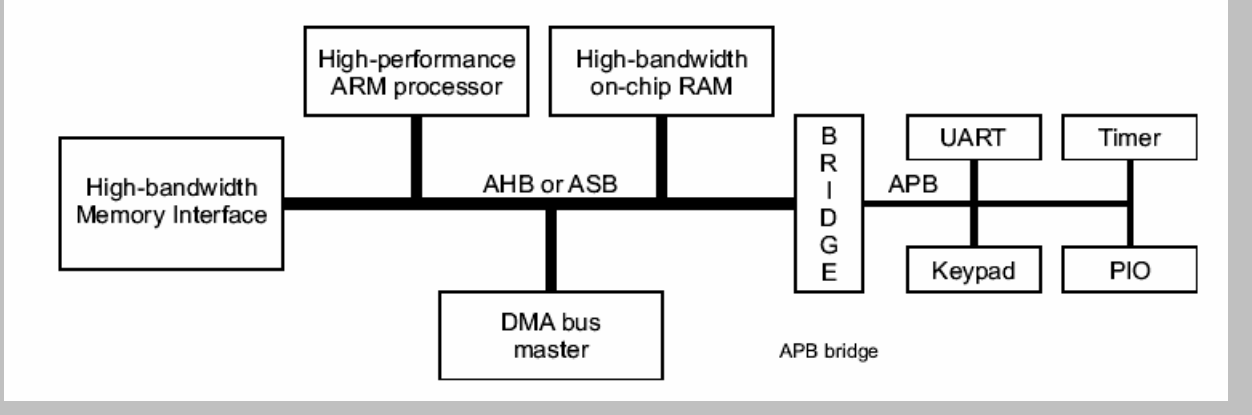
AMBA AHB: SLAVE RESPONSE EXEMPLE



APB Bus

AMBA BUS : APLICATION

HIGH PERFORMANCE BUS FOR MICROCONTROLERS (ON CHIP)



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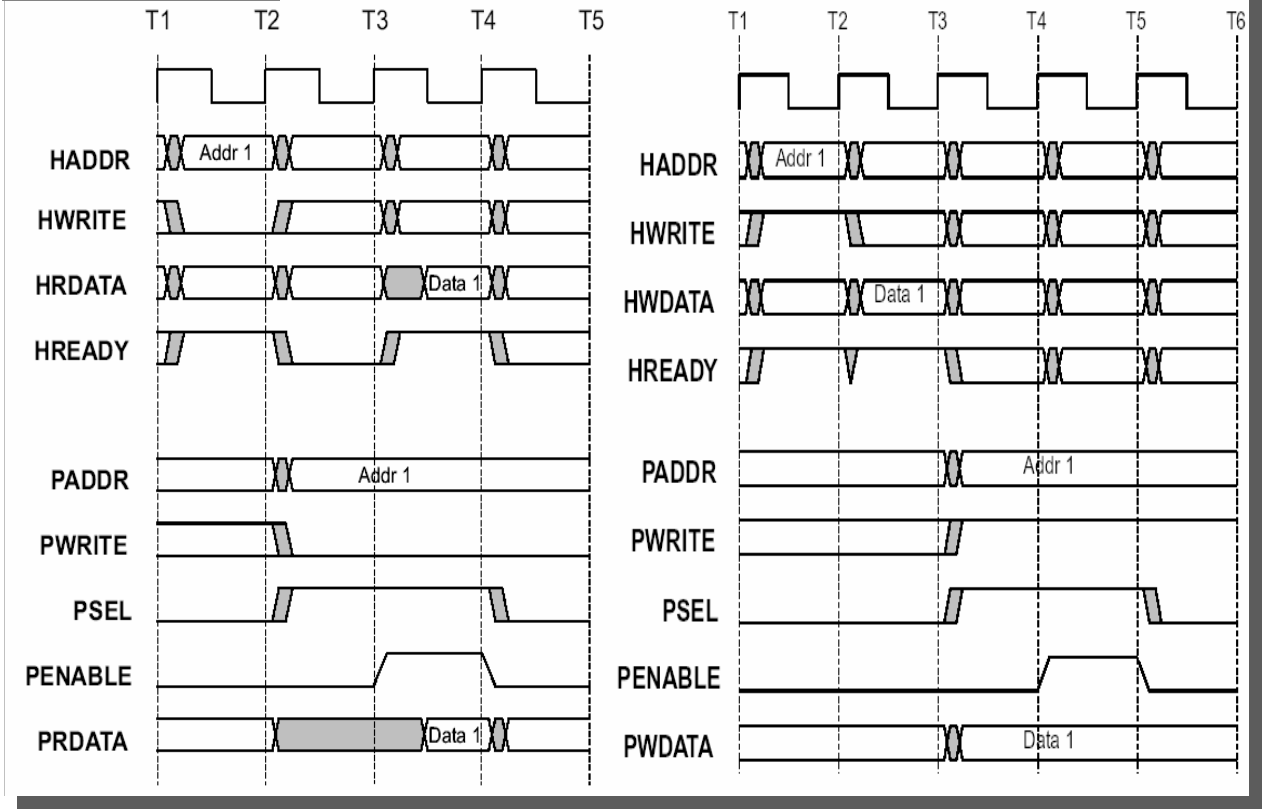
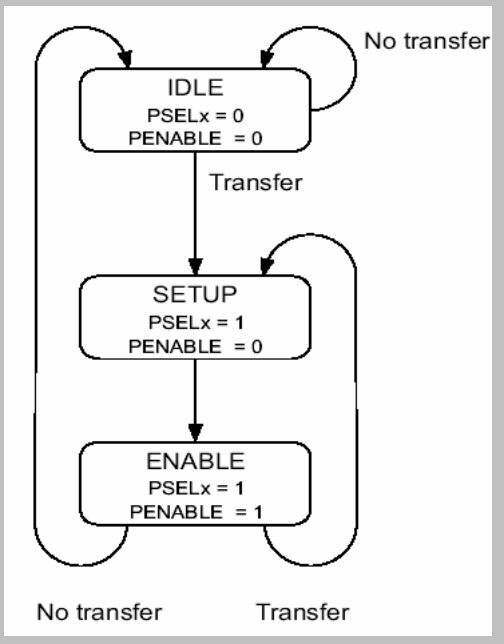
AHB-APB BRIDGE



AMBA APB: STATE DIAGRAM



AMBA APB: TRANSFERS