Chapter 3
Communication Protocols
Introduction:
Parallel/Serial Communication
In a system with binary codification

1 Physic Line ➔ 1 bit
If the indivisible chunk > 1 bit

MULTIPLEXING
× SPACE (Parallel)
× TIME (Serial)

With a binary code, only a bit may be transmitted through a single line. For units of information of more than one bit, whether we use more lines (Space multiplexing or parallel) or we assign a time slot to every bit (Time multiplexing or serial)
<table>
<thead>
<tr>
<th>EXAMPLES</th>
<th></th>
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<tbody>
<tr>
<td>µP Bus</td>
<td></td>
</tr>
<tr>
<td>Parallel</td>
<td>AB, DB, CB</td>
</tr>
<tr>
<td>1 Transfer ≥ 1 Clock cycle</td>
<td></td>
</tr>
<tr>
<td>RS232</td>
<td></td>
</tr>
<tr>
<td>Serial</td>
<td>1 Physic Line</td>
</tr>
<tr>
<td>1 Bit = 1 Clock cycle</td>
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</table>
To recover time multiplexed data we need the clock that has been used to multiplex them, so we need to be synchronized. Strictly speaking, serial transmission is synchronous.

Distinction between synchronous and asynchronous serial transmission is based on how we do recover synchronization.

In synchronous serial transmission without dedicated clock line, clock is recovered from data.
### CONSEQUENCES OF SYNCRONIZATION METHOD

**ASYNCRONOUS SERIAL COMMUNICATION**
- Clock shift accumulation
- Limited message length
- Limited transmission speed

**SYNCRONOUS SERIAL COMMUNICATION**
- Constant synchronization
- Strictly synchronous
- Extra clock line
- Periodic synchronization
- Synchronization rate depends on speed
- Synchronization depends on message
I2C Bus
Separate CLOCK (SCL) and DATA (SDA) lines
Uses DOMINANT STATE SIGNALING (Output devices are open collector or open drain)
DOMINANT state is line at low level, when ANY device connected to the line is transmitting a low level.
RECESSIVE state is line at high level, when ALL devices connected to the line are transmitting a high level.
I2C: DATA SYNCRONIZATION

SDA

SCL

Valid Data

Change is allowed
I2C: TRANSMISSION START AND STOP

SDA

SCL

Start Condition

Stop Condition
Basic transfer is:
1) Start condition
2) 7 address bits
3) 1 R/W* bit
4) 1 address acknowledge bit (Slave forcing a dominant level)
5) Undefined time (optional) of “Slave not ready”, where slave forces a dominant level in SCL line, thus stopping the transmission until ready.
6) 8 data bits or 8 bit groups in case of multiple data transmission.
7) 1 data acknowledge bit (for every data byte)
8) Stop condition
During acknowledge bit time, *master* leaves SDA line floating (Recessive) and *slave* forces line dominant.
I2C: SCL SYNCRONIZATION

SCL = SCL1 and SCL2
Address containing more dominant bits gets the bus
I2C: BUS EXTENSIONS

- Standard (S): Up to 100 Kb/s
- Fast (F): Up to 400 Kb/s
- High Speed (Hs): Up to 3.4 Mb/s
- 10 bit Address

See I2C specs (Annexed documents)
Digital Systems

I2C: FAST MODE: P.U. RESISTANCE

ON=0.8V
OFF=2V

Needed from $C_L = 200\text{pF}$

See I2C specs (Annexed documents)
I2C: ASYMMETRIC SCL

SDA
Valid Data

SCL
Change is allowed

Longer time for change

SCL may be stretched up to 30-70
Digital Systems

CAN Bus
Physical Layer
1) Sublevel MDI: Standard = 120 ohm twisted pair
2) Signaling: Current mode differential. DOMINANT state signaling
3) Controller: Synchronization, bit timing and coding-decoding.
No Return to Zero (NRZ)
If data do not have a transition at least every 5 bit, a stuffing bit is added for resynchronization.
Two frequency division stages to adjust bit time
TRANSMISSION SPEED ADJUST

TWO OPTIONS: DIVIDING FACTOR & QUANTUM NUMBER
Digital Systems

1 BIT = 4 SEGMENTS

<table>
<thead>
<tr>
<th>Segment</th>
<th>Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>SYNC_SEG</td>
<td>1 tq</td>
</tr>
<tr>
<td>PROP_SEG</td>
<td>1..16 tq</td>
</tr>
<tr>
<td>PHASE_SEG1</td>
<td>1..8 tq</td>
</tr>
<tr>
<td>PHASE_SEG2</td>
<td>Sample Point</td>
</tr>
</tbody>
</table>

Nominal Bit-Time
SEGMENT FUNCTIONALITY

- **SYNC**: Indicates the bit start
- **PROP**: Compensates inter-node delay
- **PHASE 1**: Compensates phase lag
- **PHASE 2**: Compensates phase lead
RJW (Resynchronization Jump Width). Lengthens phase_1 to recover synchronization.
RJW (Resynchronization Jump Width). Shortens phase 2 to recover synchronization
Only end nodes have 120 ohm resistor.
All nodes have to be able to act as a *master*. 
Transmitter:
RECESSIVE: CAN_H-CAN_L < 0.1V
DOMINANT: CAN_H-CAN_L > 2V

Receiver:
RECESSIVE: CAN_H-CAN_L < 0.5V
DOMINANT: CAN_H-CAN_L > 0.9V
Also week Pull-up resistors of 15Kohm approx.
Differential Transmission

Good immunity to common mode noise
Digital Systems

**SIGNALING CHANGE**

FROM FULL DUPLEX TO HALF DUPLEX

- Transmitter (Tx) uses 5V and 0V signals.
- Receiver (Rx) also uses 5V and 0V signals.
- CAN_H and CAN_L signals are used for communication.

In half-duplex mode, data transmission and reception cannot occur simultaneously, allowing for more efficient resource utilization and reduced interference compared to full-duplex systems.
Data Link Layer
MESSAGE TYPES

- **DATA FRAME**: INITIATED BY TRANSMITTER (Contains data)
- **REMOTE FRAME**: INITIATED BY RECEIVER (Data inquiry)
- **ERROR FRAME**: ERROR SIGNALING (Active or passive)
- **OVERLOAD FRAME**: RETRANSMISSION INQUIRY (Delayed)
It is not an address oriented bus but a message oriented bus. Arbitration field DOES NOT MAKE REFERENCE TO THE NODE BUT TO THE MESSAGE ITSELF. The same identifier may be used by more than one node.
Digital Systems

ARBITRATION FIELD FORMAT

**Standard Format**

Remote Frame

Arbitration Field

Control Field

Data Field

SOF 11 bit Identifier RTR IDE r0 DLC

**Extended Format**

Extended Format

Arbitration Field

Control Field

SOF 11 bit Identifier RTR IDE 18 bit Identifier RTR r1 ro DLC
Same that I2C.
Digital Systems

**WHY LIN BUS**

- COST REDUCTION IS VERY IMPORTANT IN THE AUTOMOTIVE INDUSTRY
- CAN BUS FULFILLS THE ROLE BUT TOO EXPENSIVE FOR SIMPLE FUNCTIONS
- SIMPLER PROTOCOL NEEDED FOR SHORT DISTANCE AND LOW SPEED
**MAIN CARACTERISTICS**

- Bidirectional communication through a single wire
- One master and up to 16 slaves
- Dominant-recessive voltage signaling
- Mixture of I2C and RS232
- RC clock with resincronization
- 20 Kbaud maximum speed
- 40 m maximum length
- Can operate along with CAN Bus
DOMINANT-RECESSIVE signaling. The master has a P.U. resistor of 1kohm. Each slave has a week P.U. resistor of 30kohm. The series diode is to protect against polarity reversal (always required in automotive environment)
Data Link Layer
BYTE STRUCTURE AND SPECIAL BYTES

Byte

Sync Delimiter

Sync Byte

START BIT
8 DATA BITS
STOP BIT

TSYNDRK

TSYNDDEL

START BIT 0 1 2 3 4 5 6 7 STOP BIT
Identifier has:
1) Four address bits (16 slaves)
2) Two length bits (2, 4 or 8 bytes message)
3) Two parity bits
MESSAGE FRAME

COMMAND FRAME HEADER

COMMAND/DATA FIELDS

NEXT MESSAGE FRAME

SYNCH BREAK
SYNCH IDENT FIELD

8 BYTE FIELDS

1 CHECK FIELD

SYNCH BREAK
SYNCH FIELD

8 byte fields with user-defined content