SGS-ATES 4000B SERIES INFORMATION

The new SGS-ATES COS/MOS **HCC/HCF 4000B** series meets the industry standardized specifications co-ordinated by EIA/JEDEC Solid State Products Council.
The official JEDEC specifications for static parameters are primarily applicable to gates, inverters, high current (inverting) drivers and devices with Medium Scale Integration.
Special types such as analog switches, multiplexers and multivibrators do not have the same input-output standards as the B series specifications but are still given with a B suffix because they satisfy the remaining JEDEC specifications.

SGS-ATES **HCC/HCF 4000B** types have the following Absolute Maximum Ratings:

Symbol	Description	Limits
V_{DD}	Supply voltage: **HCC**	-0.5 to 20 V
	HCF	-0.5 to 18 V
V_i	Input voltage	-0.5 to V_{DD} +0.5 V
I_i	DC input current (any input)	± 10 mA
P_{tot}	Total power dissipation (per package)	200 mW
	Dissipation per output transistor for T_{op}= full package temp. range	100 mW
T_{op}	Operating temperature: **HCC** types	-55 to 125 °C
	HCF types	-40 to 85 °C
T_{stg}	Storage temperature	-65 to 150 °C

The Recommended Operating Conditions are specified as follows:

Symbol	Description	Limits
V_{DD}	Supply voltage: **HCC**	3 to 18 V
	HCF	3 to 15 V
V_i	Input voltage	0 to V_{DD} V
T_{op}	Operating temperature: **HCC** types	-55 to 125 °C
	HCF types	-40 to 85 °C

If these ratings are compared with the corresponding JEDEC values shown in table II and III it can be seen that the SGS-ATES **HCC/HCF 4000B** devices have much better limits than those of the JEDEC specifications.
The static electrical characteristics of the **HCC/HCF 4000B** series, excluding special devices such as analog switches, multiplexers, drivers, etc. are shown in table I.
The SGS-ATES **HCC/HCF 4000B** family has the quiescent leakage current (I_L) specified at 5, 10, 15, 20 V and the other static electrical characteristics at 5, 10, 15 V for both extended and intermediate temperature ranges.

HCC/HCF 4000B series features

The principal features of the HCC/HCF 4000B series are as follows:

- operating range for **HCC** 3-18V; **HCF** 3-15V
- Rationalised range of quiescent leakage current (I_L) specifications corresponding to gate, buffer and flip-flop, and Medium Scale Integration products.
- Maximum input leakage current (I_{IH}, I_{IL}) of ± 1 μA at V_{DD}= 18V for **HCC**, 15V for **HCF** with V_i = 0 to 18V for **HCC**, 0 to 15V for **HCF** over the full temperature range.
- Input and output logic levels completely independent of temperature.
- Input voltage levels which define a very high DC noise immunity (45% V_{DD} typical).
- Noise margins of 1 V min at 5V V_{DD}
  2 V min at 10V V_{DD}
  2.5V min at 15V V_{DD}
- Low (400 ohm typical) and constant output impedance in both logical states giving fixed and equal output transition times.
- Output current capable of driving

  a) two low power TTL loads
  b) one low power Schottky TTL load
  c) two HLL loads

  over the rated temperature range.
- Output current and input threshold independent of the number of inputs paralleled together.
- Square transfer voltage characteristics.

General COS/MOS characteristics

The main advantages offered by COS/MOS devices over corresponding bipolar devices (DTL, LPS, TTL, ECL, HLL) are:

- very low quiescent power dissipation (typically 10 nW/gate, 10 μW/MSI)
- wide operating voltage range (3 to 18V for **HCC**; 3-15V for **HCF**)
- high input impedance (typically 10^{12} Ω)
- high DC noise immunity (typically 45% of supply voltage).

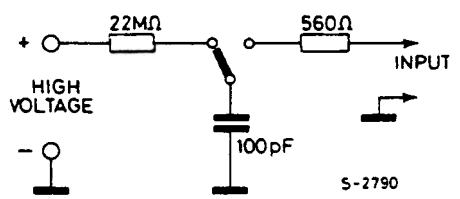
This digital family however has slower switching speeds than most bipolar families. For example the typical propagation times for COS/MOS and other logic families are:

	COS/MOS	ECL	LPS	TTL	DTL	HLL
Propagat. delay time (ns)	35	2	5	10	30	110

Moreover, due to the high input impedance of the MOS gates, COS/MOS devices require greater care in handling.
The normal gate oxide thickness is 800 to 1000 Å with a corresponding breakdown voltage between gate and substrate of 80 to 90V.
The electrostatic potential of the human body is much higher than this range, reaching 12 kV with a discharge capacity of approximately 100 pF. In fact an equivalent body discharge network is shown in fig. A.

SGS-ATES 4000B SERIES INFORMATION (continued)

Fig. A - Equivalent body discharge network



The characteristic values of electrostatic potential in an environment with relative humidity in the range 25% to 36% are as follow:

Source of electrostatic potential	Typical value (kV)	Maximum value (kV)
Person walking on a carpet	12	39
Person walking on vinyl tiles	4	13
Person working at a bench	0.5	3
16 pin DIP in a plastic box	3.5	12
16 pin DIP in plastic tubes used for shipping	0.5	3

Overvoltage protection networks are therefore used for the inputs of COS/MOS device.
The **HCC/HCF 4000B** devices use an improved protection network over that used in the **4000A** series. The level of protection for the **4000B** products has been raised to 4 kV , the previous solution for the **4000A** products protected the gate oxide against electrostatic discharges only up to approximately 1 kV. The following figures show the difference between the two input protection networks for a basic inverter:

Fig. B

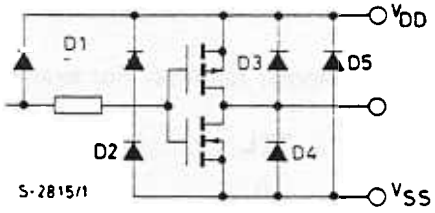
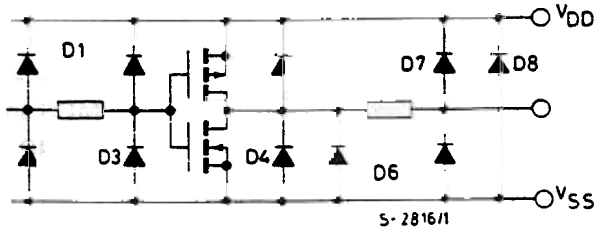


Fig. C



In COS/MOS as in Linear Integrated Circuits a "latch-up" phenomenon may appear. This is caused by an electrical pulse which, acting on an SCR structure of parasitic bipolar transistors inside COS/MOS devices (shown in fig. D), produces a low resistance path between supply voltage and ground that remains after the pulse has ceased leading rapidly to device destruction.

This phenomenon will occur either when V_{DD} is more than the maximum rating and approaches the breakdown voltage of the SCR structure or when the following conditions are verified:

a) the product of the gains of the two parasitic transistors is greater than or equal to unity;

b) the base-emitter junction of both transistors is forward biased;

c) supply voltage and input circuits are able to deliver a current equal to the holding current of the SCR (fig. E).

In particular, condition (b) may be caused by:

1) voltages induced through the oxide by based metallization;

2) lateral voltage drops between substrate and P-well due to photo current generated by radiation. These drops can forward bias the gate-cathode junction of the parasitic SCR.

This effect is particularly significant in buffers which are devices most subject to latch-up due to the combination of large geometry and low silicon resistivity.
For these reasons voltage transients or large output current surges occurring during operation near the maximum rating should be avoided.

Fig. D

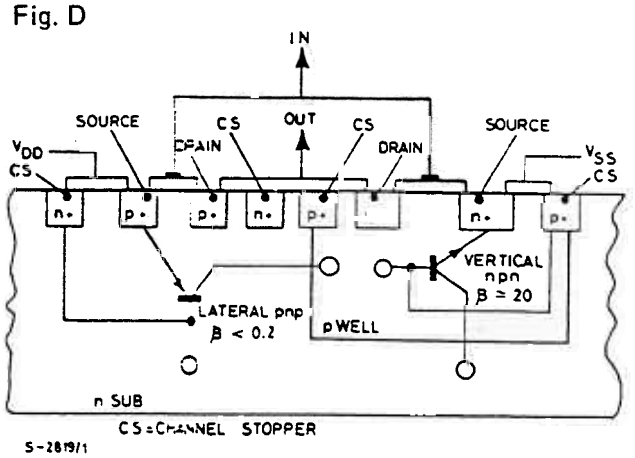
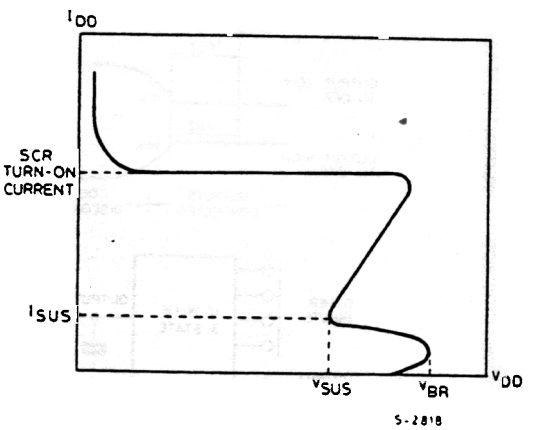


Fig. E



The B series devices are much better protected against latch-up than the A series because of their higher typical breakdown voltage:

Characteristic	A series	B series
V_{BR}	17 V	25 V
V_{SUS}	15 V	22 V
I_{SUS}	10 to 40 mA	50 to 100 mA

SGS-ATES 4000B SERIES INFORMATION (continued)

B series dynamic switching parameters

The dynamic electrical characteristics are specified at T_{amb}= 25°C under the following conditions:

- load capacitance (C_L) of 50 pF and load resistance (R_L) of 200 kΩ;
- input pulse amplitude equal to supply voltage (V_{DD});
- input rise and fall times of 20 ns;
- propagation delay times measured from 50% the point of the input voltage to the 50% point of the output voltage;
- transition times measured from 10% to 90% of the supply voltage (V_{DD}).

In some devices other time parameters are also specified:

a) Set up time
b) Hold time
c) Removal time
d) Tri-state disable delay times.

The figures below show the meaning of these parameters:

Fig. F

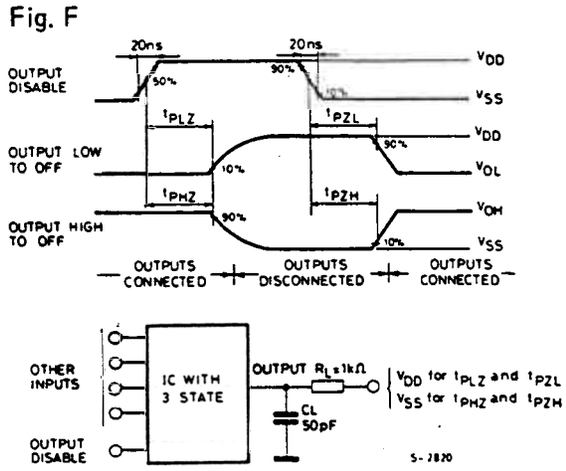
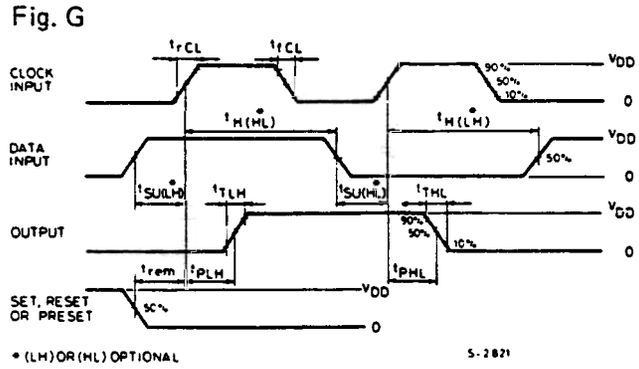


Fig. G



Comparison between B and UB devices

The **HCC/HCF 4000B** family also includes suffix UB products that only meet some of the B series electrical specifications.
These have logic outputs that are not buffered, and V_{IL} and V_{IH} that are specified as 20% V_{DD} and 80% V_{DD} respectively for V_{DD}= 5V and 10V and 17% V_{DD} and 83% V_{DD} respectively for V_{DD}= 15V.

The corresponding values of suffix B types are:

V_{IL}= 30% V_{DD}
V_{IH}= 70% V_{DD} for V_{DD}= 5V and 10V and V_{IL}= 27% V_{DD}
V_{IH}= 73% V_{DD} for V_{DD}= 15V

The other main differences between B and UB gates are summarized below:

Characteristic	Buffered	Unbuffered
Typical output impedance	Constant: 400 Ω (typ.) at V_{DD}= 5V	Variable: dependent on number of inputs paralleled together
Voltage transfer characteristic	Square and independent of the number of inputs tied together	Rounded (as A series) and shifted with different number of inputs paralleled together
Propagation delay	Moderate: 150 ns at V_{DD}= 5V 65 ns at V_{DD}= 10V 50 ns at V_{DD}= 15V	Fast: 60 ns at V_{DD}= 5V 30 ns at V_{DD}= 10V 25 ns at V_{DD}= 15V
AC gain	High and constant: ≃ 68 dB	Low and dependent on supply voltage: 28 dB at V_{DD}= 5V 23 dB at V_{DD}= 10V 18 dB at V_{DD}= 15V
AC band width	Low: 230 kHz at V_{DD}= 5V 280 kHz at V_{DD}= 10V 295 kHz at V_{DD}= 15V	High: 710 kHz at V_{DD}= 5V 885 kHz at V_{DD}= 10V 2800 kHz at V_{DD}= 15V
Input capacitance	Low: average 1 to 2 pF peak 2 to 4 pF	High: average 2 to 3 pF peak 5 to 10 pF
Noise margin	Excellent: 1V at V_{DD}= 5V 2V at V_{DD}= 10V 2.5V at V_{DD}= 15V	Good: 0.5V at V_{DD}= 5V 1V at V_{DD}= 10V 1V at V_{DD}= 15V
Output transition time	200 ns (typ.) at V_{DD}= 5V C_L = 50 pF	50 to 100 ns at V_{DD}= 5V C_L = 50 pF

If B and UB gates are presented with slow transition time signals the behaviour of the two types differs. In fact, because of high AC gain of B devices (obtained with the two extra inverters) the outputs tend to develop a few cycles of oscillation between V_{DD} and V_{SS} when input rise or fall time is more than 1 ms at V_{DD}= 5V and AC noise is reduced to 2 – 3 mV within the B device bandwidth.
The unbuffered gates (which have less gain) tend not to oscillate with the same input ramp unless a noise voltage of 200 to 300 mV is present within the device bandwidth.

GENERAL OPERATING AND HANDLING INSTRUCTIONS

Power source rules

1) Referring to standard input network protection of fig. B, when separate power supplies are used fo V_{DD} and for the device inputs, the V_{DD} supply should always be turned on before the input sign source and the input signal should be turned off before the V_{DD} supply is turned off.
This rule will prevent the D1 input protection diode from overdissipation and possible damage whe the device power supply is grounded.
When the device power supply is an open circuit, violation of this rule can result in undesired circu operation although device damage may not result; AC inputs can be rectified by D1 input diode t act as a power supply.

2) The steady power-supply operating voltage should be kept within the recommended operatir conditions and always below the maximum ratings.

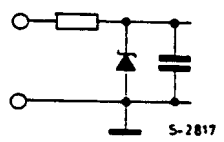
3) The power-supply polarity for COS/MOS circuits should not be reversed. The positive (V_{DD}) te minal should never be more than 0.5V negative with respect to the negative (V_{SS}) terminal (V_{DD} $V_{SS} > -0.5V$). Reversal of polarities will forward-bias and short the structural and protection dioc between V_{DD} and V_{SS}.

4) Power-source current capability should be limited to the minimum value which will assure goc logic operation.

5) Large values of resistors in series with V_{DD} or V_{SS} should be avoided; transient turn-on of inpu protection diodes can result from drops across such resistors during switching.

A good practice is to use a zener protection diode in parallel with the power bus as shown in fig. below.
The zener value should be above the expected maximum regulation excursion, but should not excee the maximum supply voltage.
A current limiting resistor is included if the supply impedance is lower than the zener power dissipatio rating allow for a given zener voltage.
The shunt capacitor value is chosen to supply required peak current switching transients.

Fig. H



Input signal rules

1) Signals should not be applied to the inputs while the device power supply is off unless the input cu rent is limited to a steady-state value of less than 10 mA. Input-signal interfaces that swing the allov able 0.5V above V_{DD} or below V_{SS} should be current-limited to 10 mA or less.
Whenever the possibility of exceeding 10 mA of input current exists, a resistor in series with the inpu must be used. The value of this resistor can be as high as 10 kΩ without affecting static electric characteristics. However, speed will be reduced because of the added RC time constant.
Particular attention should be given to long input-signal lines where high inductance can increase th likelihood of large-signal pickup in noisy environments. In these cases, series resistance with shur capacitance at the IC input terminals is recommended. The shunt capacitance should be made as larg as possible consistent with the system speed requirements.

2) All COS/MOS inputs should be terminated. When COS/MOS inputs are wired to edge card connecto with COS/MOS drive coming from another PC board, a shunt resistor should be connected to V_D or V_{SS}.

3) When COS/MOS circuits are driven by TTL logic a pull-up resistor should be connected from the COS/MOS inputs to 5V.

4) Input signals should be maintained within the recommended input signal swing range.

5) Input rise and fall times for clocked devices must not exceed 15 μs in order to avoid high consumption, false triggering, etc. With slower inputs a Schmitt trigger must be employed.

Output rules

1) The power dissipation in a COS/MOS package should not exceed the rated value for the ambient temperature specified. The actual dissipation should be calculated when (a) shorting outputs directly to V_{DD} or V_{SS}, (b) driving low-impedance loads, or (c) directly driving the base of PNP or NPN bipolar transistors.

2) Output short circuits often result from testing errors or improper board assembly. Shorts on buffer outputs on power supplies greater than 5V can damage COS/MOS devices.

3) COS/MOS, like active pull-up TTL, cannot be connected in the "wire-OR" configuration because an "on" PMOS and an "on" NMOS transistor could be directly shorted across the power-supply rails. For applications with wire OR configurations it is necessary to use devices with tri-state logic outputs.

4) Paralleling gates is recommended only when the gates are within the same IC package.

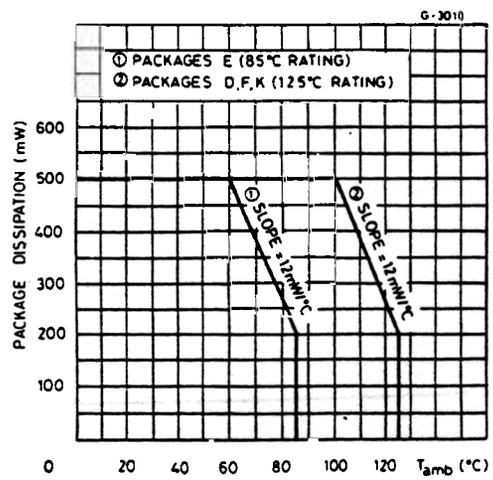
5) Output loads should return to a voltage within the supply-voltage range (V_{DD} to V_{SS}).

6) Large capacitive loads (greater than 5000 pF) on COS/MOS buffers or high-current drivers act like short circuits and may over-dissipate output transistors.

7) Output transistors may be over-dissipated by operating buffers as linear amplifiers or using these types as one-shot or astable multivibrators.

8) Shorting of output to V_{SS} or V_{DD} can cause the device power dissipation to exceed the safe value of 500 mW as shown in fig. I.
This is possible with supply voltage higher than 5V.
For cases in which a short circuited load is driven directly (base of PNP or NPN bipolar transistor) the requirements for gate operation must be determined by consulting the published data. Note that a individual output transistor dissipation must be limited to 100 mW.

Fig. I - Standard COS/MOS thermal derating chart



Noise Immunity and Noise Margin

DC Noise Immunity

The V_{IL} and V_{IH} characteristics define the maximum tolerable noise voltages at an input terminal when input signals are within 50 mV of supply lines.

Noise Margin

The noise margin voltage is the maximum voltage that can be added, at an input voltage $V_i = V_{OL}$ or V_{OH} of the preceding stage without upsetting the logic or causing the output to exceed the output voltage V_o.
In practice, DC noise immunity is much more significant than noise margin because the COS/MOS outputs are normally within 50 mV of supply lines. Noise immunity increases if the input pulse width becomes less than the propagation delay of the circuit.
This condition is often described as AC noise immunity.

Handling rules

Since each user's manufacturing environment is different it is only possible to give some general notes for avoiding damage from electrostatic voltages:

a) handling equipment, trays, table tops and transport carts should be conductive;

b) metal parts of fixtures, tools, soldering irons and table tops should be grounded to a common point;

c) operators should use grounded (metal or conductive) plastic wrist straps with a 1 MΩ series resistor;

d) packages should not be removed from their conductive or antistatic carriers until required; this should only be done by a grounded operator. Devices removed should be placed in a conductive tray;

e) all tests should be performed by a grounded operator and after completion of test, devices should be reinserted in conductive carriers;

f) the printed circuit boards should have shorting bars installed prior to assembly (soldering). When possible COS/MOS IC's should be the last component installed on PC boards.

Table I - STATIC ELECTRICAL CHARACTERISTICS (SGS-ATES 4000B and UB)

Parameter		Test conditions				Values						Unit
		V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}		25°C		T_{High}		
						Min.	Max.	Min.	Max.	Min.	Max.	
I_L (gates)	HCC types	0/ 5			5		0.25		0.25		7.5	μA
		0/10			10		0.5		0.5		15	
		0/15			15		1		1		30	
		0/20			20		5		5		150	
	HCF types	0/ 5			5		1		1		7.5	
		0/10			10		2		2		15	
		0/15			15		4		4		30	
I_L (buffer, FF)	HCC types	0/ 5			5		1		1		30	μA
		0/10			10		2		2		60	
		0/15			15		4		4		120	
		0/20			20		20		20		600	
	HCF types	0/ 5			5		4		4		30	
		0/10			10		8		8		60	
		0/15			15		16		16		120	
I_L (MSI)	HCC types	0/ 5			5		5		5		150	μA
		0/10			10		10		20		300	
		0/15			15		20		20		600	
		0/20			20		100		100		3000	
	HCF types	0/ 5			5		20		20		150	
		0/10			10		40		40		300	
		0/15			15		80		80		600	
V_{OH}		0/ 5		< 1	5	4.95		4.95		4.95		V
		0/10		< 1	10	9.95		9.95		9.95		
		0/15		< 1	15	14.95		14.95		14.95		
V_{OL}		5/0		< 1	5		0.05		0.05		0.05	V
		10/0		< 1	10		0.05		0.05		0.05	
		15/0		< 1	15		0.05		0.05		0.05	
V_{IH} (B series)			0.5/4.5	< 1	5	3.5		3.5		3.5		V
			1/9	< 1	10	7		7		7		
			1.5/13.5	< 1	15	11		11		11		
V_{IL} (B series)			4.5/0.5	< 1	5		1.5		1.5		1.5	V
			9/1	< 1	10		3		3		3	
			13.5/1.5	< 1	15		4		4		4	
V_{IH} (UB series)			0.5/4.5	< 1	5	4		4		4		V
			1/9	< 1	10	8		8		8		
			2/13	< 1	15	12		12		12		
V_{IL} (UB series)			4.5/0.5	< 1	5		1		1		1	V
			9/1	< 1	10		2		2		2	
			13/2	< 1	15		3		3		3	
I_{OH}	HCC types	0/ 5	2.5		5	-2		-1.6		-1.15		mA
		0/ 5	4.6		5	-0.64		-0.51		-0.36		
		0/10	9.5		10	-1.6		-1.3		-0.9		
		0/15	13.5		15	-4.2		-3.4		-2.4		
	HCF types	0/ 5	2.5		5	-1.53		-1.36		-1.1		
		0/ 5	4.6		5	-0.52		-0.44		-0.36		
		0/10	9.5		10	-1.30		-1.1		-0.90		
		0/15	13.5		15	-3.6		-3		-2.4		
I_{OL}	HCC types	0/ 5	0.4		5	0.64		0.51		0.36		mA
		0/10	0.5		10	1.6		1.3		0.9		
		0/15	1.5		15	4.2		3.4		2.4		
	HCF types	0/ 5	0.4		5	0.52		0.44		0.36		
		0/10	0.5		10	1.3		1.1		0.9		
		0/15	1.5		15	3.6		3		2.4		

Table I - STATIC ELECTRICAL CHARACTERISTICS (continued)

Parameter		Test conditions				Values						Unit
		V_I (V)	V_O (V)	$\|I_O\|$ (μA)	V_{DD} (V)	T_{Low}		25°C		T_{High}		
						Min.	Max.	Min.	Max.	Min.	Max.	
I_{IL}, I_{IH}	HCC types	0/18	Any input		18		±0.1		±0.1		± 1	μA
	HCF types	0/15			15		±0.3		±0.3		± 1	
I_{OL},I_{OH}	HCC types	0/18			18		±0.4		±0.4		± 12	μA
	HCF types	0/15			15		±1.0		±1.0		±7.5	
C_i									7.5			pF
$C_{i(UB)}$									22.5			pF

STANDARD JEDEC SPECIFICATIONS

Table II - ABSOLUTE MAXIMUM RATINGS

Symbol	Description	Limits
V_{DD}	Supply voltage	-0.5 to 18 V
V_i	Input voltage	-0.5 to V_{DD} +0.5 V
I_i	DC input current (any input)	± 10 mA
T_{st}	Storage temperature range	-65 to 150 °C

Table III - RECOMMENDED OPERATING CONDITIONS

Symbol	Description	Limits
V_{DD}	Supply voltage	3 to 15 V
V_i	Input voltage	0 to V_{DD} V
T_{op}	Operating temperature for extended range devices	-55 to 125 °C
	for intermediate range devices	-40 to 85 °C

Table IV - STATIC ELECTRICAL JEDEC CHARACTERISTICS

Parameter		Test conditions				Values						Unit
		V_i (V)	V_o (V)	$\|I_o\|$ (μA)	V_{DD} (V)	T_{Low}		25°C		T_{High}		
						Min.	Max.	Min.	Max.	Min.	Max.	
I_L (gates)	HCC				5		0.25		0.25		7.5	μA
					10		0.5		0.5		15	
					15		1		1		30	
	HCF				5		1		1		7,5	μA
					10		2		2		15	
					15		4		4		30	
I_L (buffer FF)	HCC				5		4		4		30	μA
					10		8		8		60	
					15		16		16		120	
	HCF				5		4		4		30	μA
					10		8		8		60	
					15		16		16		120	
I_L (MSI)	HCC				5		5		5		150	μA
					10		10		10		300	
					15		20		20		600	
	HCF				5		20		20		150	μA
					10		40		40		300	
					15		80		80		600	
V_{OL}		0/ 5		< 1	5		0.05		0.05		0.05	V
		0/10		< 1	10		0.05		0.05		0.05	
		0/15		< 1	15		0.05		0.05		0.05	
V_{OH}		5/0		< 1	5	4.95		4.95		4.95		V
		10/0		< 1	10	9.95		9.95		9.95		
		15/0		< 1	15	14.95		14.95		14.95		
V_{IL}			0.5/4.5	< 1	5		1.5		1.5		1.5	V
			1/9	< 1	10		3		3		3	
			1.5/13.5	< 1	15		4		4		4	
V_{IH}			4.5/0.5	< 1	5	3.5		3.5		3.5		V
			9/1	< 1	10	7		7		7		
			13.5/1.5	< 1	15	11		11		11		
I_{OL}	HCC	0/ 5	0.4		5	0.64		0.51		0.36		mA
		0/10	0.5		10	1.6		1.3		0.9		
		0/15	1.5		15	4.2		3.4		2.4		
	HCF	0/ 5	0.4		5	0.52		0.44		0.36		mA
		0/10	0.5		10	1.3		1.1		0.9		
		0/15	1.5		15	3.6		3		2.4		
I_{OH}	HCC	0/ 5	4.6		5	-0.25		-0.2		-0.14		mA
		0/10	9.5		10	-0.62		-0.5		-0.35		
		0/15	13.5		15	-1.8		-1.5		-1.1		
	HCF	0/ 5	4.6		5	-0.2		-0.16		-0.12		mA
		0/10	9.5		10	-0.5		-0.4		-0.3		
		0/15	13.5		15	-1.4		-1.2		-1.0		
I_i	HCC	0/15			15		± 0.1		± 0.1		± 1	μA
	HCF	0/15			15		± 0.3		± 0.3		± 1	μA