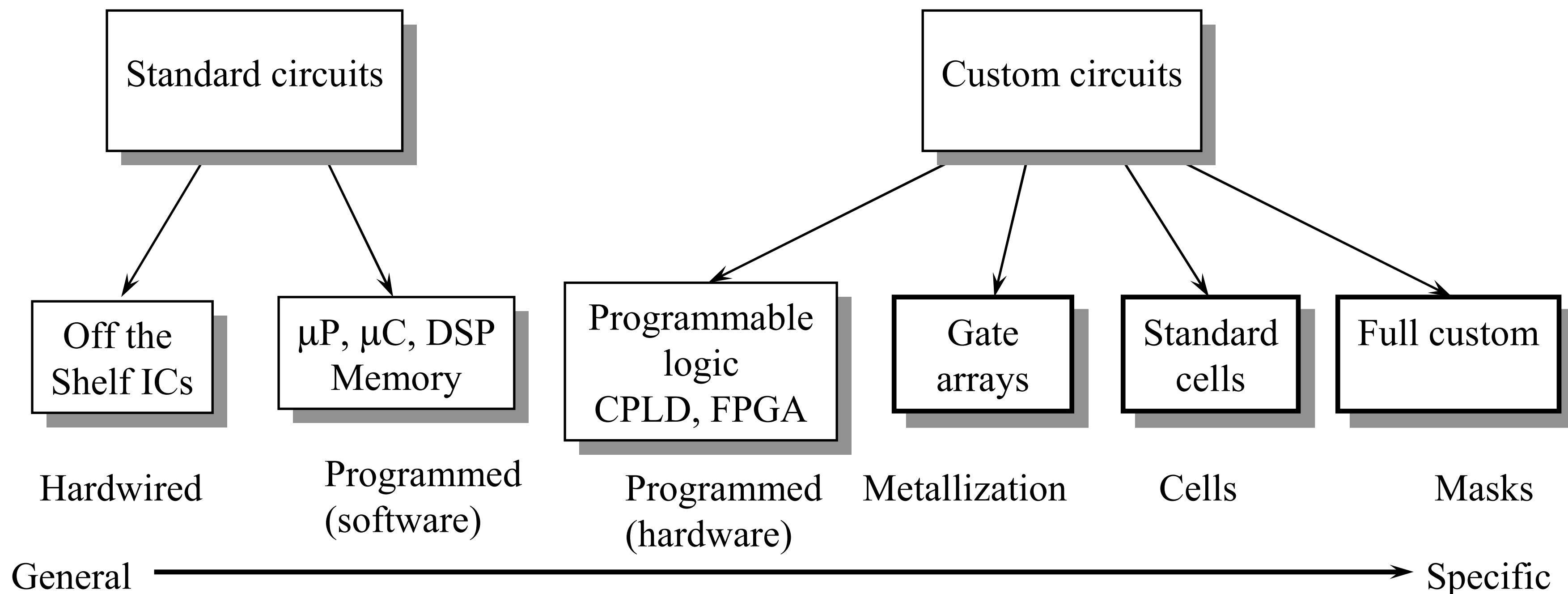
VLSI Digital Design

MODULE I
INTRODUCTION

1.1. Technologies for digital design
1.2. Integration capability and future trends
1.3. Design Techniques
1.4. State of the art
1.5. Synchronous design review
    1.5.1. Non-recommended digital design techniques
    1.5.2. Synchronous flip-flops
    1.5.3. Building synchronous systems

1.1 Technologies for digital design



N: number of units, P: Power consumption, T: design time, f: operating frequency, S: Size, R: Reliability

Semicustom Integrated Circuits

Gate Arrays: Committed gate or transistor array except some interconnect metal layers

+ Fewer specific masks
+ Lower cost than *standard cells*
+ High integration
+ Moderate power consumption
+ High performance (fast)

- Fixed array of transistors
- Reduced flexibility (devices not used)
- Manufacturing time
- Not reprogrammable (hardware)

Standard Cells: Pre-defined circuits that are interconnected according to the user design

+ Device usage efficiency
+ High integration
+ Lower power consumption
+ High performance (fast)
+ Permits third-party predefined modules

- Manufacturing time
- All masks have to be manufactured
-High cost (except in large manufacturing
- volume)
- Not reprogrammable (hardware)

Full Custom Integrated Circuits

Complete definition of all the IC (Integrated Circuit) layers.

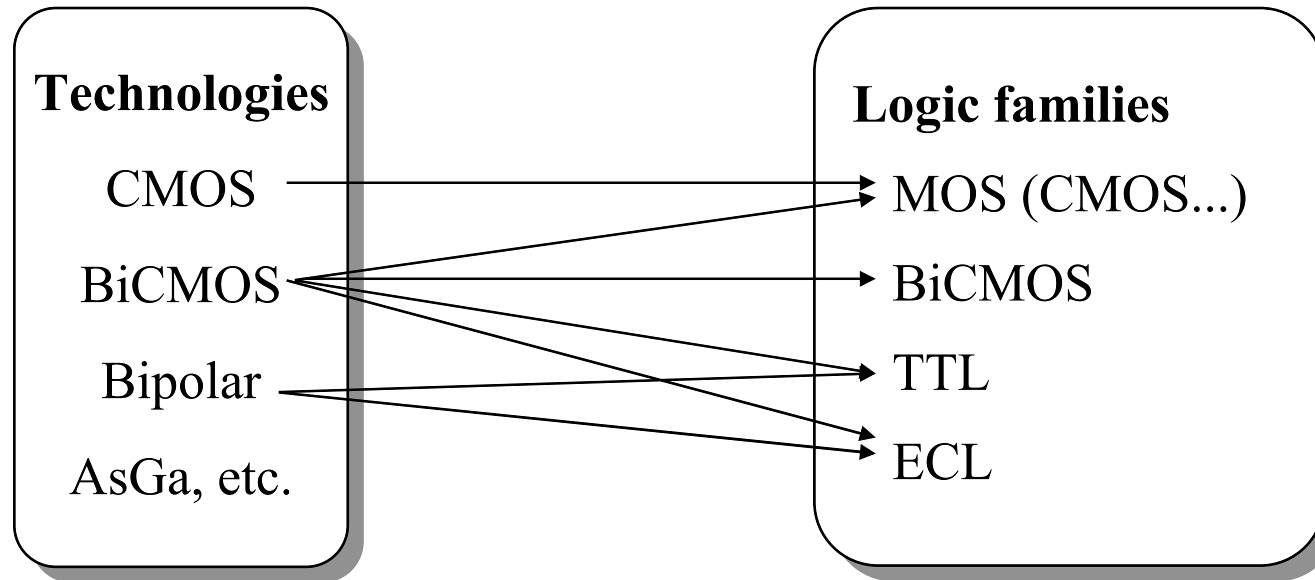
+ Maximum efficiency in area, speed and power consumption

- Very long design time (cost)
- Manufacturing time as in standard cells
- Not reprogrammable (hardware)

Applications:

- Massive ICs (commercial general-purpose processors, memories, etc.)
- Very high-speed / low power or special applications
- Analog and/or RF circuits

Technologies and logic families

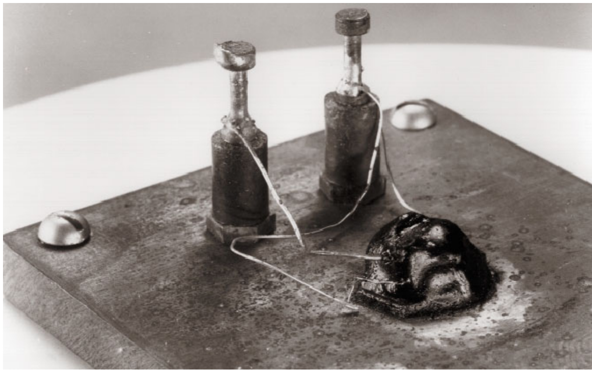


MOS/CMOS prevails:
- High integration capability
- Low power(?): f(CK), short channel
- Parasitic capacitances: memory
- Low cost

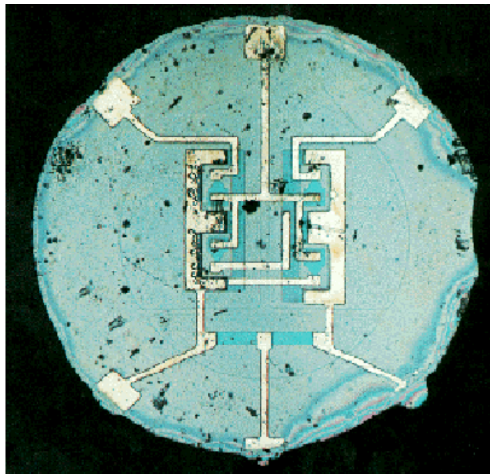
Bipolar: High frequency

BiCMOS: High performance, CMOS-compatible

1.2 Integration capability and future trends

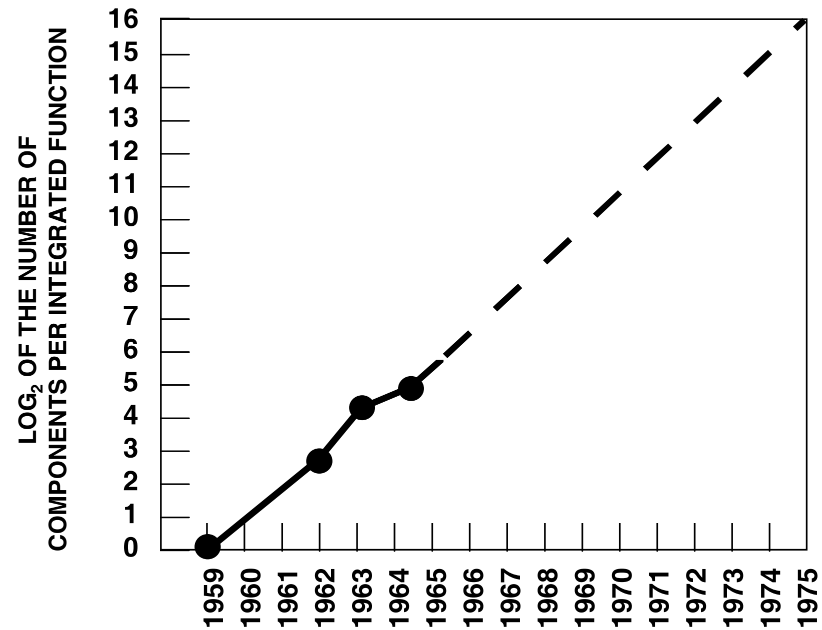


The first transistor



The first IC

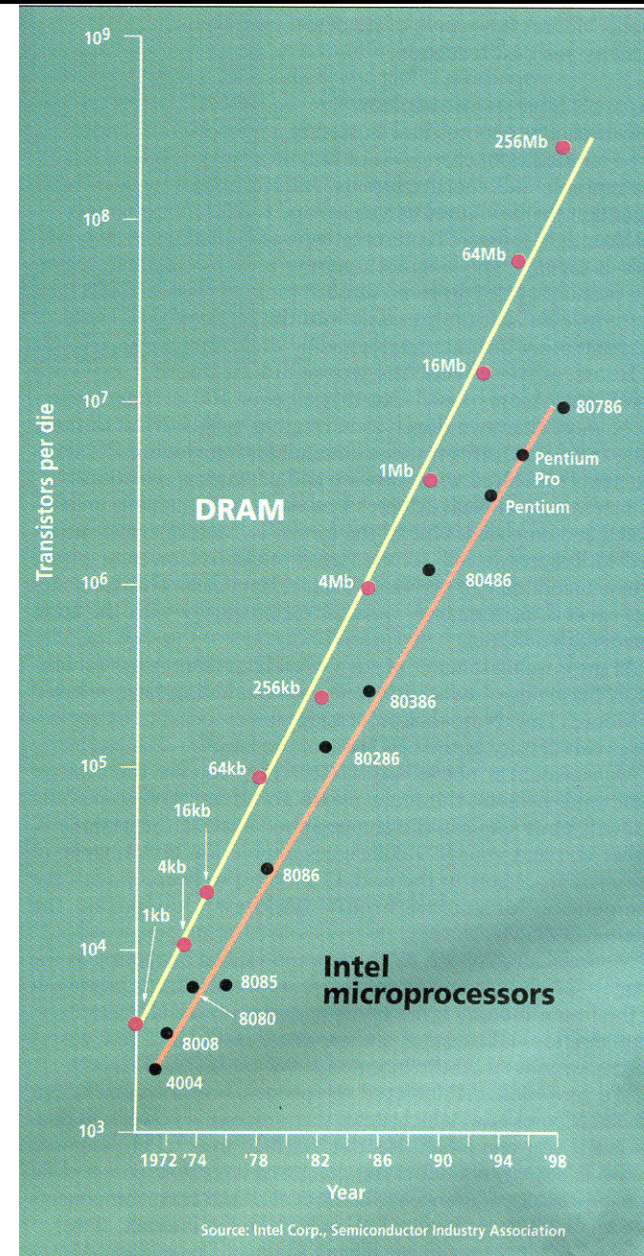
Moore's Law (original)



Gordon Moore, Intel
Electronics, April 19, 1965

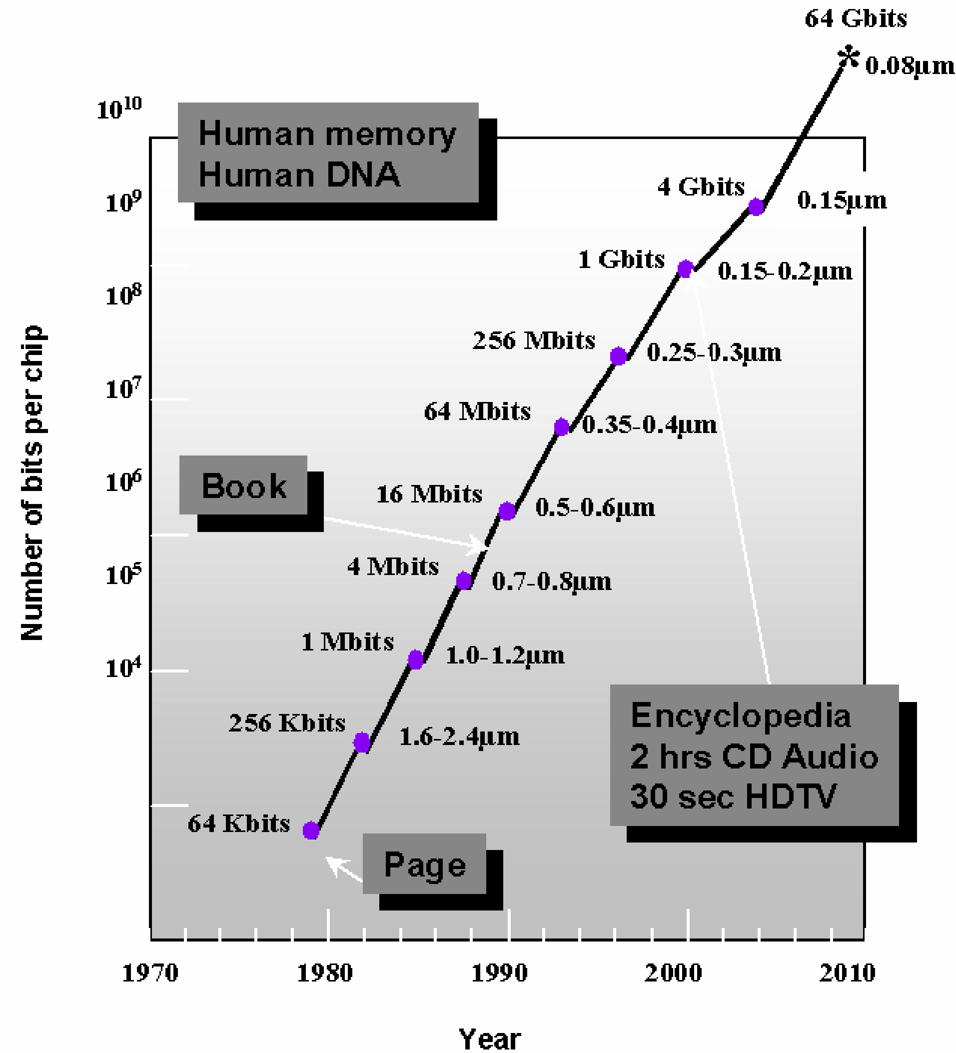
Moore's Law (revisited)

ICs complexity
doubles every 18 months



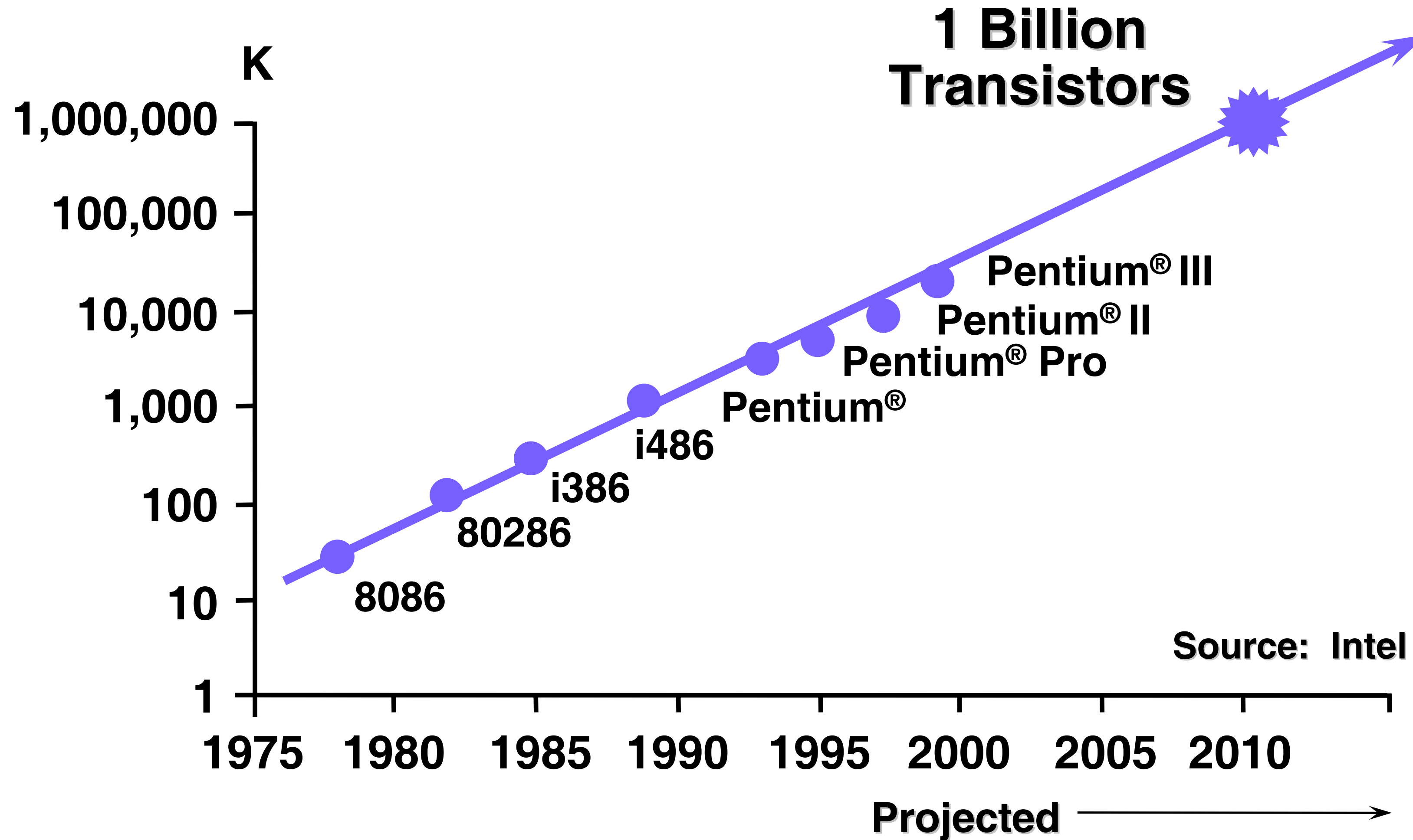
IEEE Spectrum, June 1997

Complexity evolution



Digital Integrated Circuits. A Design Perspective. J. M. Rabaey, A. Chandrakasan, B. Nikolic

Number of transistors in processors



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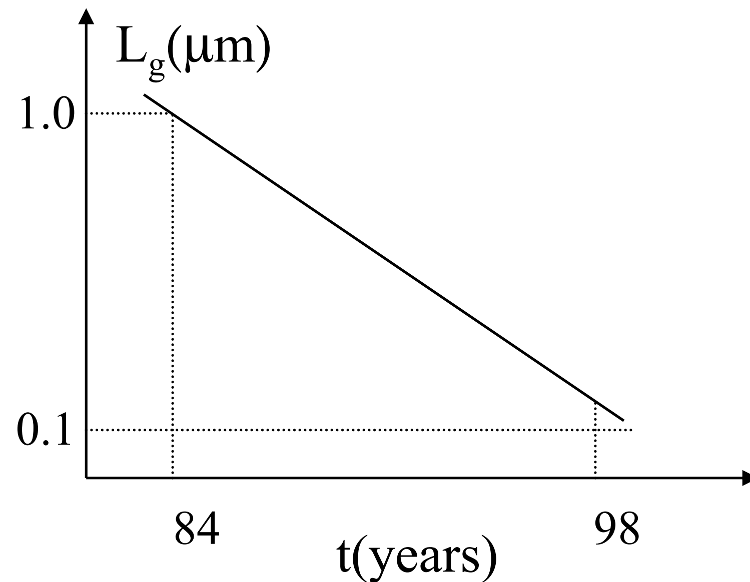
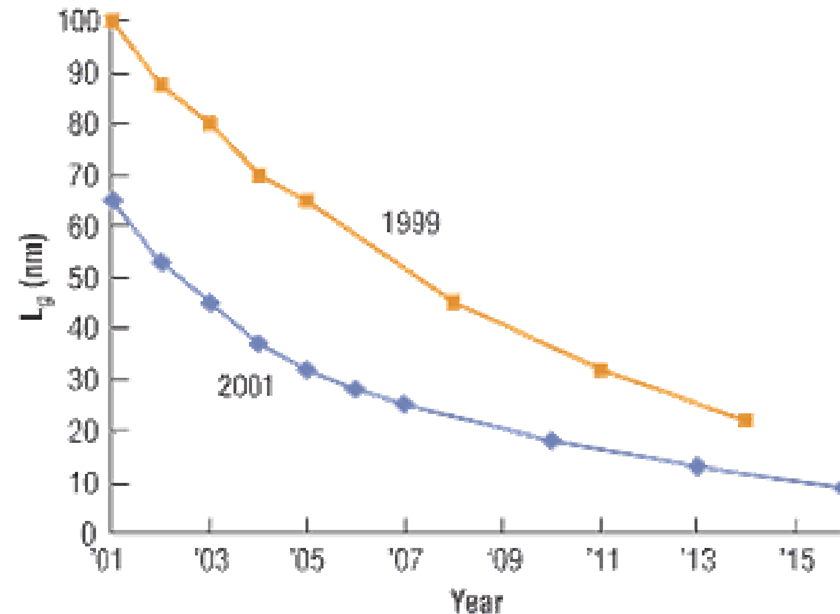
Minimum feature reduction

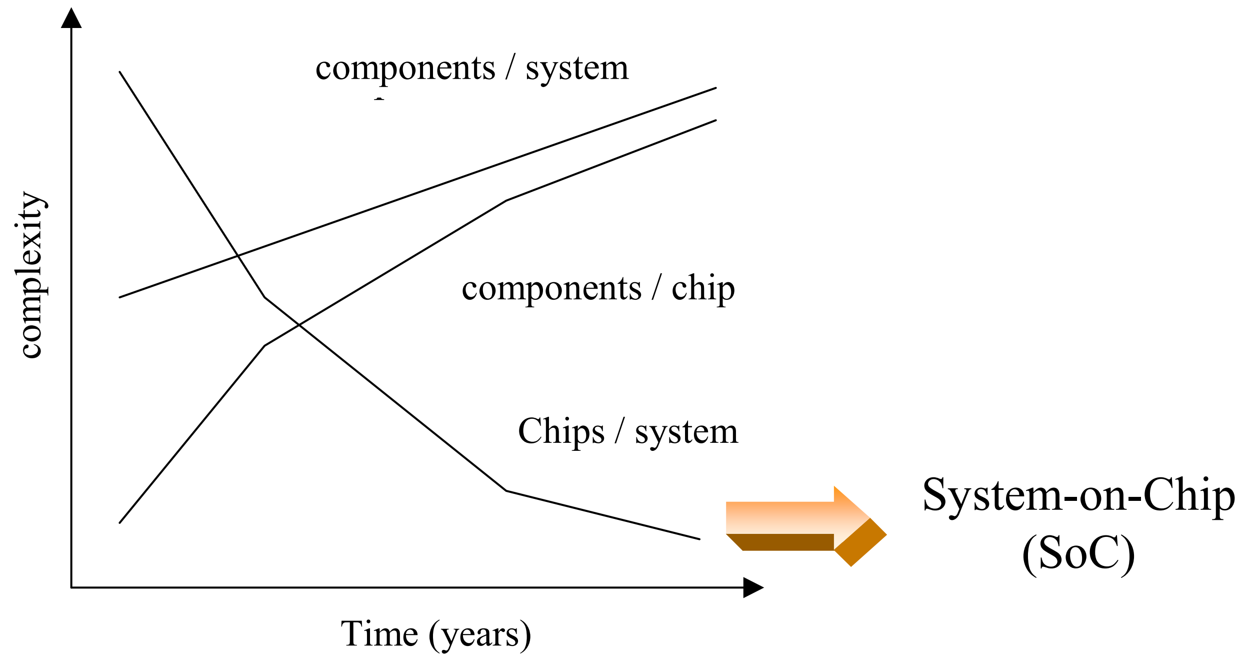




Future IC fabrication rests on solutions to circuit and device scaling. Solid State Technology July, 2002

Based on the biannual report of the Semiconductor Industry Association (SIA), International Technology Roadmap for Semiconductors (ITRS) 2001 Edition, Austin, TX: International Sematech, 2001 (http://public.itrs.net).

Relationship between component number and chips per system



Silicon limits (1998)

1. Technology limitations

- Minimum feature size: ~ 0.1 μm
- Maximum chip dimensions (*yield*): ~ 10 cm^2
- Gate delay: ~ 10 ps
- Maximum oxide electric field (MOS): ~ 5 10^8 V/m

2. Design limitations

- Sub-threshold current
- Interconnect line length
- Fan-out
- Clock distribution
- Power dissipation

3. Economical limitations

- Manufacturing line cost
- Power-speed tradeoff

Table 2. MOSFET Technology Projection: High Speed Scenario

Minimum feature size (μm)	0.5	0.35	0.25	0.18	0.13	0.09
Year of introduction	1992	1995	1998	2001	2004	2007
SRAM density	4Mb	16Mb	64Mb	256Mb	1Gb	4Gb
V_{cc}(V) (+10% for max V_{cc})	5	3.3	3.3	3.3	2.2	2.2
MOSFET gate oxide (nm)	15	9	8	7	4.5	4
Junction depth (μm)	0.15	0.15	0.1	0.08	0.08	0.07
NMOS I_{dsat} @ V_{gs} = V_{cc} (mA/μm)	0.56	0.48	0.55	0.65	0.51	0.62
PMOS I_{dsat} @ V_{gs} = V_{cc} (mA/μm)	0.27	0.22	0.26	0.32	0.24	0.32

Table 3. MOSFET Technology Projection: Low Power Scenario

Minimum feature size (μm)	0.5	0.35	0.25	0.18	0.13	0.09
V_{cc}(V) (+10% for max v_{cc})	3.3	2.2	2.2	1.5	1.5	1.5
MOSFET gate oxide (nm)	12	7	6	4.5	4	4
NMOS I_{dsat} @ V_{gs} = V_{cc} (mA/μm)	0.35	0.27	0.31	0.21	0.29	0.33
PMOS I_{dsat} @ V_{gs} = V_{cc} (mA/μm)	0.16	0.11	0.14	0.09	0.13	0.16

Silicon limits (2000)

Table. Transistor Requirements for Logic

Year of Introduction "Technology Node"	2001	2002 "130 nm"	2003	2004	2005 "100 nm"
Equivalent physical oxide thickness T_{ox} (nm)	1.5-1.9	1.5-1.9	1.5-1.9	1.2-1.5	1.0-1.5
Sidewall spacer thickness (nm) extension structure	59-108	52–104	48-96	44-88	40-80
Sidewall spacer thickness control (nm, 3σ)	≤ 10%	≤ 10%	≤ 10%	≤ 10%	≤ 10%
Gate electrode thickness	100	85	80	70	65
Active poly doping to achieve 10% GOx depletion	3.1E+20	3.1E+20	3.1E+20	3.9E+20	4.6E+20
Silicide thickness (nm)	40	34	32	28	25
Contact Xj (nm)	55-105	45-90	43-85	38-75	35-70
Drain extension Xj (nm)	30-50	25-43	24-40	20-35	20-33
Lateral abruptness for source extension (nm/decade)	3.4	2.9	2.7	2.4	2.2
Extension lateral abruptness (nm/decade)	10	8.5	8	7	6.5

Solutions being pursued (yellow) No known solution (red)

(Note: Adapted from Table 22a of the 1999 International Technology Roadmap for Semiconductors)

Semiconductor International
March 2000, p. 70

Table 1. nMOSFET parameters extrapolated from the *1999 ITRS Roadmap*

Year in production	2005	2008	2011	2014
DRAM gate length (nm)	100	70	50	35
MPU gate length (nm)	65	45	32	22
Max. X_jSD(nm)	100	70	50	35
S/D ext. X_j nom. (μm)	0.025–0.04	0.02–0.028	0.013–0.02	0.01–0.013
T_{ox} equivalent (nm)	1.0–1.5	0.8–1.2	0.6–0.8	0.5–0.6
V_T 3σ variation (±mV)	33	25	17	17
V_{suppl} (V)	0.9–1.2	0.6–0.9	0.5–0.6	0.3–0.6
N_{ave} ($\times 10^{18}$cm^{-3})	1.2	2.5	4	6
$N_{carriers}$ in channel	600	350	180	90
Nominal I_{on} at 25°C (μA/μm) NMOS/PMOS high performance	750/350	750/350	750/350	750/350
W_{depl} (nm)	29	20	16	13
$N_{impurities}$ ($L = W_{min}$) dense lines, MPU	239–348	150–239	96–150	55–96

Solid-State Technology
March 2000, p. S14

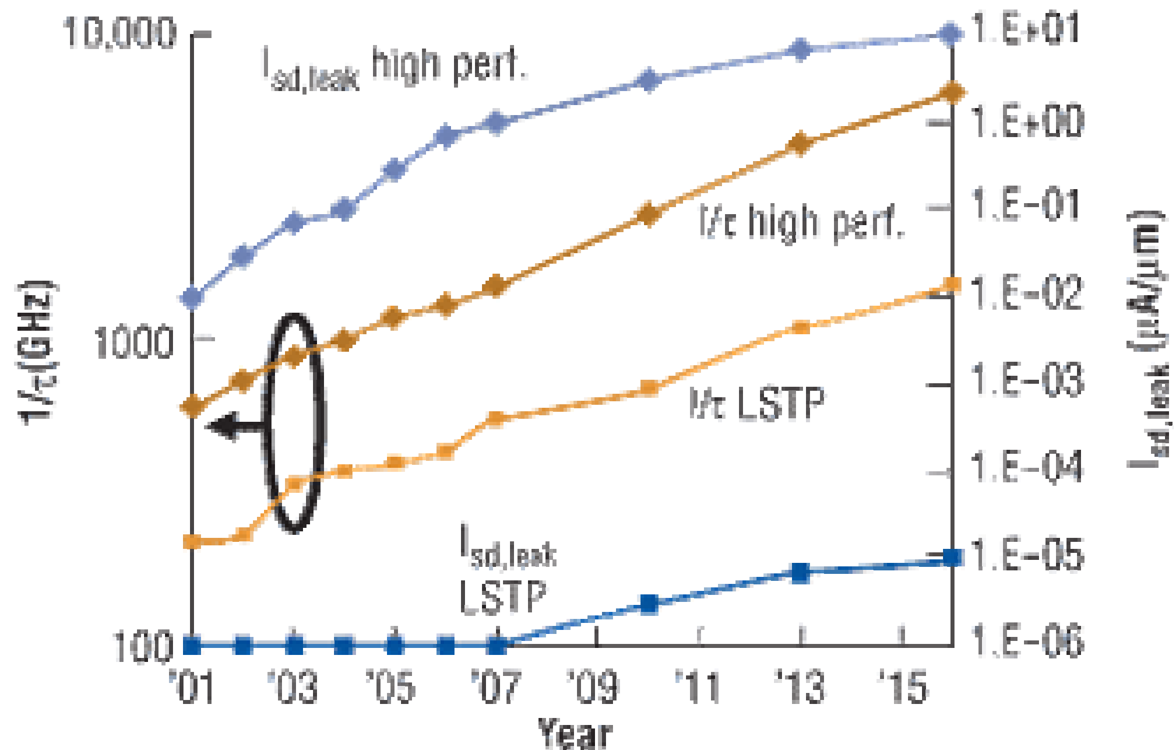
Silicon limits (2002)

Table 1. High-Performance Logic Technology Requirements

Year of production	2001	2002	2003	2004	2005	2006	2007
Technology node (nm)	130			90			65
Physical gate length (nm)	65	53	45	37	32	28	25
Equivalent oxide thickness (EOT) (nm)	1.3-1.6	1.2-1.5	1.1-1.6	0.9-1.4	0.8-1.3	0.7-1.2	0.6-1.1
Gate depletion and quantum effects electrical thickness adjustment (nm)	0.8	0.8	0.8	0.8	0.8	0.8	0.5
T_{ox} electrical equivalent (nm)	2.3	2.1	2.0	2.0	1.9	1.9	1.4
Nominal power supply voltage (V_{dd})	1.2	1.1	1.0	1.0	0.9	0.9	0.7
Nominal high-perf. NMOS subthreshold current (@25°C) (µA/µm)	0.01	0.03	0.07	0.1	0.3	0.7	1
Nominal high-perf. NMOS saturation current drive (I_{dd}) (@V_{dd}, @25°C) (µA/µm)	900	900	900	900	900	900	900

Fabricating 90 nm Devices by 2004
Semiconductor International, 1/1/2002

Silicon limits (2002)



Future IC fabrication rests on solutions to circuit and device scaling. Solid State Technology July, 2002.

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Silicon limits (2002)

Minimum transistor (prototype):

Silicon bulk planar transistor
Gate length:

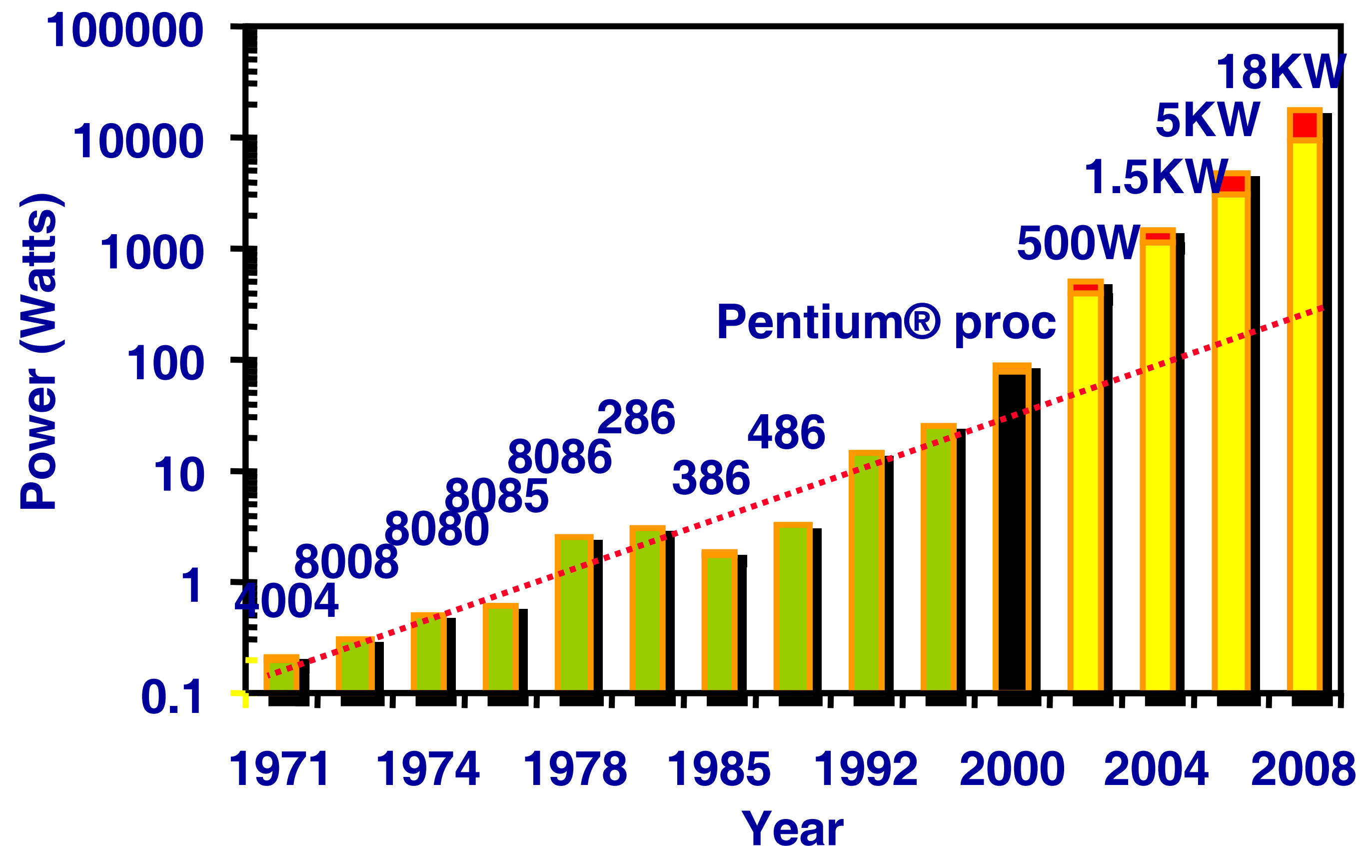
15 nm

This guarantees 4 new generations

- Reduction factor for one generation : 0,7
- Area reduction factor : 0,5

CMOS needed, still viable
Solid State Technology February, 2002
Report on:
2001 IEEE International Electron Devices Meeting (IEDM), Dec. 2001.

Power reduction extrapolation



Digital Integrated Circuits. A Design Perspective. J. M. Rabaey, A. Chandrakasan, B. Nikolic

Reducing power

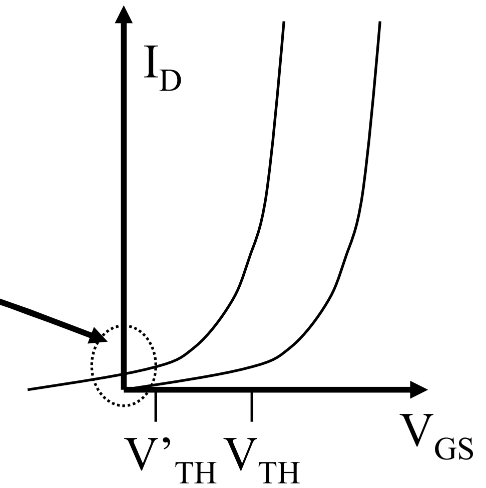
- Integration increase
- Portable applications

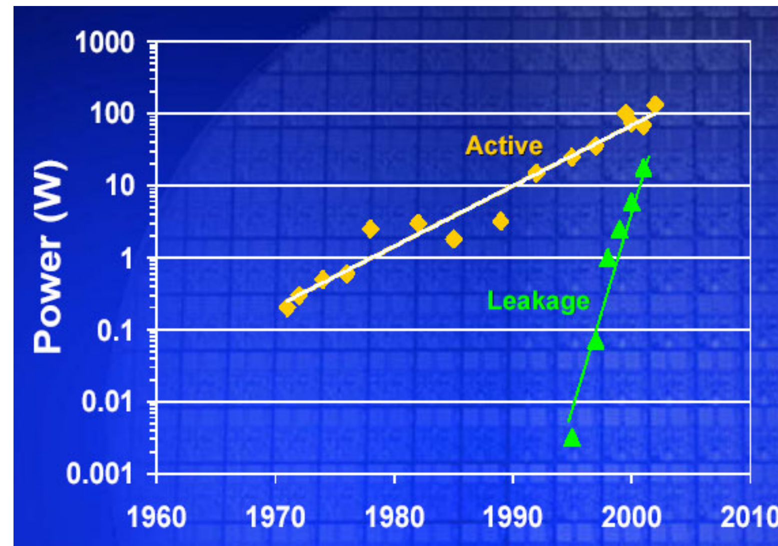
Insulator breakdown electric field ⇨ V_{DD} ↓ (3.3 V ⇦ 2.2 V ⇦ 1.5 V ⇦ 1 V...)

Example: for 5 V: t_{ox} > 10 nm,

for 3.3 V: t_{ox} > 6.6 nm

- V_{DD} ↓ ⇨ V_{TH} ↓ ⇨ **Current threshold ↑**

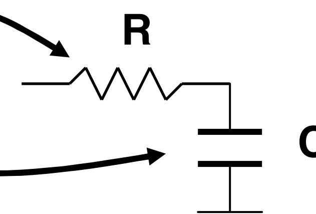




Technological improvements

- SOI (*Silicon On Insulator*): bulk parasitic current elimination

- **Cu** interconnects : Reduction of parasitic resistance
- Low-k insulator: Reduction of parasitic capacitance



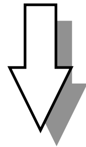
Signal integrity

- Line coupling
- Suitable V_{DD} and V_{SS} levels
- Automatic tools
  - Driver strength
  - Receiver noise immunity
  - Parasitics
- *Victims* and *aggressors* detection
- Applied solutions
  - Buffer dimensioning
  - Line separation
  - Shielding

1.3 Design techniques

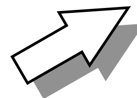
Design techniques' evolution

Exponential increase of integration capability



Designer productivity increase (#TRT/day)

Solution: Rise the abstraction level



Current methodology: HDLs (Hardware Description Languages)

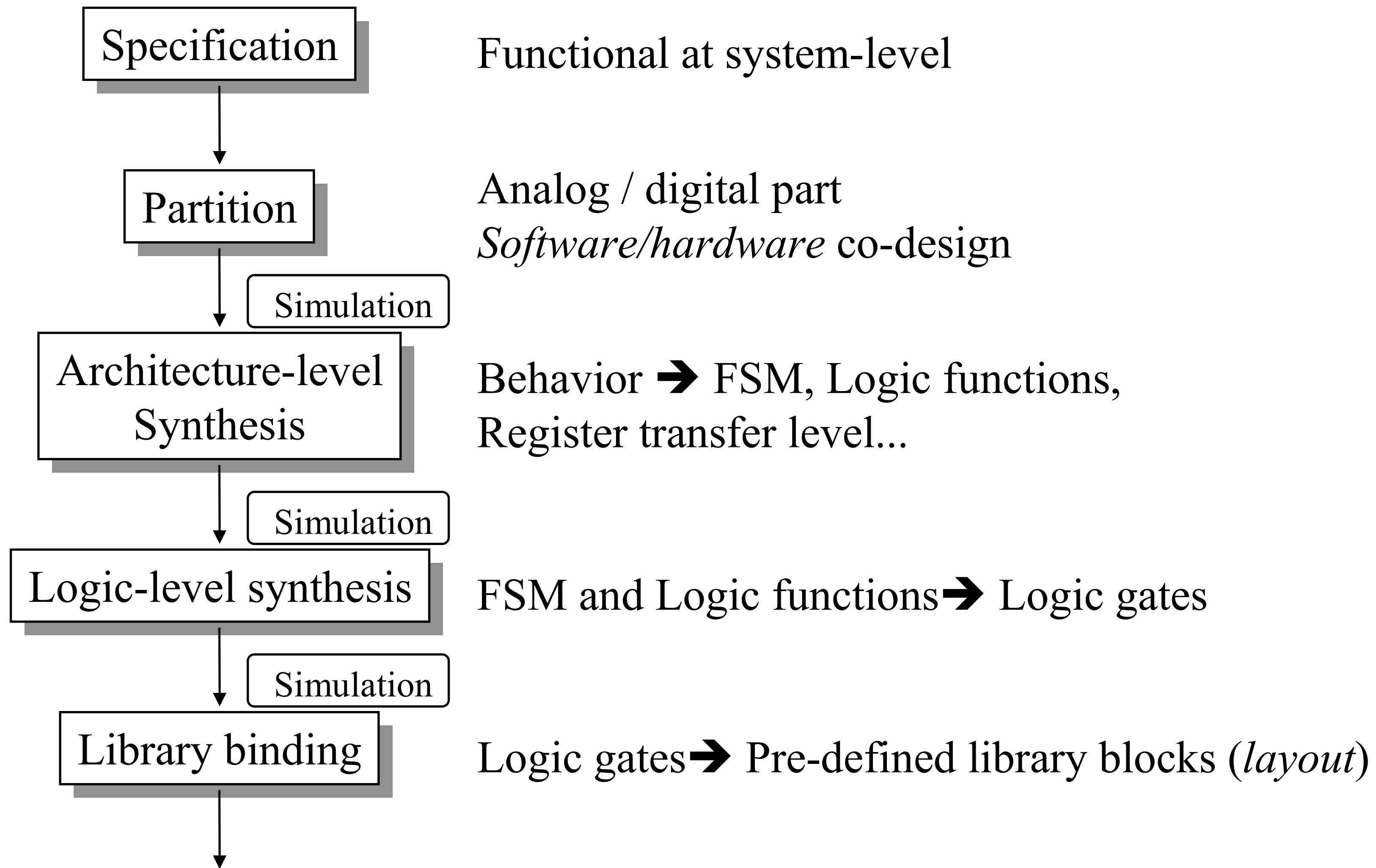
- Documentation
- Portability
- Description at several abstraction levels (hierarchy)
- Behavioral (functional) and structural description
- Simulation
- Synthesis
- *Retargetting* (rapid prototyping)

The most common languages are **VHDL** and **Verilog**

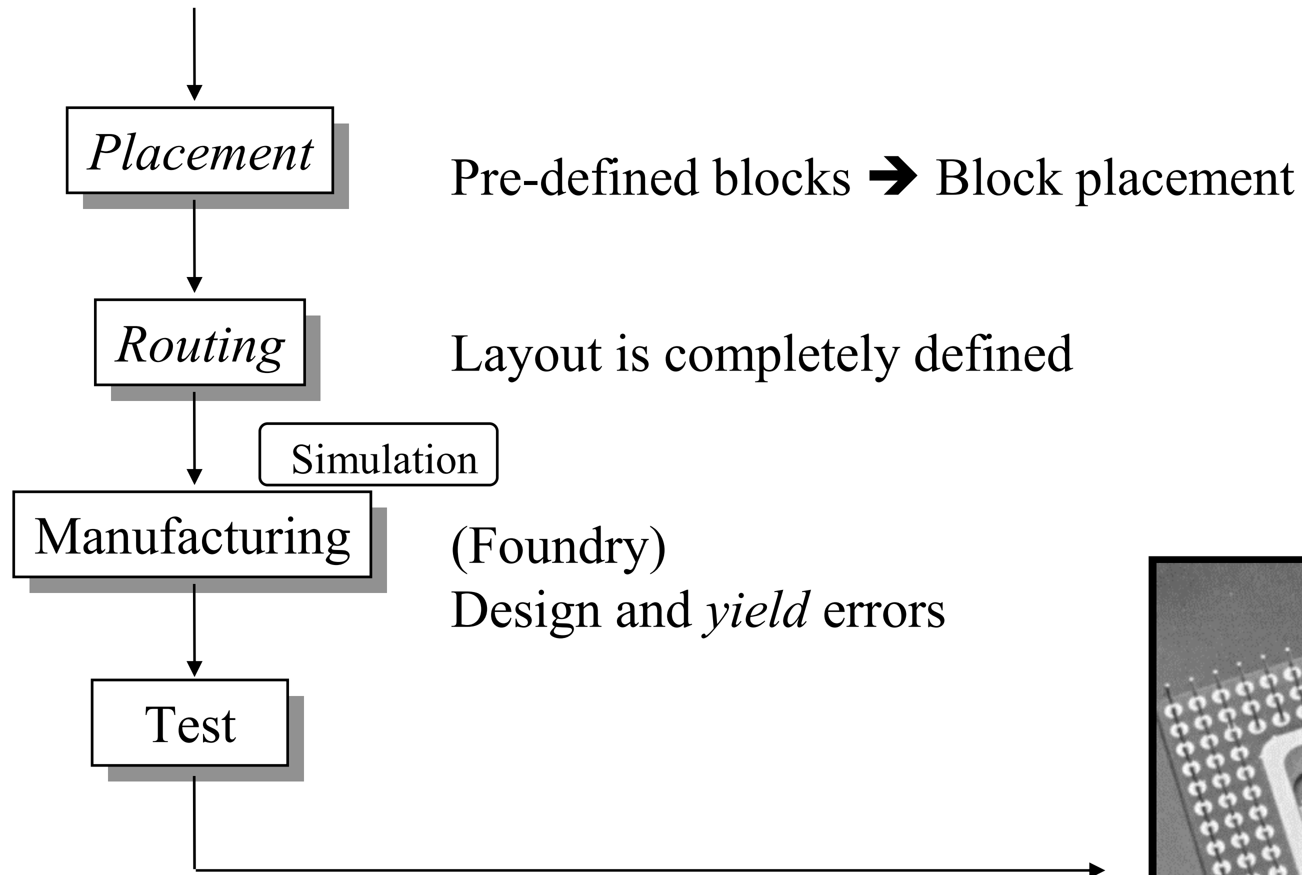
New trends

- *Hardware/software co-design*
- High-level design environments (SystemVerilog, SystemC)
- IP (*Intellectual Property*) *cores* usage

Design process (1)



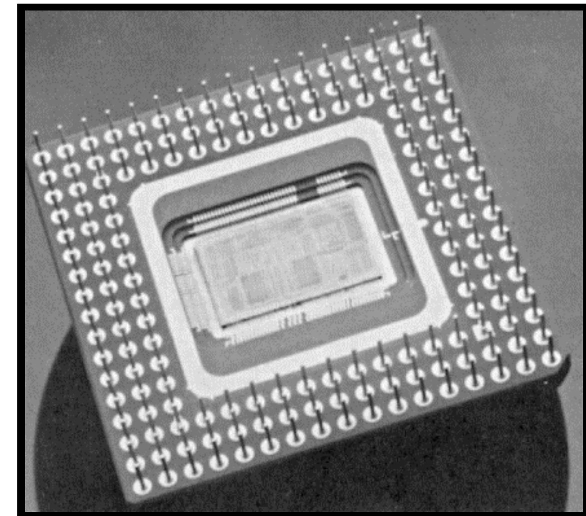
Design process (2)



Pre-defined blocks ➔ Block placement

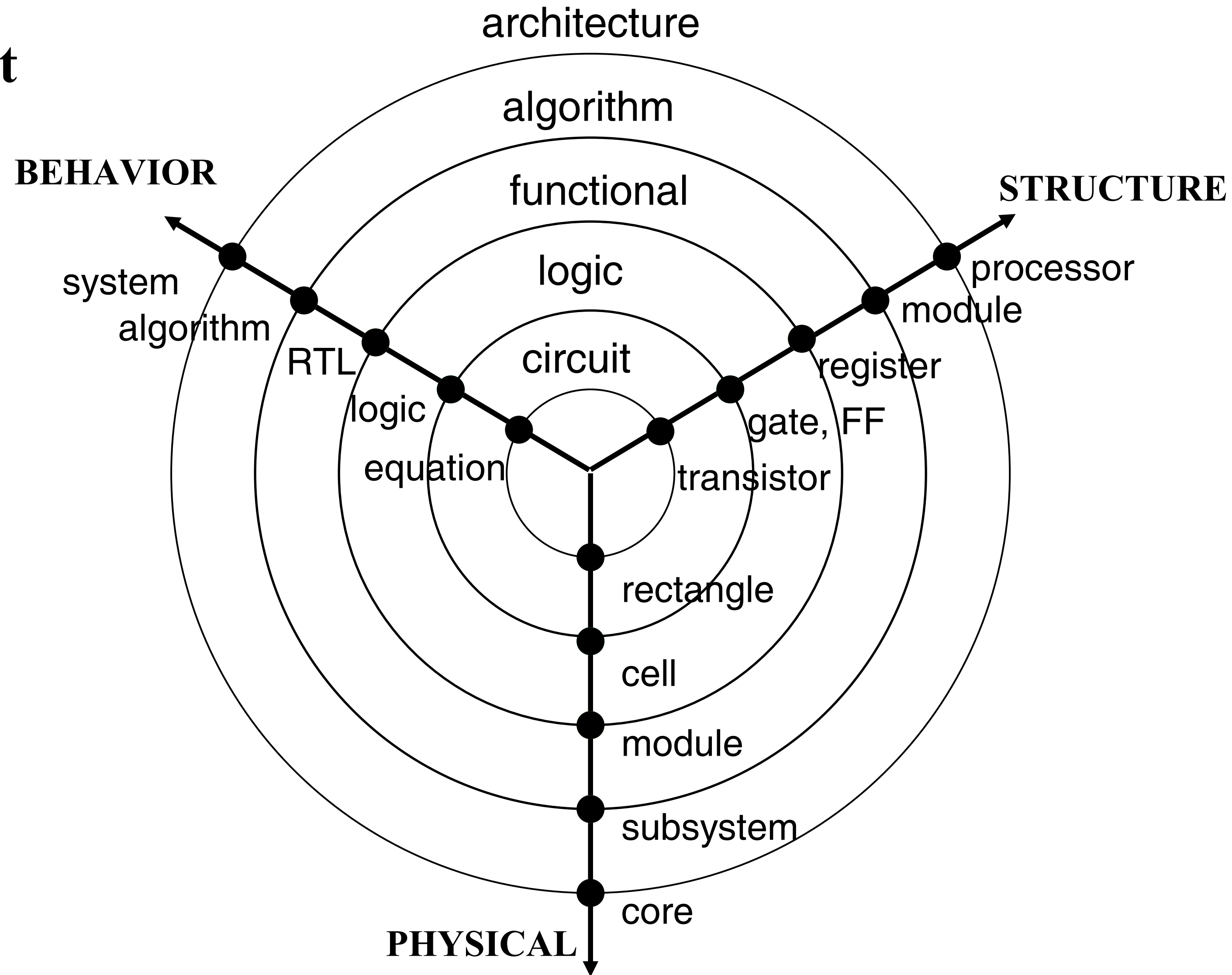
Layout is completely defined

(Foundry)
Design and *yield* errors

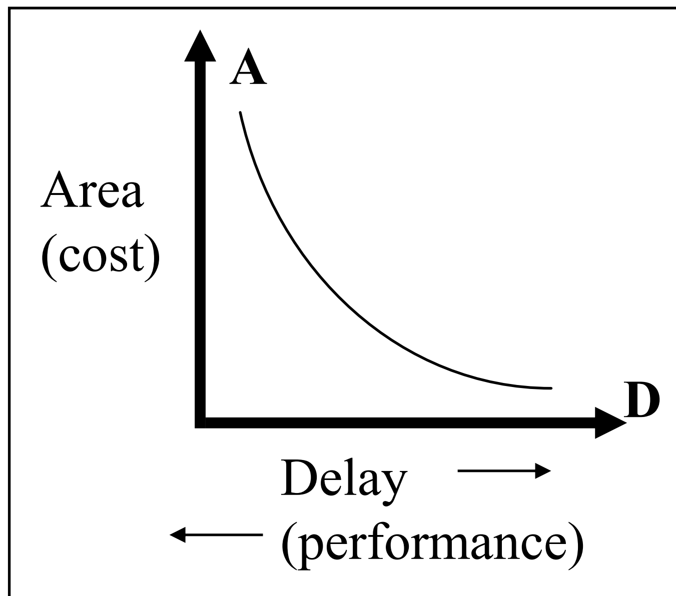


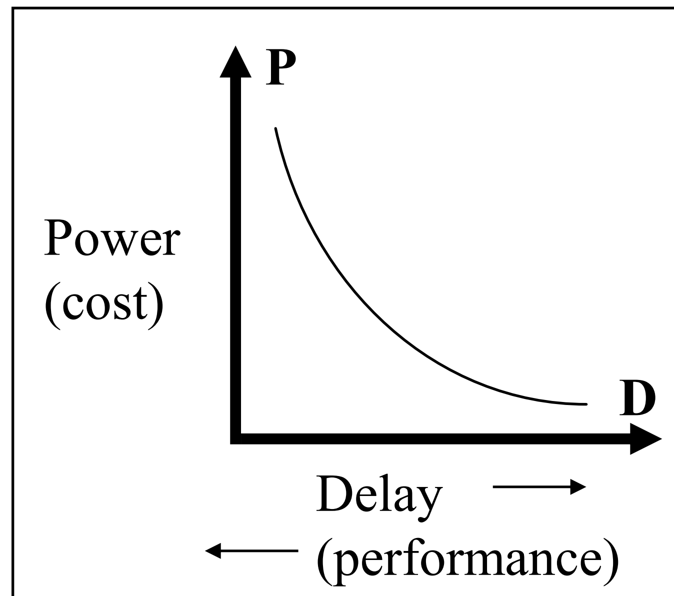
Digital design domains and abstraction levels

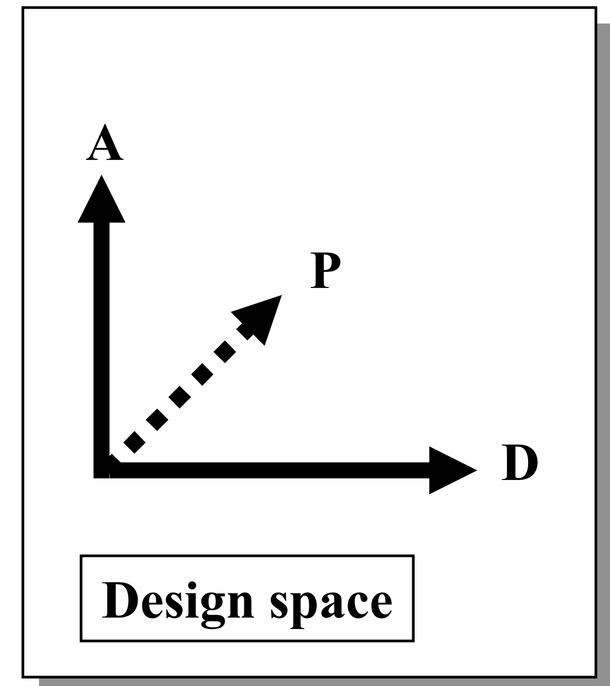
- **Y-chart**



Cost-Performance tradeoff: Design space







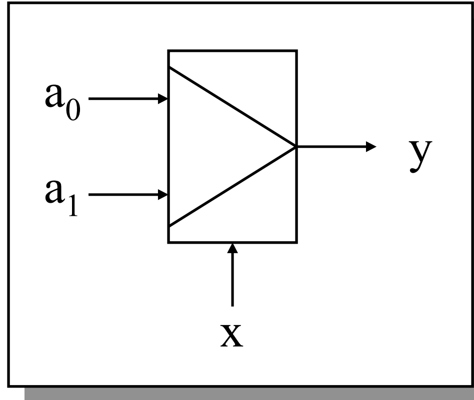
Description levels

```
mux: process(x,a0,a1)
      if x = '0' then y <= a0;
      elsif x = '1' then y <= a1;
      else y <= 'Z';
      end if;
end process mux;
```

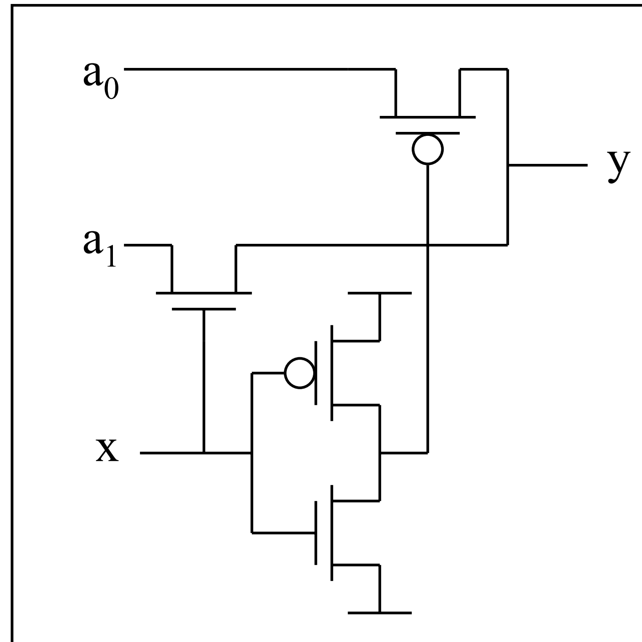
Behavioral HDL

```
mux1: mux
      port map(
      in0 => a0, in1 => a1,
      ctl => x, out => y);
```

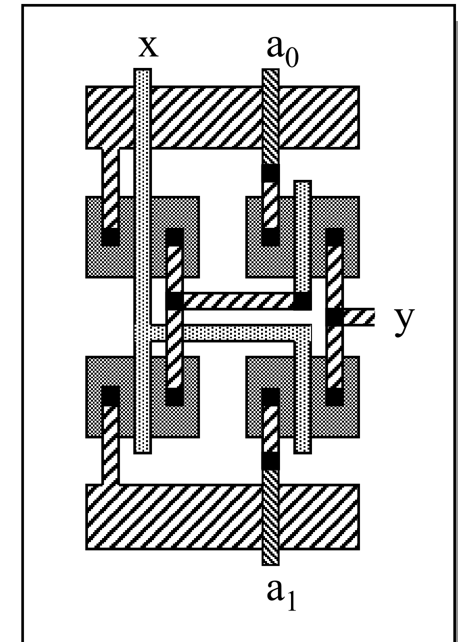
Structural HDL



Logic level



Electric level



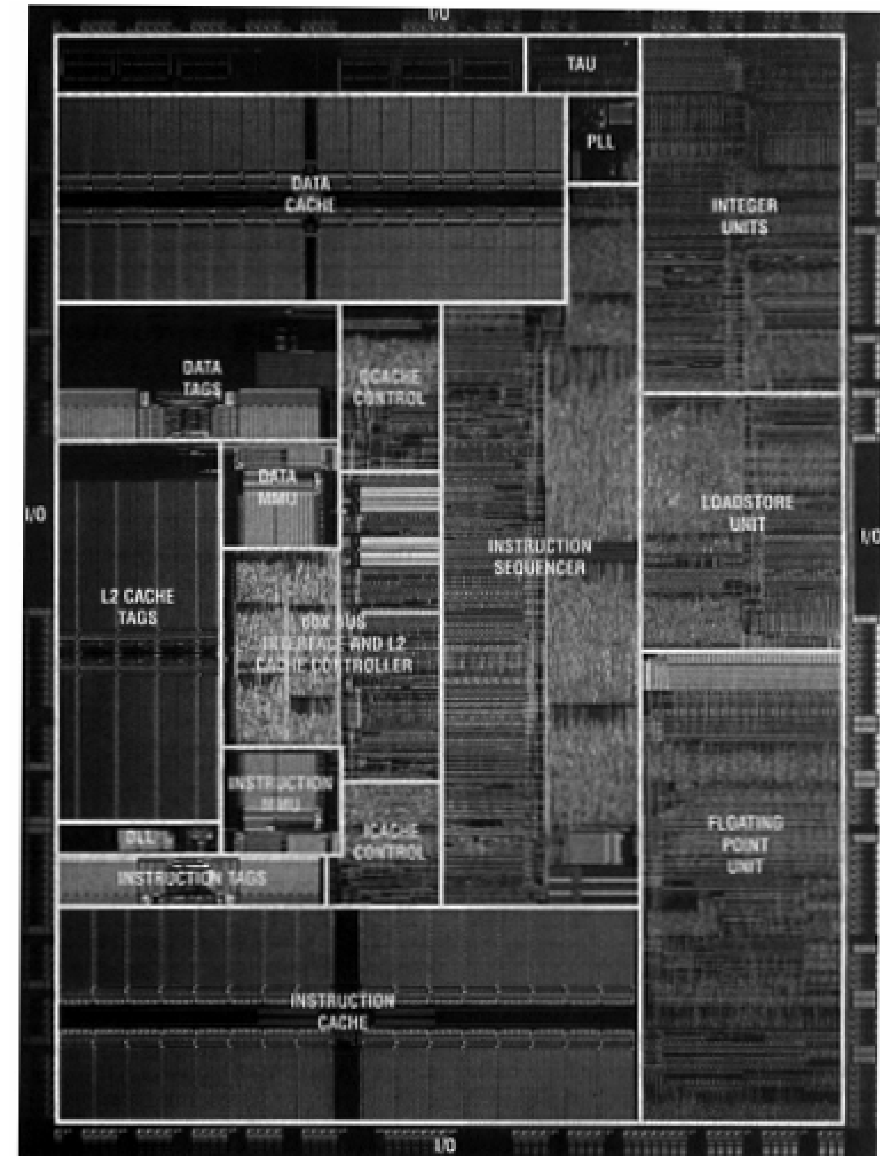
Layout level

1.4 State of the art

32-bit RISC Microprocessor (PowerPC)

Features

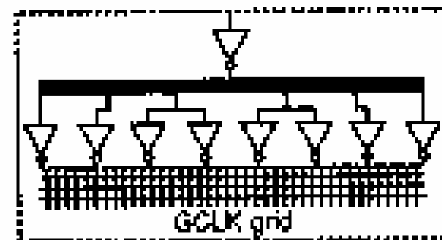
Technology	0.2 µm
V_{DD}	1.8 V
V_{DD} d'E/S	3.3 V
Metal material	Cu
Metal levels	6
Frequency	450 MHz
Power	3 W @ 400 MHz
Die area	40 mm^2

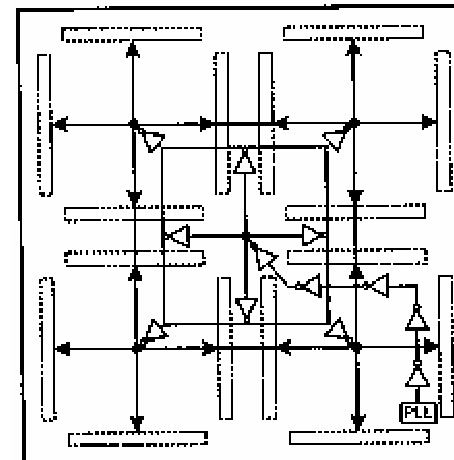


IEEE Journal of Solid-State Circuits, Nov. 1998, pp. 1609-1616

DEC Alpha Microprocessor (ISSCC 1997)

- 64-bit RISC (Reduced Instruction Set Computer)
- 0.35 µm 6-metal CMOS technology
- 600 MHz
- 15.2 Mtransistors
- 17 × 18.9 mm^2 = 3.2 cm^2
- 72 W @ V_{DD} = 2.2 V
- 587 pins (198 for V_{DD} and V_{SS})
- 64 kbyte on-chip cache
- 1 µF on-chip surface capacitor (to regulate V_{DD})
- Hierarchical clock distribution

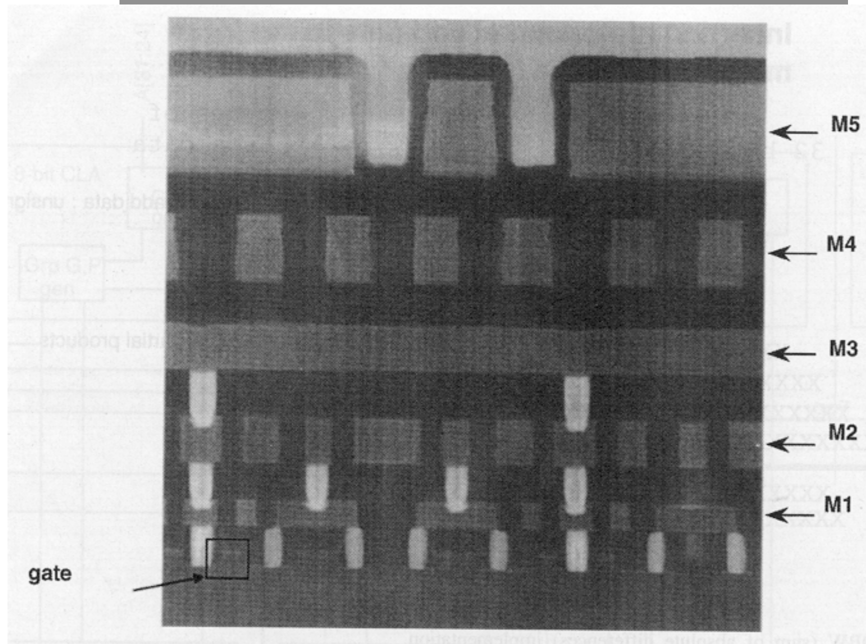


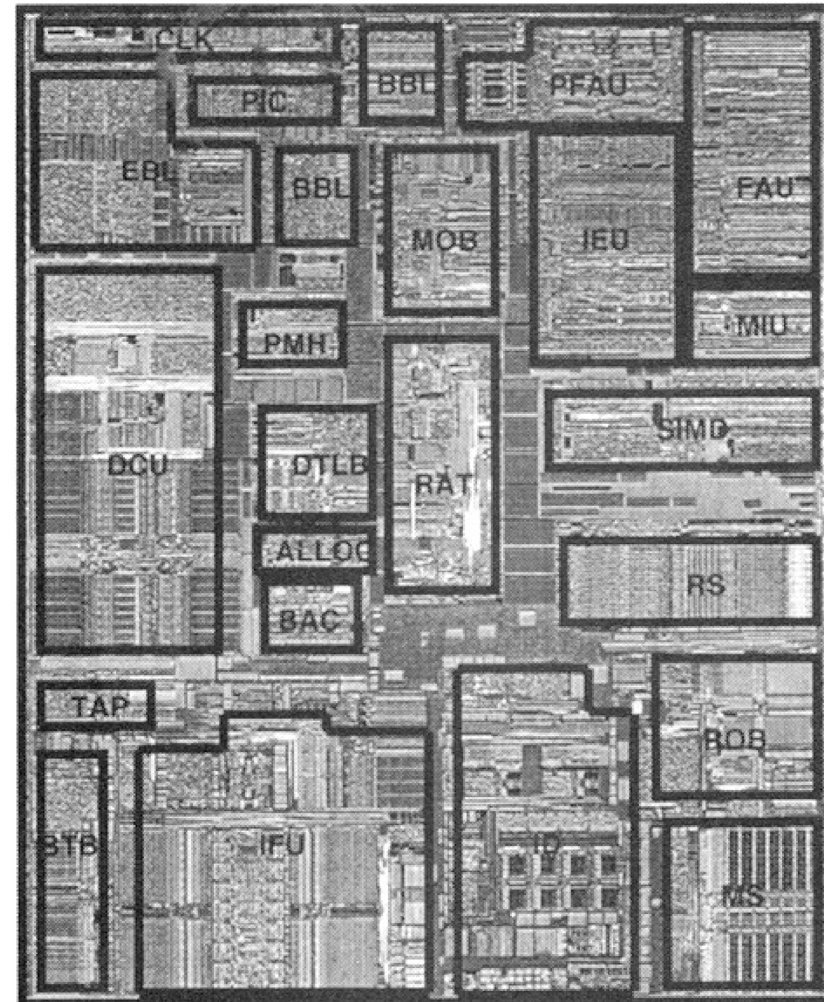


IEEE Journal of Solid-State Circuits, Nov. 1998, pp. 1627-1633

Microprocessor IA-32 (Intel, 1999)

Characteristics	
Technology	0.25 µm
V_{DD}	1.4 - 2.2 V
Metal levels	5
Frequency	650 MHz
Transistor count	9.5 M
Dimensions	123 mm^2

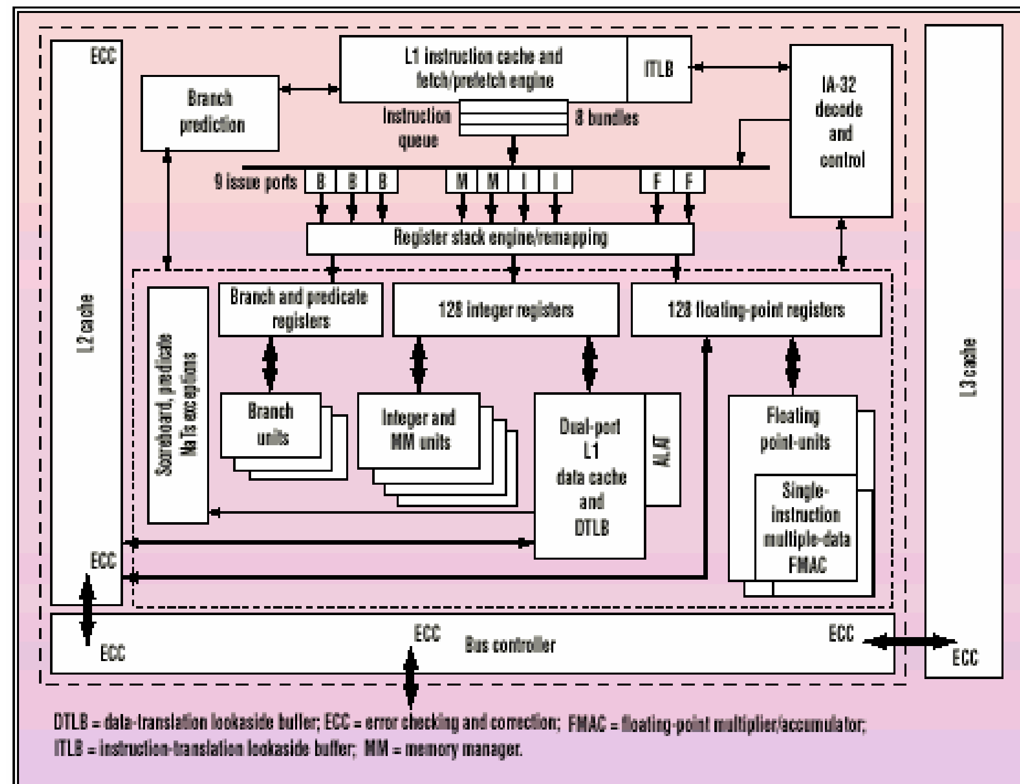




IEEE Journal of Solid-State Circuits, Nov. 1999, pp. 1454-1465

Microprocessador IA-64 (Intel, 2000)

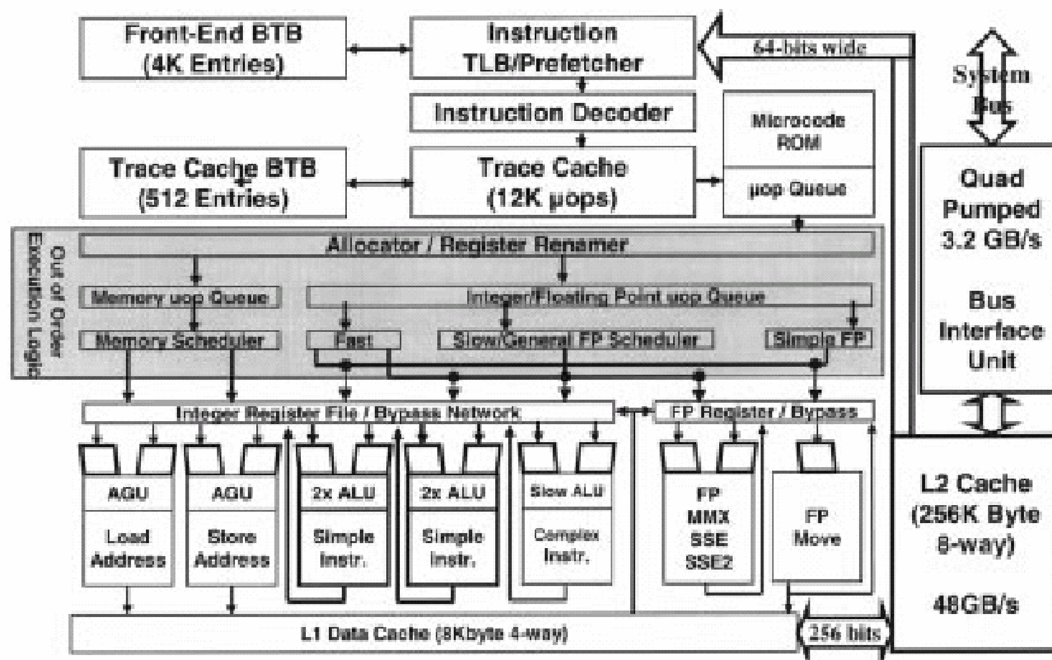
Characteristics	
Technology	0.18 µm
Metal levels	6
Frequency	800 MHz
Transistor count	25.4 M
Pin count	1012

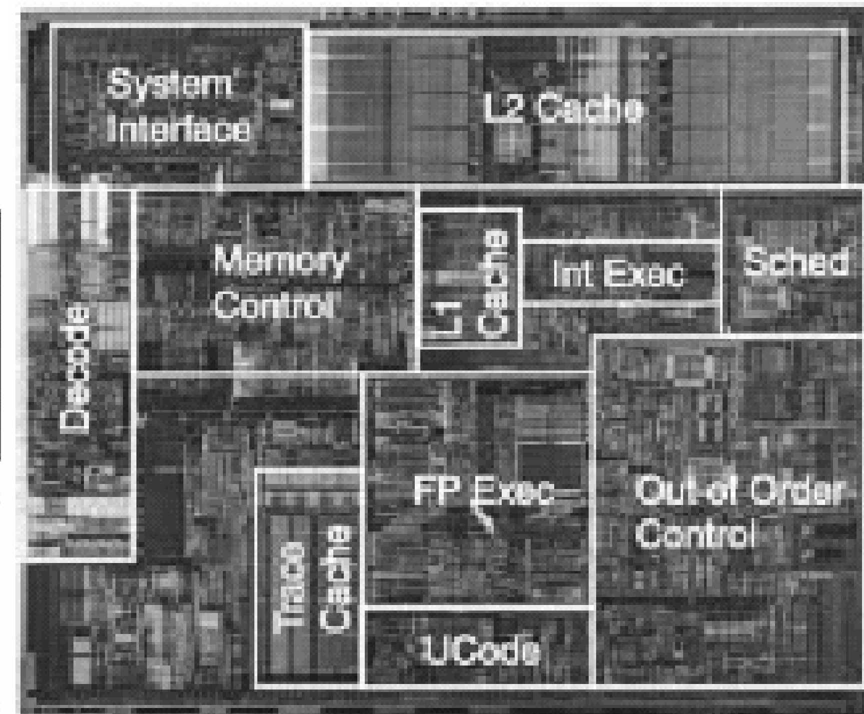


IEEE Journal of Solid-State Circuits, Nov. 2000, pp. 1539-1544

Microprocessor Pentium 4 (Intel, 2001) 1/2

- 42 Mtransistors
- 0.18-µm CMOS
- 6 aluminium levels
- Chip area: 217 mm^2
- Power: 55W @ 1500 MHz @ 1.75 V

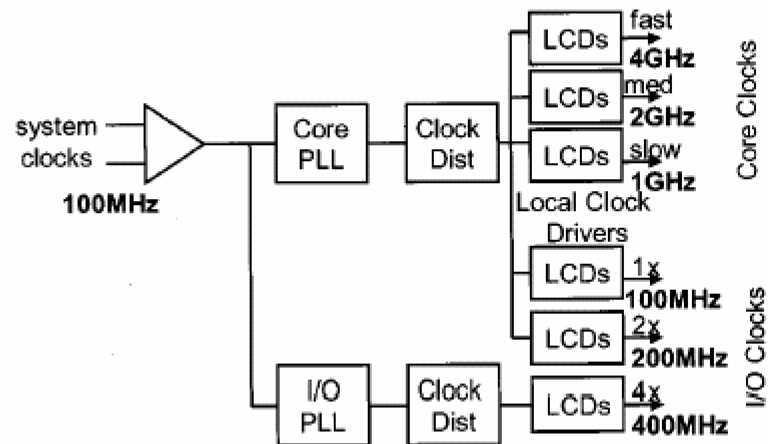


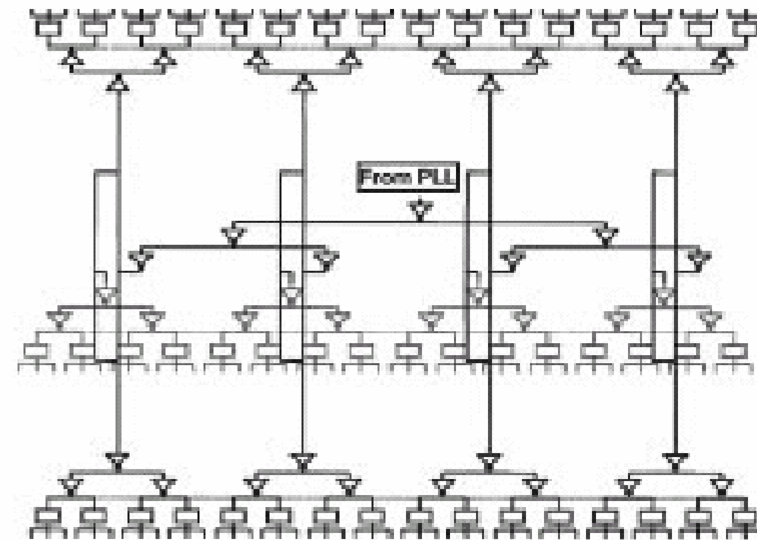


A 0.18-µm CMOS IA-32 Processor With a 4-GHz Integer Execution Unit
IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 36, NO. 11, NOVEMBER 2001

Microprocessor Pentium 4 (Intel, 2001) 2/2

Clock distribution (H-tree)

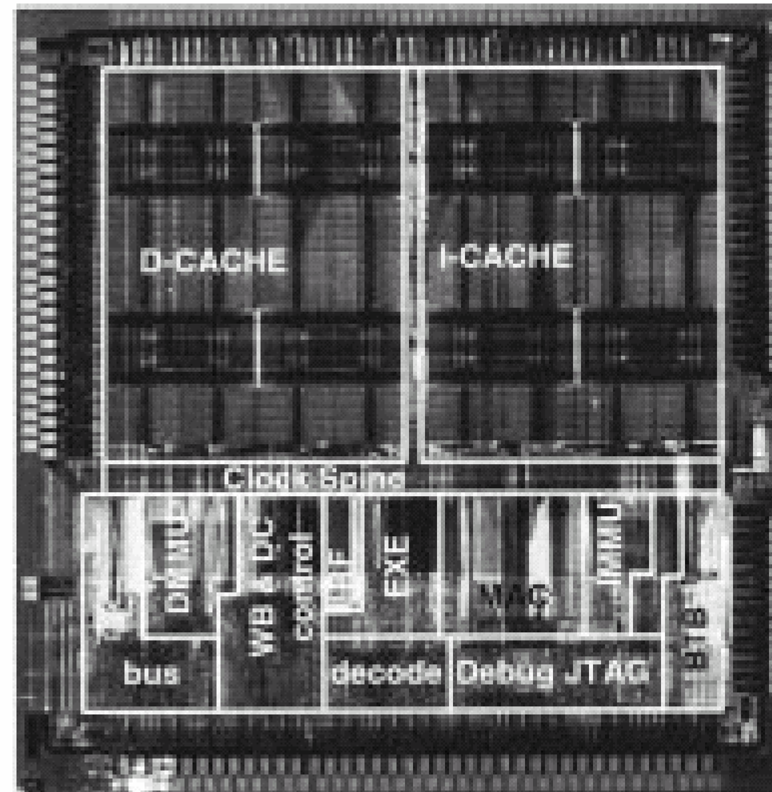




A Multigigahertz Clocking Scheme for the Pentium® 4 Microprocessor
IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 36, NO. 11, NOVEMBER 2001

RISC Microprocessor core (2001)

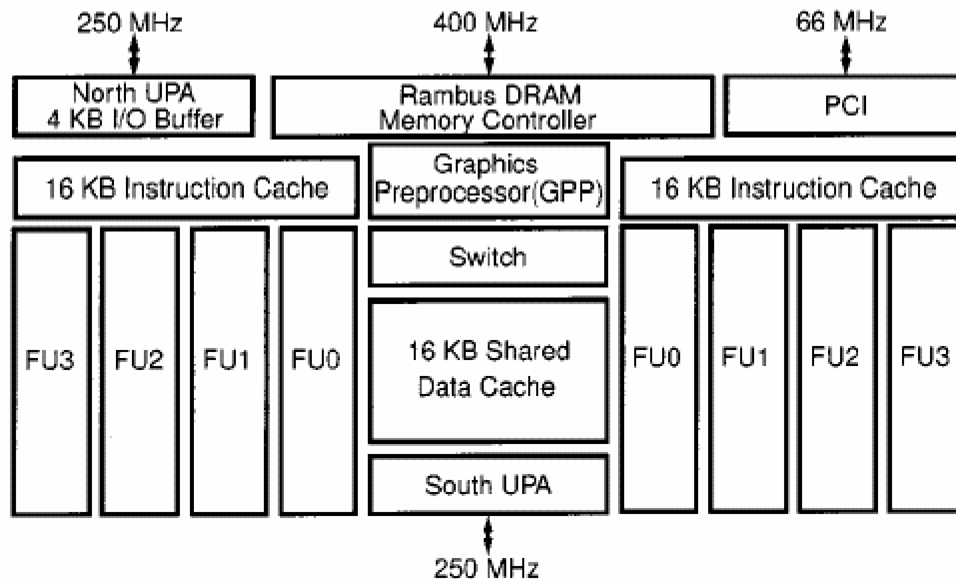
- Instruction set ARM™ V.5TE
- Custom logic
- 6-layer metal
- 0.18-μm CMOS process
- 16.77 mm²
- Range V_{DD} 0.75–1.65 V
- 55 mW @ 0.7 V, 200 MHz
- 900 mW @ 1.65 V, 800 MHz
- 4500 MIPS/W @ 0.75 V
- 850 MIPS/W @ 1.65 V



An Embedded 32-b Microprocessor Core for Low-Power and High-Performance Applications
IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 36, NO. 11, NOVEMBER 2001

Dual microprocessor MAJC (2001)

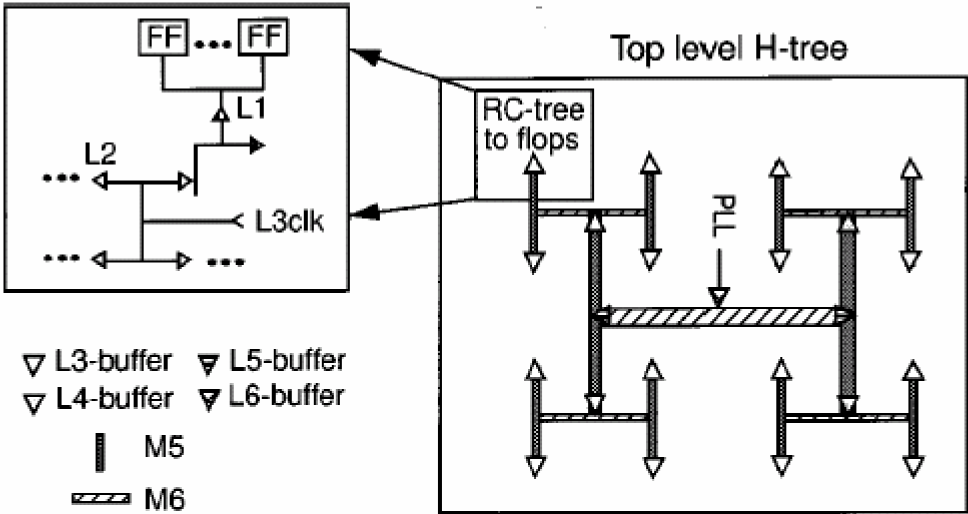
- 0,22 μm CMOS
- 6 levels Cu
- Leff 0,12/0,15 μm
- 12,9 Mtransistors
- 276 mm^2
- 624 pins (247 for supply)
- 18 W @ 500 MHz @ 1,8 V



The First MAJC Microprocessor: A Dual CPU System-on-a-Chip

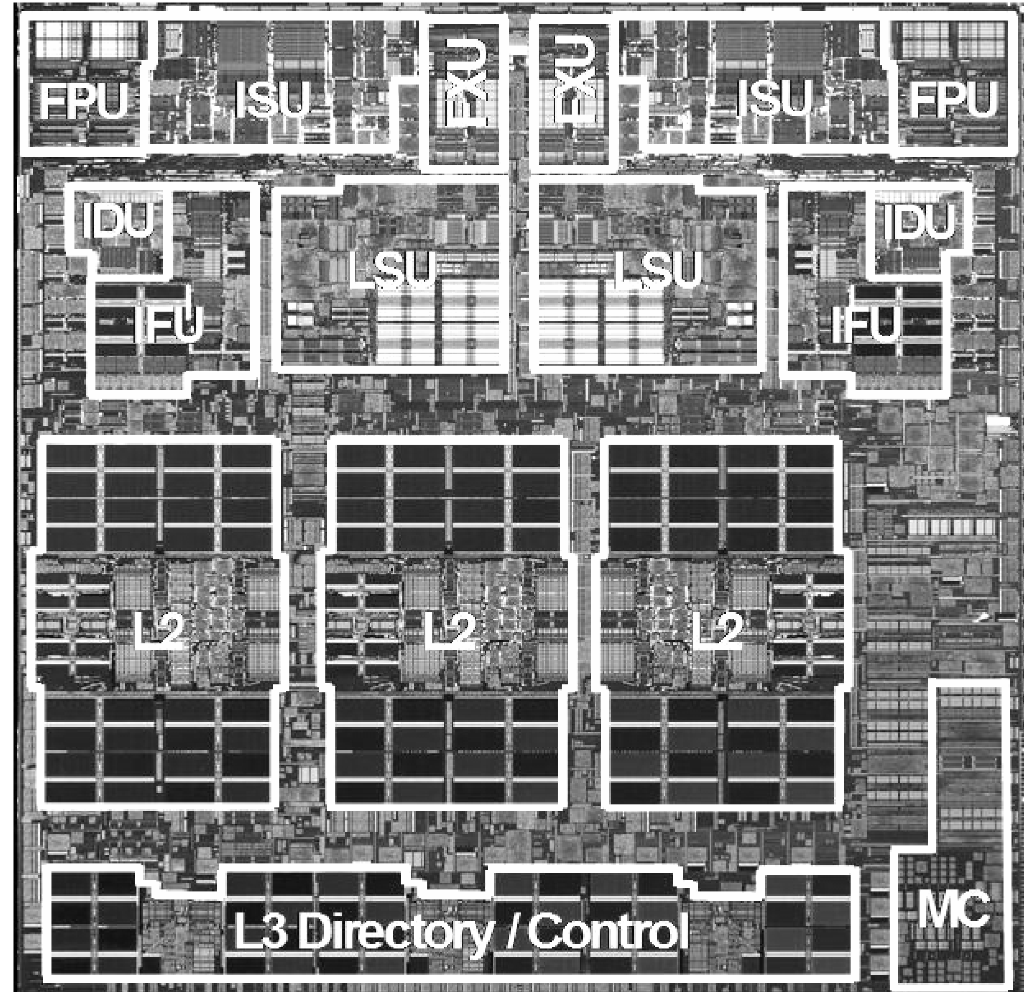
IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 36, NO. 11, NOVEMBER 2001 1609

Clock distribution (H-tree)



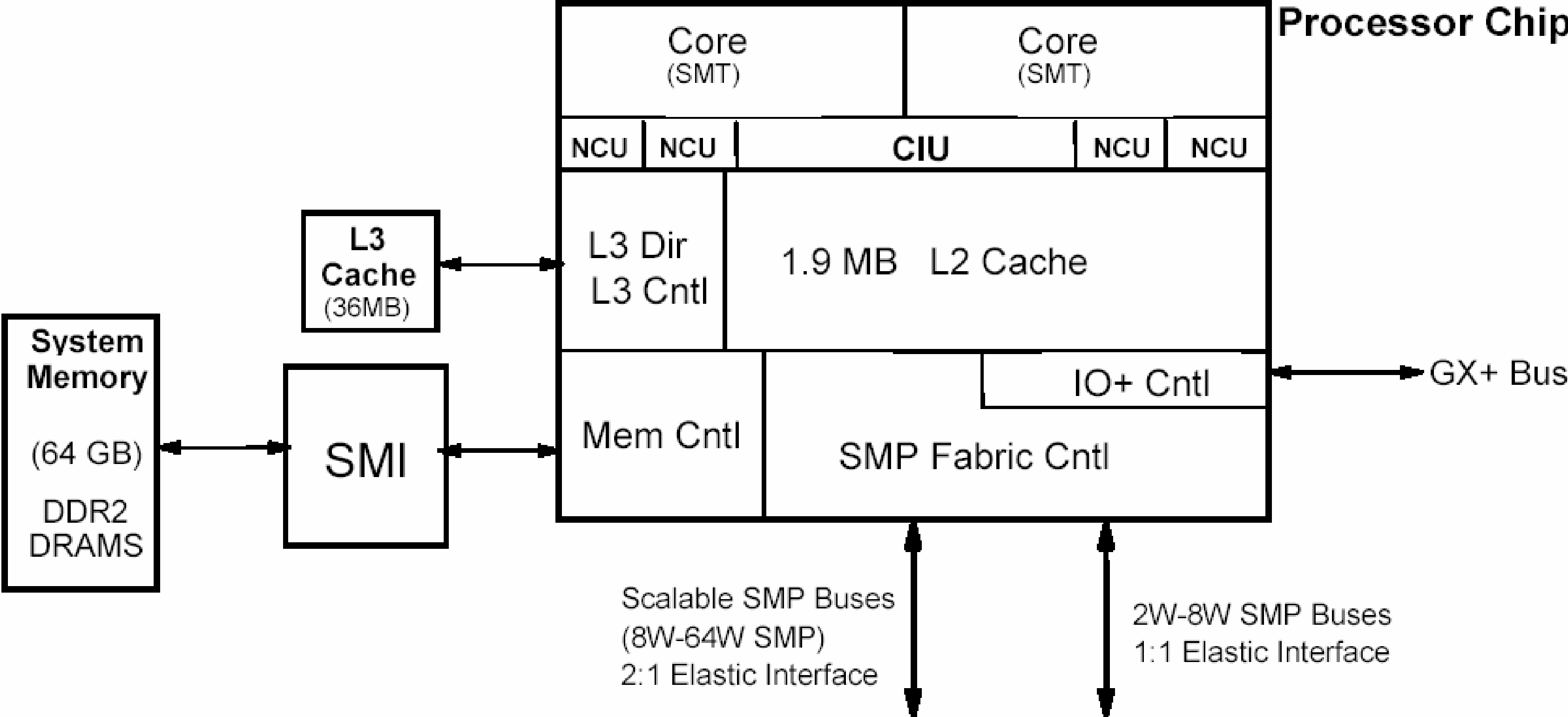
Microprocessor POWER5 (2004)

- 130 nm SOI
- 8 levels Cu
- low-k dielectric
- 276 Mtransistors
- 389 mm^2
- Dual core
- Simultaneous multithreading
- 1.5 GHz @ 1.3 V
- 1.9 MB L2 cache and directory/control L3
- 24 temperature sensors



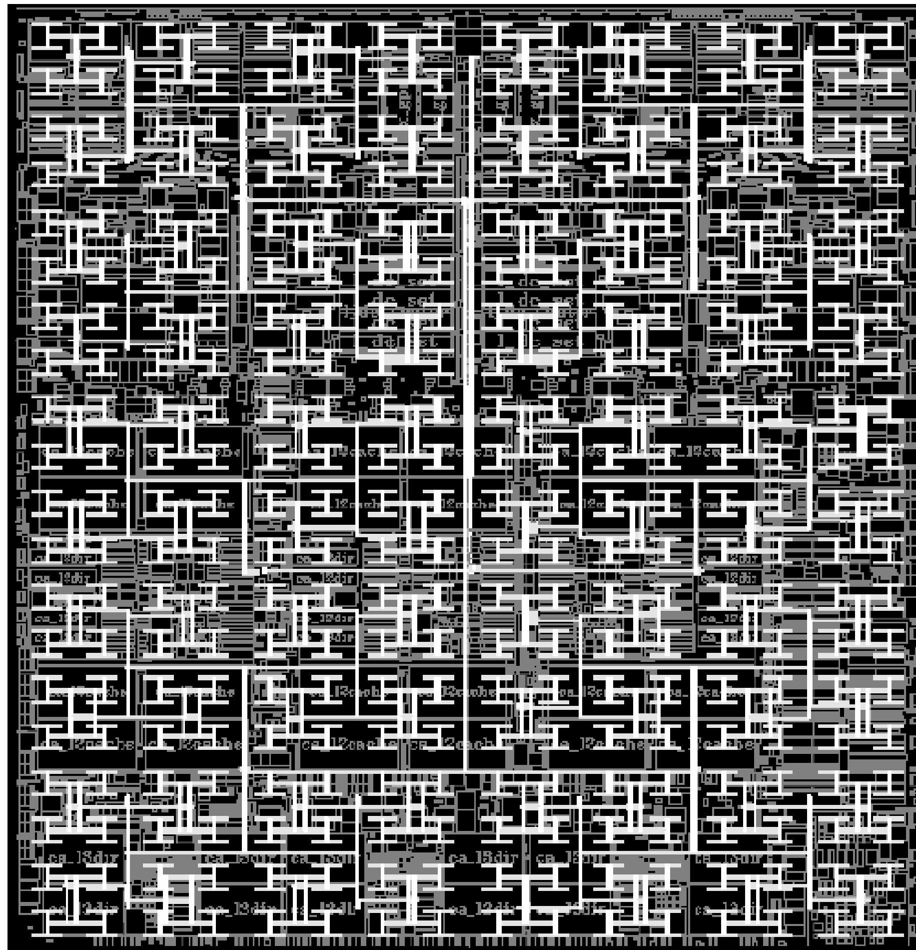
Design and Implementation of the POWER5^{TM} Microprocessor

International Solid-State Circuits Conference 2004

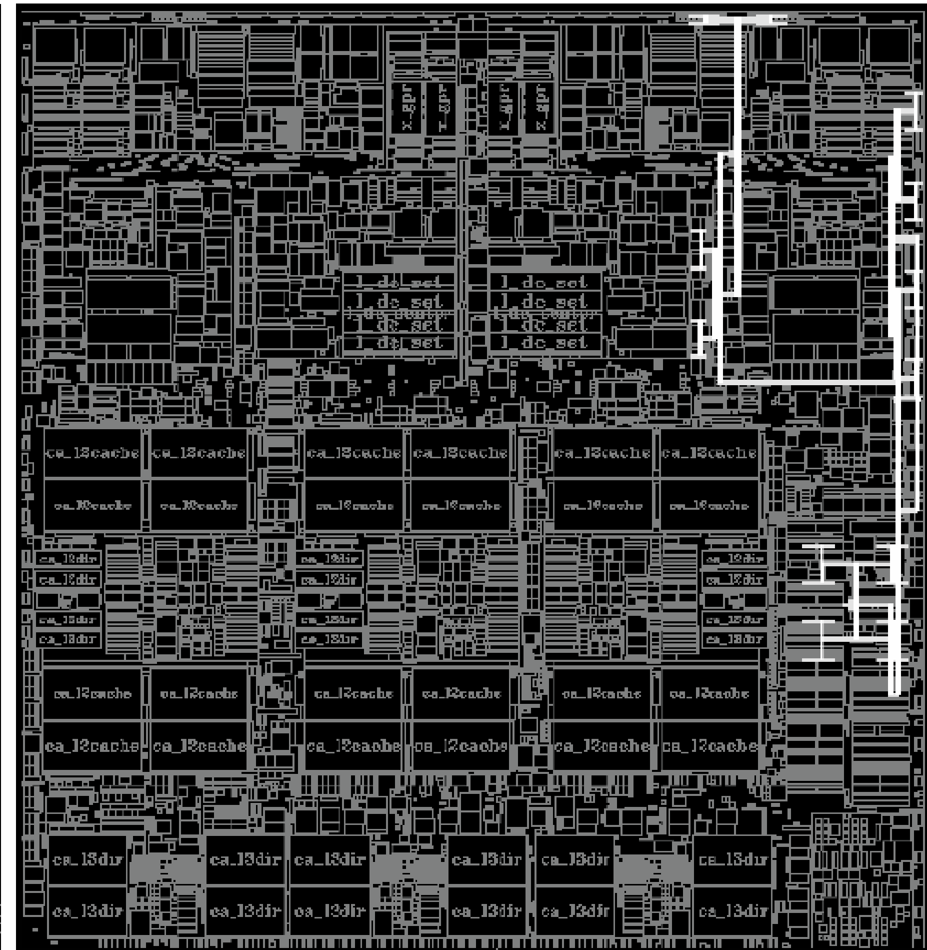

Processor Chip
Core
(SMT)
Core
(SMT)
NCU
NCU
CIU
NCU
NCU
L3
Cache
(36MB)
L3 Dir
L3 Cntl
1.9 MB L2 Cache
System
Memory
(64 GB)
DDR2
DRAMS
SMI
Mem Cntl
IO+ Cntl
GX+ Bus
SMP Fabric Cntl
Scalable SMP Buses
(8W-64W SMP)
2:1 Elastic Interface
2W-8W SMP Buses
1:1 Elastic Interface

- Clock distribution

Main clock



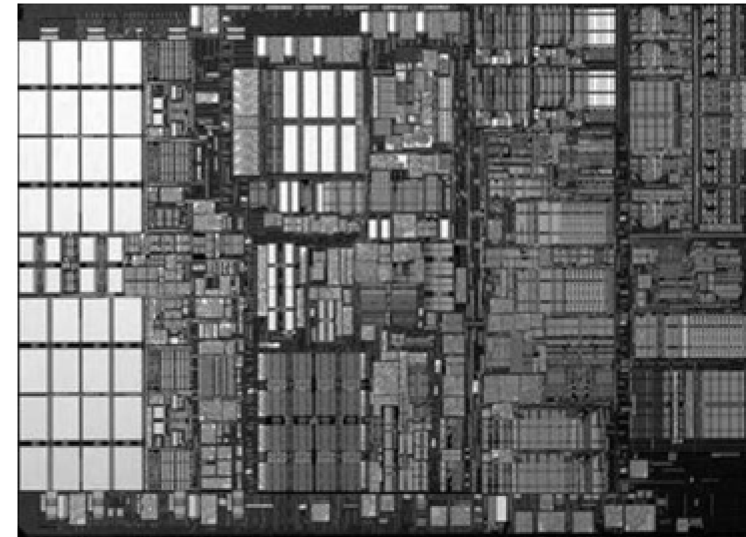
Memory clock

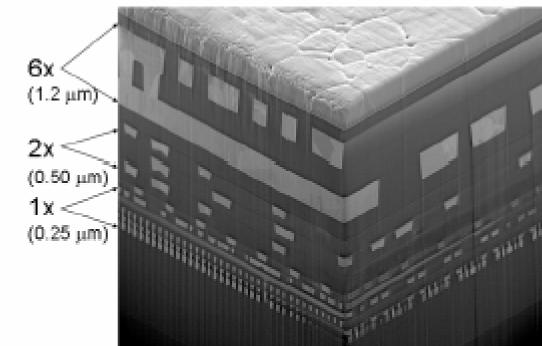


IBM 64-bit superscalar Microprocessor with power management *(2005)*

- 130 nm / 90 nm CMOS SOI
- 10 levels Cu
- Low-k dielectric
- 58 Mtransistors
- 118 mm^2 (130 nm) / 62 mm^2 (90 nm)
- 50 W @ 2.5 GHz @ 1.3 V

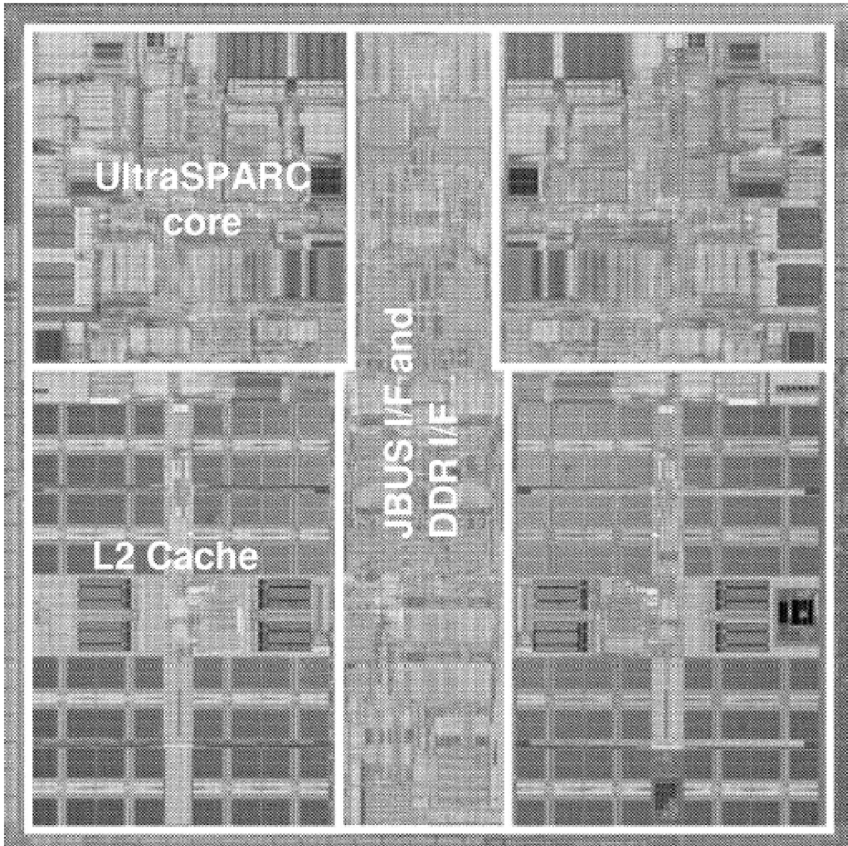
	130 nm	90 nm
Technology	CMOS w/ SOI	Strained CMOS w/ SOI
Gate Lpoly	55 nm	46 nm
Tox	13 & 22 Angstrom	10.5, 15 & 22 Angstrom
I_{dsat} NFET/PFET	917/418 μA/μm @ 1.2 V (AC) 850/408 μA/μm @ 1.2 V (with self-heating)	938/400 μA/μm @ 1.0 V (AC) 875/375 μA/μm @ 1.0 V (with self-heating)
I_{off} NFET/PFET	30 nA/15 nA @ nominal 200 nA/100 nA @ min	40 nA/40 nA @ nominal 300 nA/300 nA @ min
Metal Levels	Up to 8 with 1x, 2x and 4x in FTEOS	Up to 10 with 1x, 2x, 4x and 6x in FTEOS/low-k
SRAM cell	1.2 μm x 1.8 μm = 2.16 μm^2	0.84 μm x 1.26 μm = 1.06 μm^2

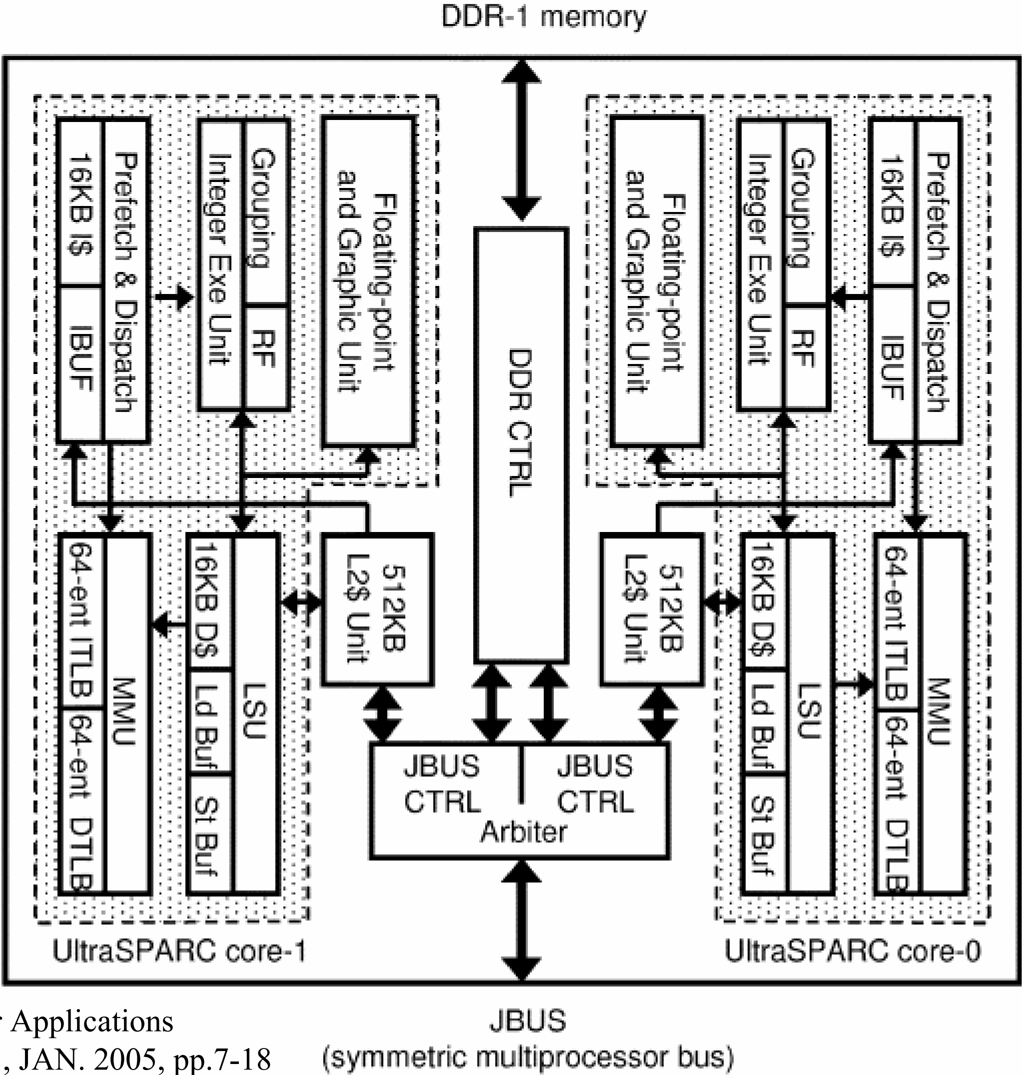




Norman J. Rohrer,*et al.,* "A 64-bit Microprocessor in 130-nm and 90-nm Technologies With Power Management Features", IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 40, NO. 1, JANUARY 2005, pp.19-27

Sun Microsystems Dual 64-bit UltraSparc (2005)

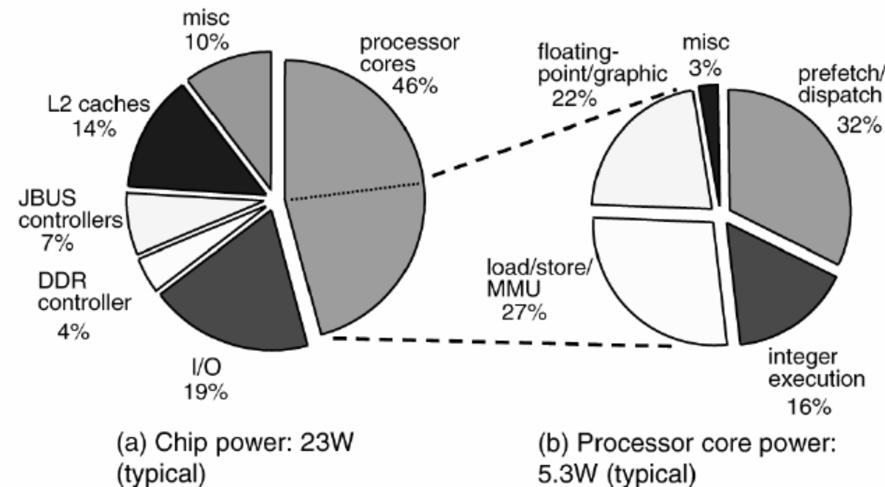




A Dual-Core 64-bit UltraSPARC Microprocessor for Dense Server Applications
IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 40, NO. 1, JAN. 2005, pp.7-18

Sun Microsystems Dual 64-bit UltraSparc (2005)

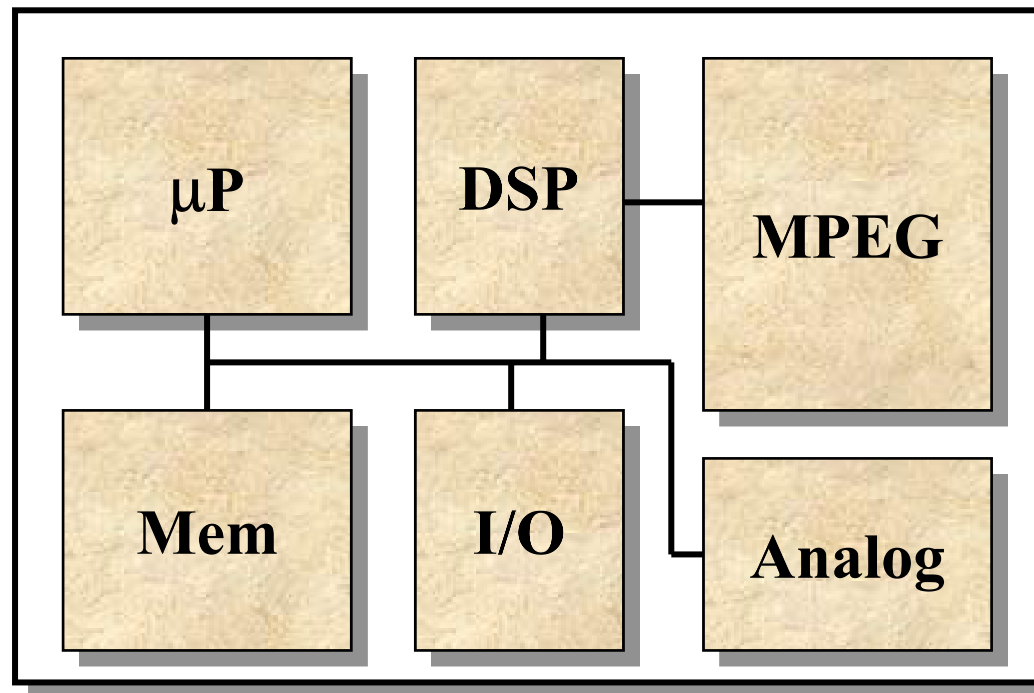
Process	0.25μm CMOS/5 layers Al (Original UltraSPARC I was fabricated in 0.5μm CMOS/4 layers Al.)	0.13μm CMOS/7 layers Cu
Voltage	1.9V	1.3V
Transistors	5.4M	80M total, 72M for SRAMs
Die size	126mm^2	206mm^2 , 29 mm^2 per core
Clock freq.	450MHz	1.2GHz
Power	23W	23W (typical), 5.3W per core
Max. memory bandwidth	3.6GB/s to L2 1.92GB/s to main memory	9.6GB/s to L2 4.26GB/s to main memory
Performance	2.5 SPECint_rate2000 (estimated)	11.0 SPECint_rate2000 (preliminary)



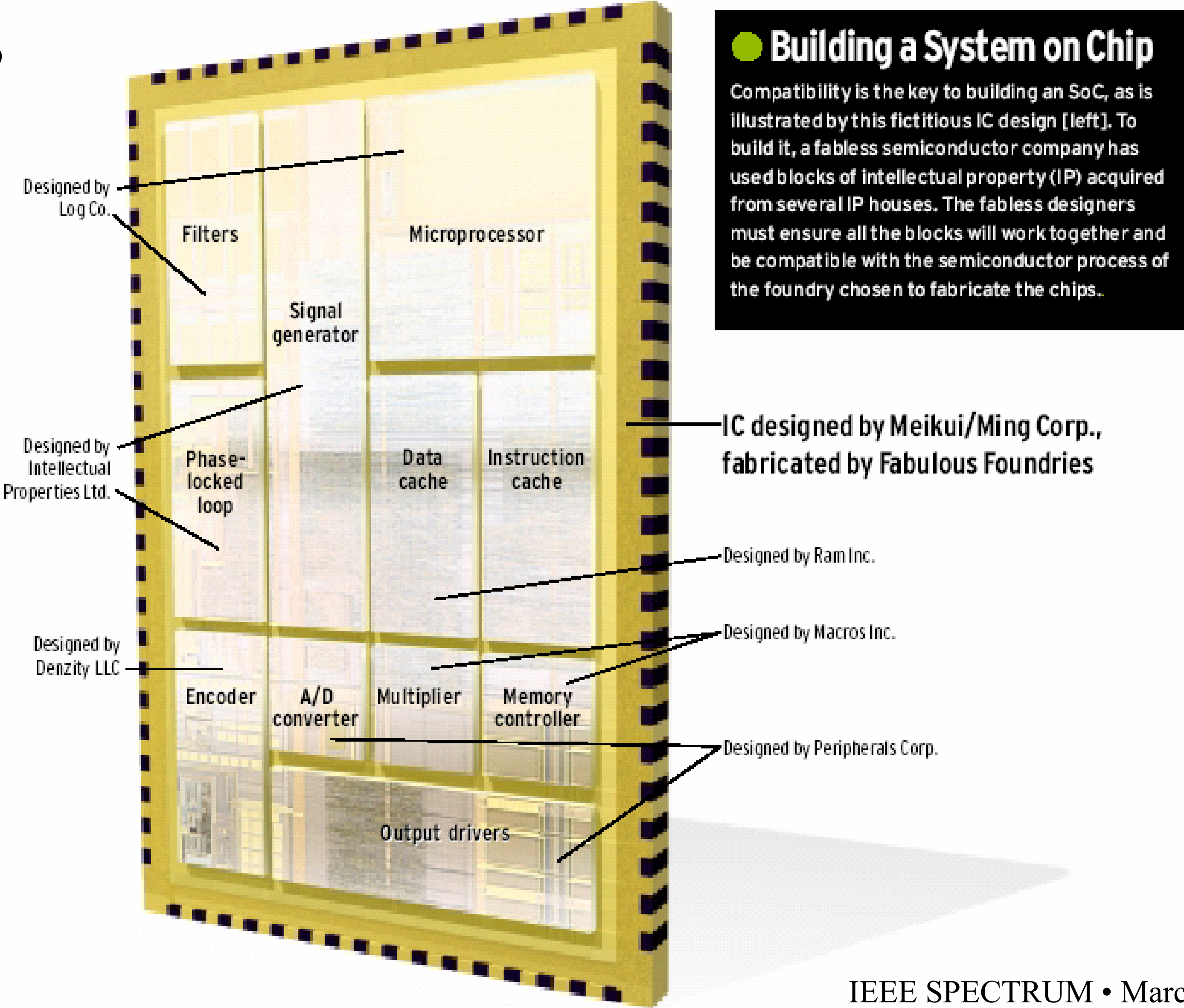
(a) Chip power: 23W (typical)
(b) Processor core power: 5.3W (typical)

Systems-on-chip, SoC, 1/3

- Current processes permit embedding in a single chip 8 Mgates and 140 Mbits of DRAM
- Technologies > 0.2 μm
- Packages of 1200 pins
- IP (Intellectual Property)-library based



SoC 2/3



IEEE SPECTRUM • March 2002

SoC 3/3

How Intellectual Property (IP) Revenues Grew Worldwide in 2000

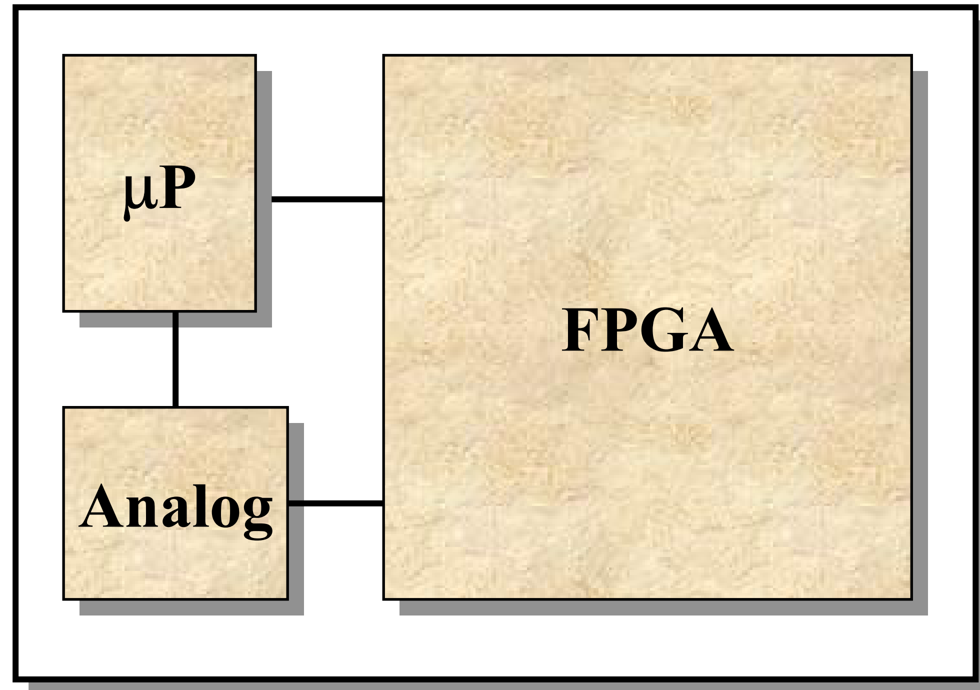
IP companies	2000 revenues, in US $ millions	Percent growth over 1999	IP companies	2000 revenues, in US $ millions	Percent growth over 1999
ARM	114.2	29.0	ARC Cores	16.1	455.2
MIPS Technologies	91.8	8.1	Tality	12.9	120.3
Rambus	72.3	66.6	Nurlogic	12.0	47.9
Mentor Graphics	34.1	6.3	Tensilica	10.3	110.2
Synopsys	33.8	39.5	Virtual Silicon	8.2	40.9
InSilicon	26.1	34.8	LEDA Systems	7.2	94.2
DSP Group	25.1	32.1	Zoran	6.8	41.7
Virage Logic	22.1	79.4	Sarnoff	6.4	-43.8
Artisan	20.8	23.7	Virtual IP Group	6.2	67.6
Parthus Technology	19.6	264.5	Others	127.0	51.8
TTP Com	17.0	45.0	**TOTAL**	**689.9**	**40.1**

Source: Gartner, Dataquest, May 2001.

IEEE SPECTRUM • March 2002

FIeld Programmable System-On-Chip (FIPSOC, 1999)

- Combines programming concepts of:
  - Microprocessor
  - FPGA
  - Analog circuits
- Integrated design environment
- Allows prototype realization of complete systems on chip.
- Easy retargetting
- Dynamically reconfigurable logic
- Software and hardware emulation



Simulation models

- HDL code. Either it can be synthesizable or not
- Useful for development stage (virtual prototyping)

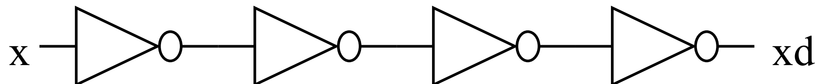
IP (Intellectual property) cores

Classes:
- Soft. synthesizable HDL code. Technology independent.
- Firm. Generic components.
- Hard. Physical components.

1.5. Synchronous design review

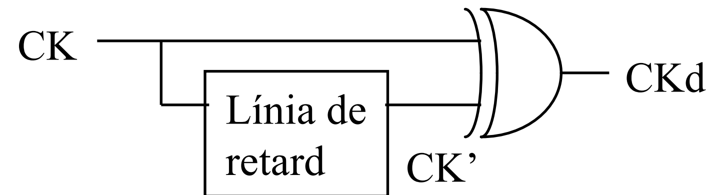
1.5.1 Non-recommended digital design techniques

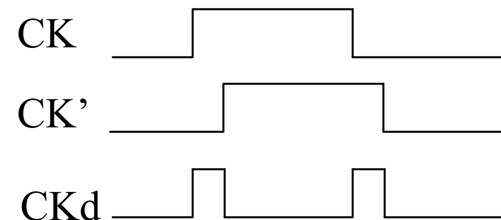
- Dubious techniques in ASIC semicustom design.
- Sometimes can be necessary.
  - Delay line
    - Sensitive to process and temperature variations ➔ variable delays
    - Unnecessary in synchronous designs



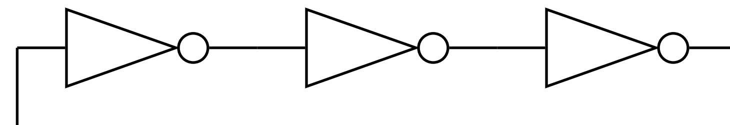
  - Frequency multiplier
    - Necessary in some specific circuits (UARTs...).
    - Normally implemented with external circuits (PLLs...).

- Example: frequency doubling.





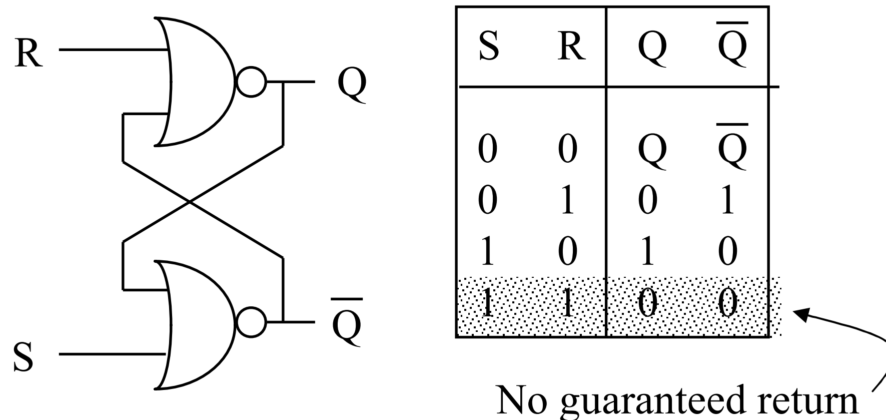
- On-chip oscillators



  - Better using library oscillators (normally in pads).

1.5.1 Non-recommended digital design techniques

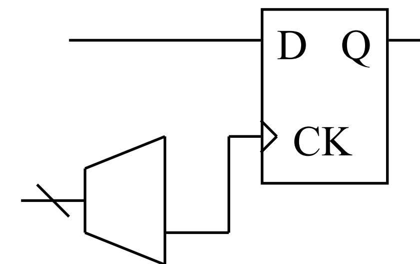
- RS flip-flop (asynchronous)
  - No guaranteed return from state R = S =1
  - Asynchronous operation
  - Sensitive to input *glitches*



S	R	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
0	1	0	1
1	0	1	0
1	1	0	0

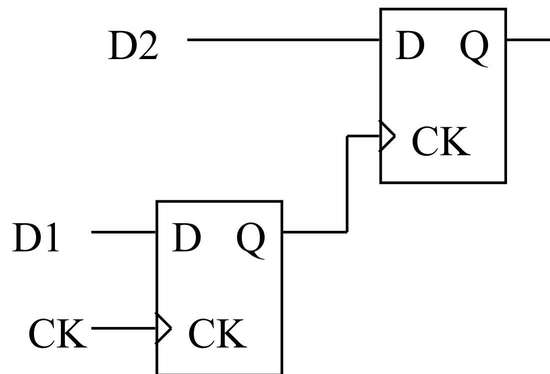
Normally it is not necessary to use this flip-flop. It can be usually replaced by a synchronous RS flip-flop.

- Implicit flip-flop
  - It arises from feedback loops in combinational circuits.
  - It must be avoided.
- Control elements incorrect usage
  - Decoders and comparators may produce *glitches* in their outputs.
  - It is discouraged to connect them to clock inputs.

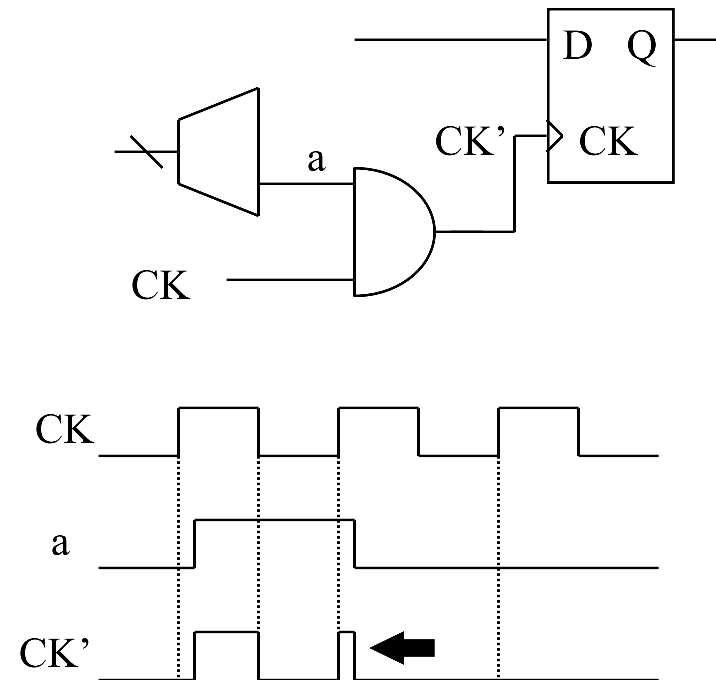


1.5.1 Non-recommended digital design techniques

- Latch output as a clock
  - Asynchronous clock
  - Prevents two successive captures

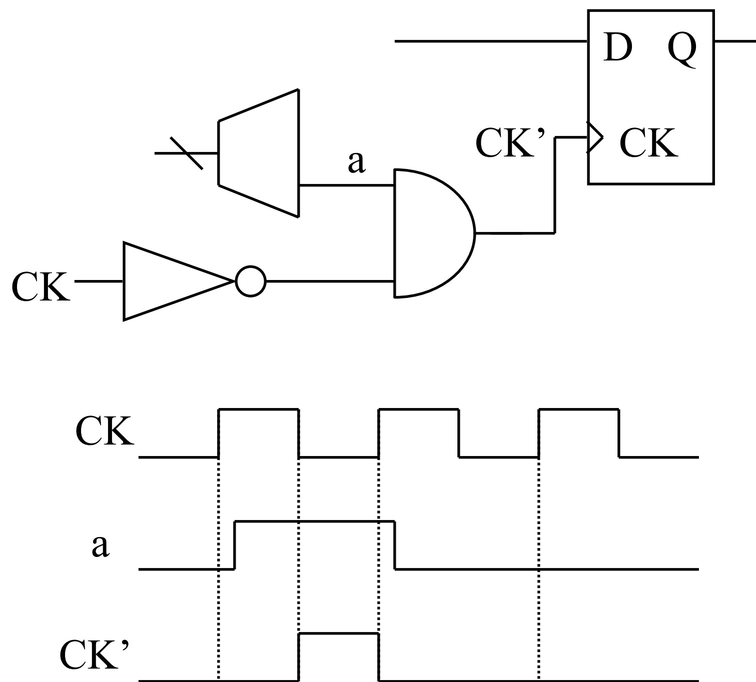


- Gated clock
  - Allows successive load, but the previous situation is even worse since there appear undesired pulses.

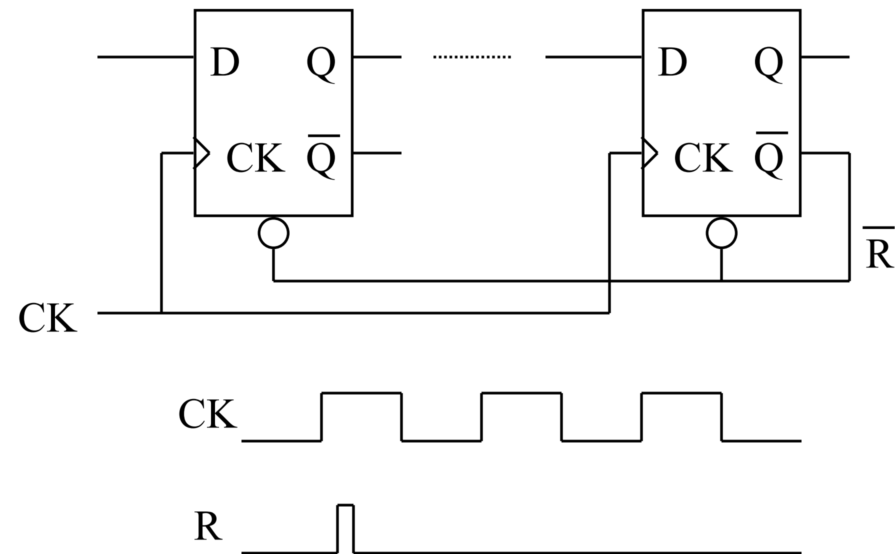


1.5.1 Non-recommended digital design techniques

- Negative clock edge
  - Reduces the available time to half the period ➔ circuits become slower.

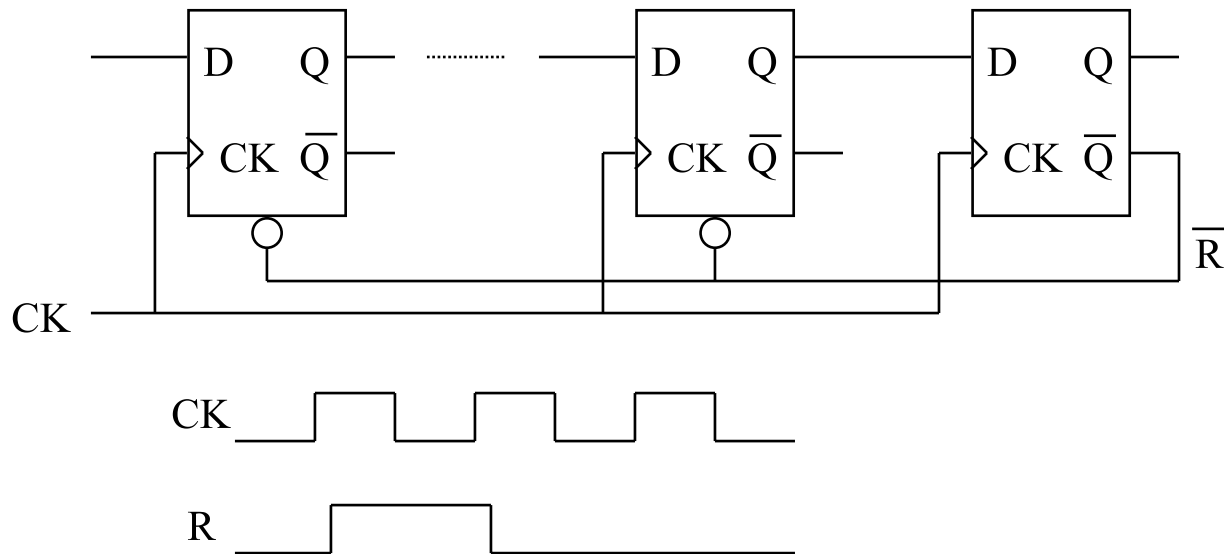


- Asynchronous clear. Short reset pulse.
  - Problems similar to *gated clock* and RS flip-flop.
  - Available time reduction during the reset period.



1.5.1 Non-recommended digital design techniques

- Asynchronous clear. Long reset pulse
  - Improves previous version.
  - A complete clock period is wasted.



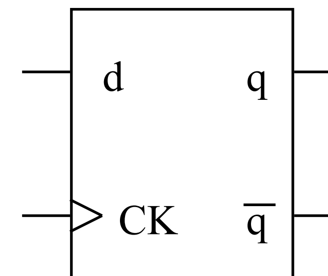
- Central clock generator.
  - Several clock signals are generated from counters or other elements.
  - Skew problem.

1.5.2 D, E, T, R synchronous flip-flops

Synchronous techniques:
- All elements operate with a clock edge (not level)
- One single primary system clock.

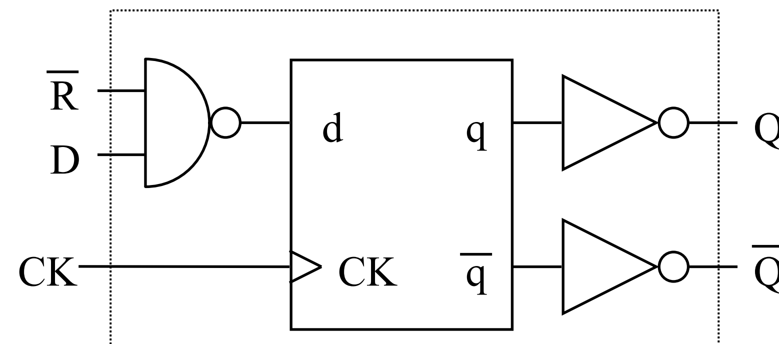
- **D flip-flop**

It is the basic element. Edge-triggered.
Constraints:
  - Setup time (input data stable before the active clock edge).
  - Hold time (input data stable after the active clock edge)
  - Minimum clock pulse width.



- **D flip-flop with synchronous clear**

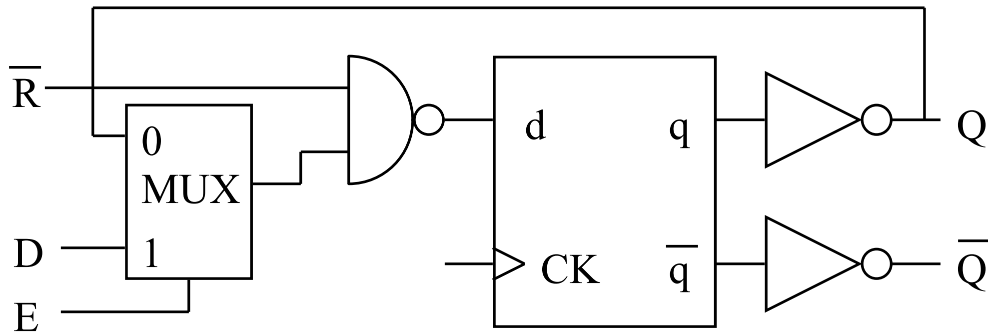
Asynchronous reset signals must be avoided.
Output inverters improve the flip-flop drive capacity.



• **E (Enable) flip-flop**

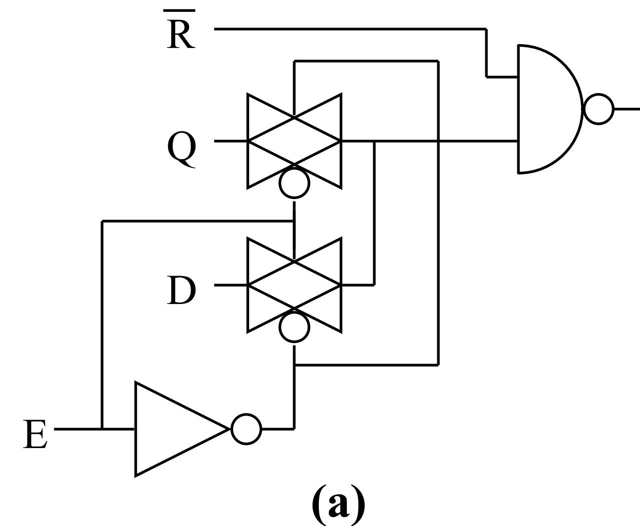
Loads input data when E is active, otherwise the flip-flop keeps the stored value.

Observation: The clock is not gated.

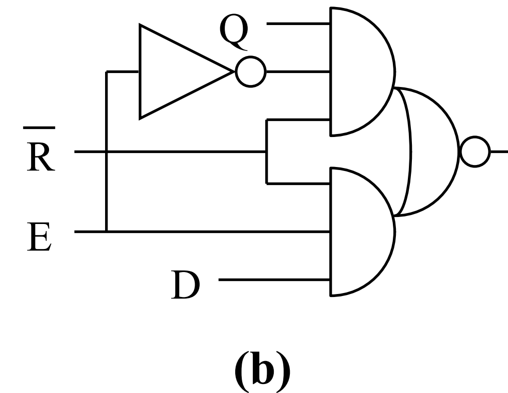


$\overline{R}$	E	D	Q	$\overline{Q}$	Operation
0	X	X	0	1	Reset
1	0	X	Q	$\overline{Q}$	Previous state
1	1	0	0	1	Data input
1	1	1	1	0	Data input

Mux solutions:



(a)

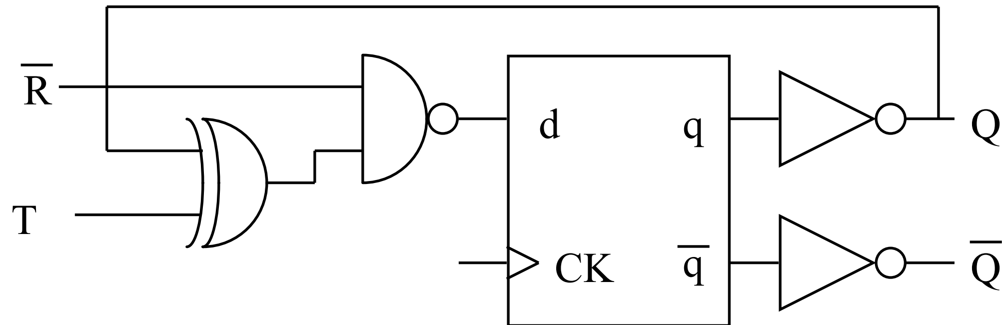


(b)

1.5.2 D, E, T, R synchronous flip-flops

•T (*Toggle*) flip-flop

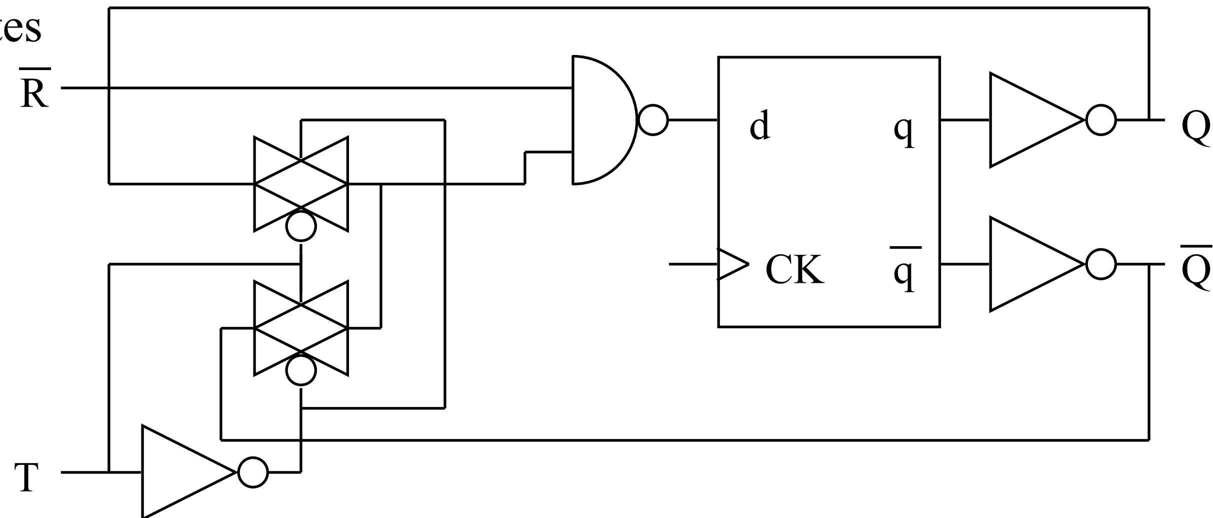
Useful for counters.



$\overline{R}$	T	Q	$\overline{Q}$	Operation
0	X	0	1	Reset
1	0	Q	$\overline{Q}$	Previous state
1	1	$\overline{Q}$	Q	Inverting

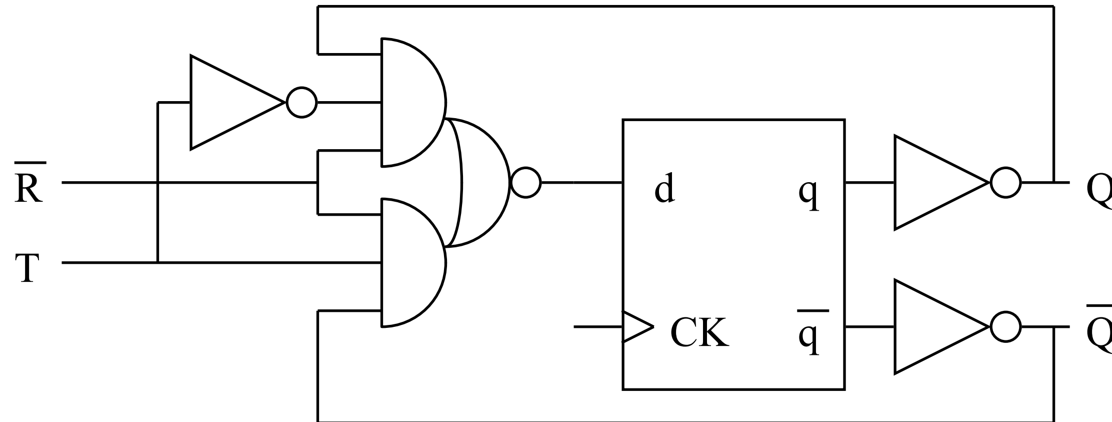
Possible implementations:

• Transmission gates

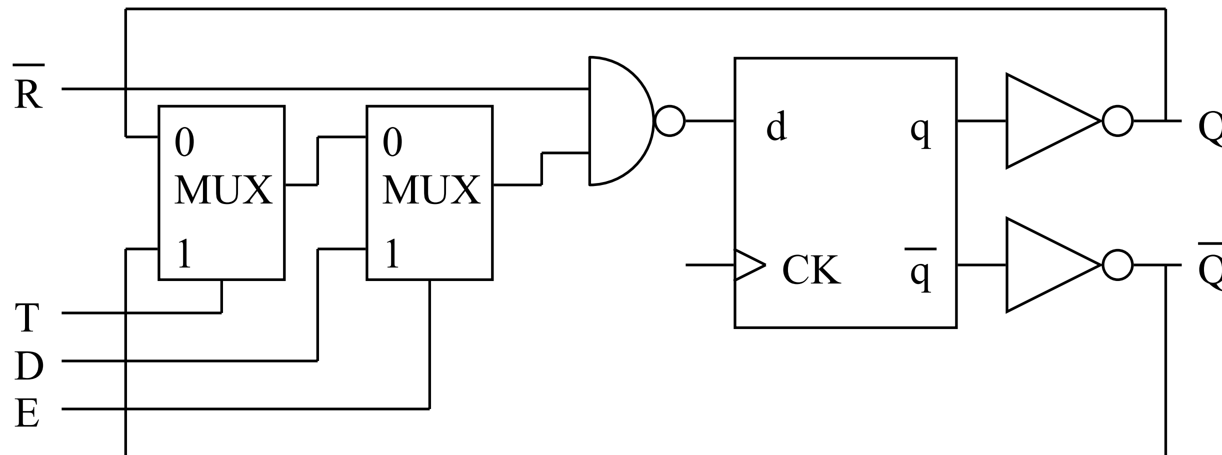


1.5.2 D, E, T, R synchronous flip-flops

- Complex gates



- **Hybrid E/T Flip-flop**

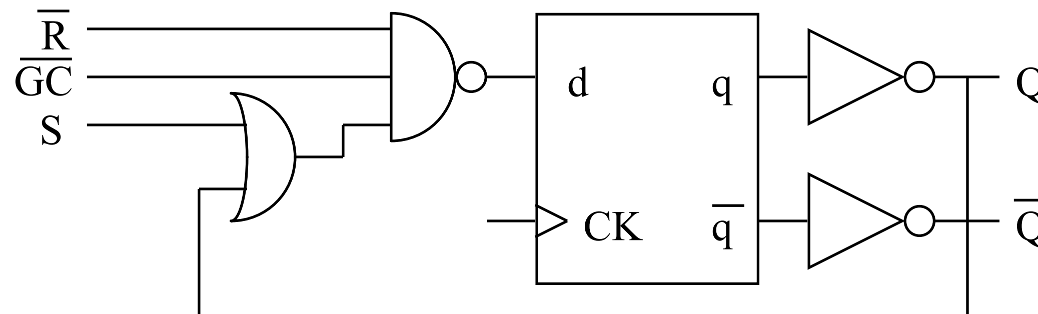


$\overline{R}$	E	T	D	Q	$\overline{Q}$	Operation
0	X	X	X	0	1	*Reset*
1	0	0	X	Q	$\overline{Q}$	Previous state
1	0	1	X	$\overline{Q}$	Q	Inverting
1	1	X	0	0	1	Data input
1	1	X	1	1	0	Data input

- **Synchronous RS flip-flop**

Global clear for reset and test.

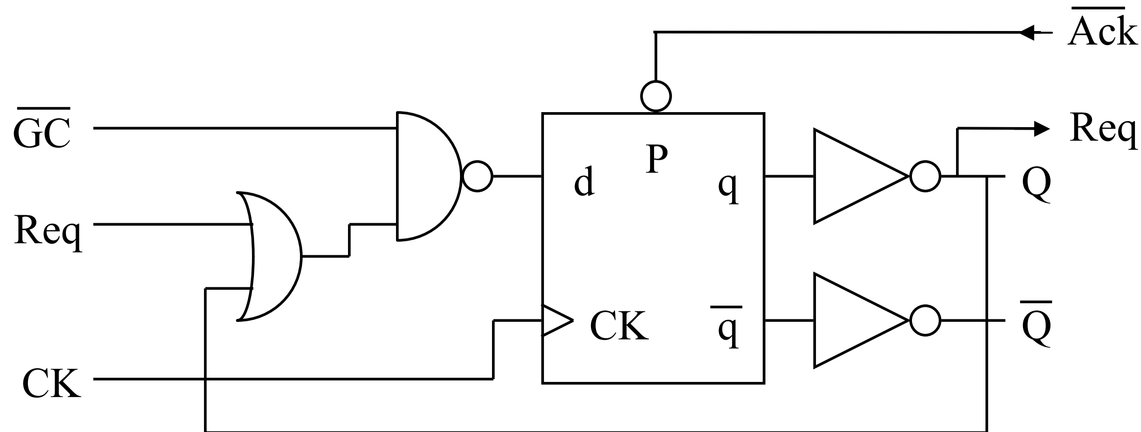
Reset (R) input has higher priority than set (S) input.



$\overline{GC}$	$\overline{R}$	S	Q	$\overline{Q}$	Operation
0	X	X	0	1	Global clear
1	0	X	0	1	Reset
1	1	0	Q	$\overline{Q}$	Previous state
1	1	1	1	0	*Set*

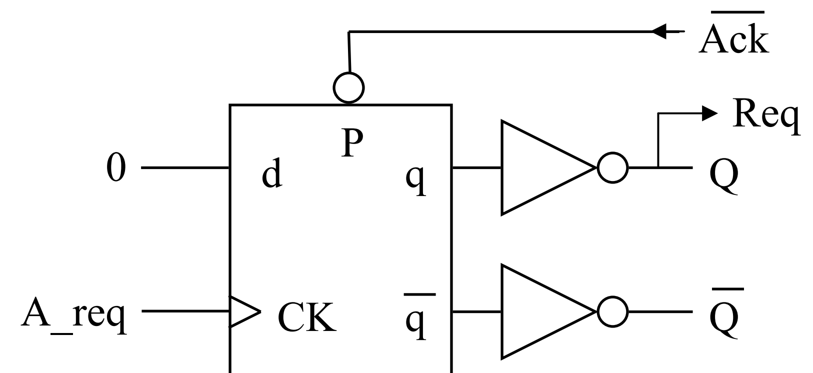
•R (*request*) flip-flop

Request is synchronous, *acknowledge* is synchronous



$\overline{Ack}$	$\overline{GC}$	Req	Q	$\overline{Q}$	Operation
0	X	X	0	1	Asynchronous clear
1	0	X	0	1	Synchronous clear
1	1	0	Q	$\overline{Q}$	Previous state
1	1	1	1	0	Request

Asynchronous version

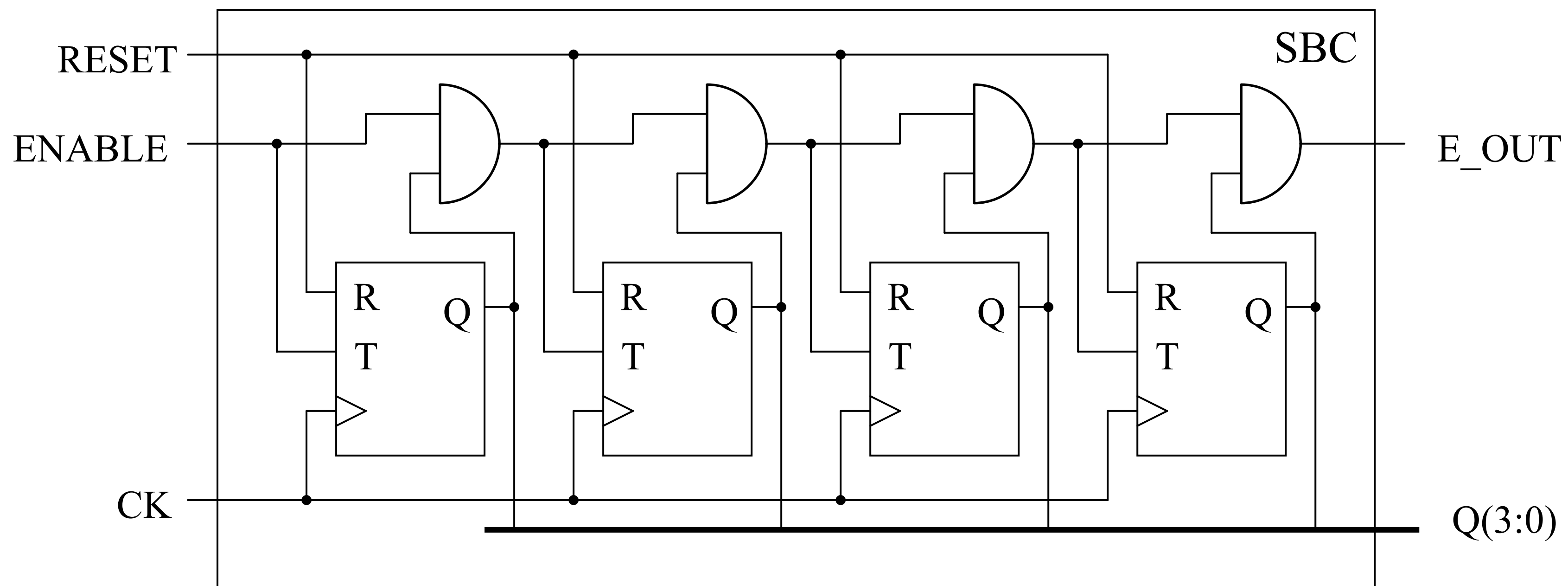


1.5.3 Building synchronous systems

From the previous primitives completely synchronous systems can be implemented.

• **Synchronous Binary Counter (SBC)**

Is the basic block



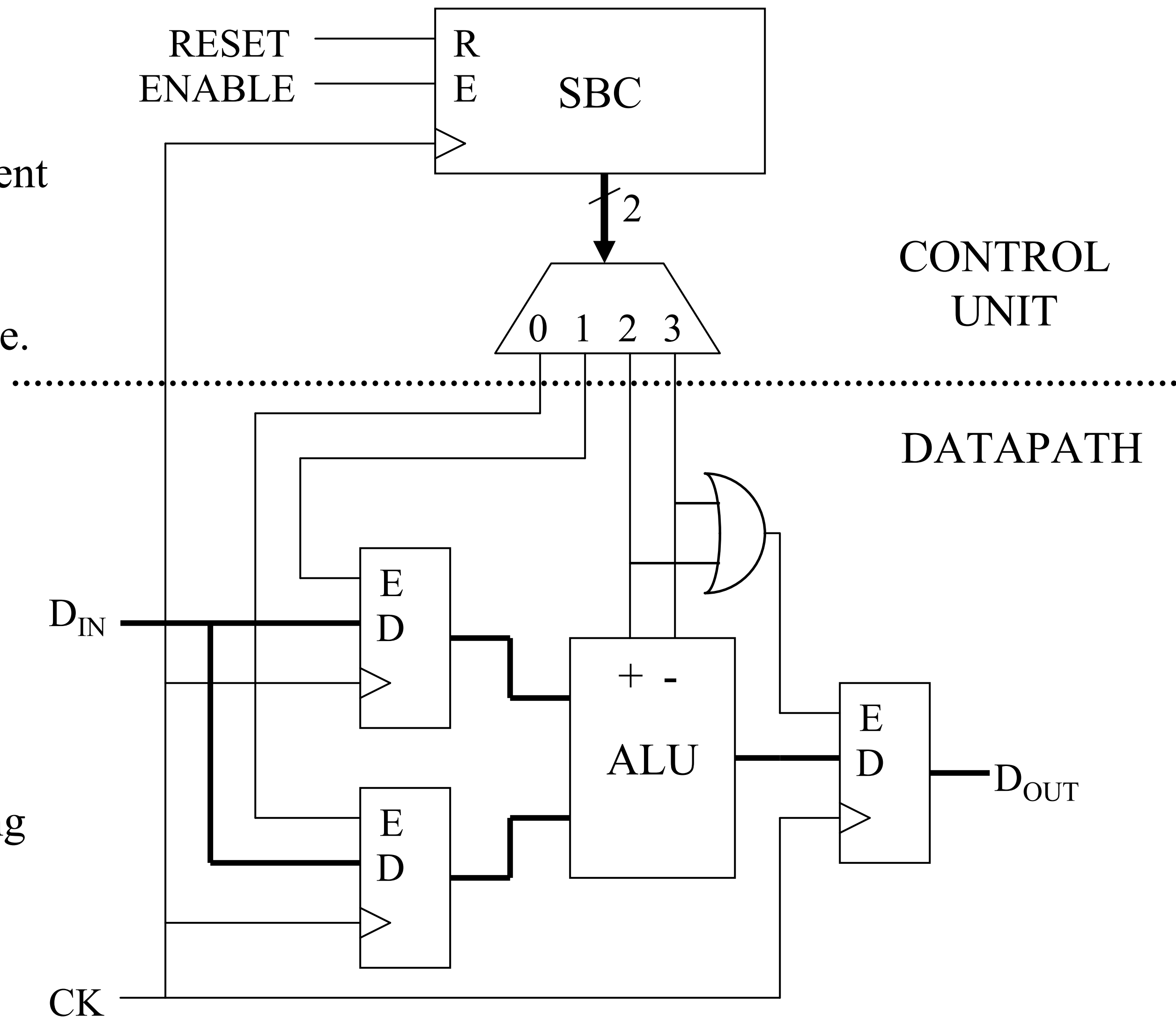
- **Cyclic state generator**

Based on:

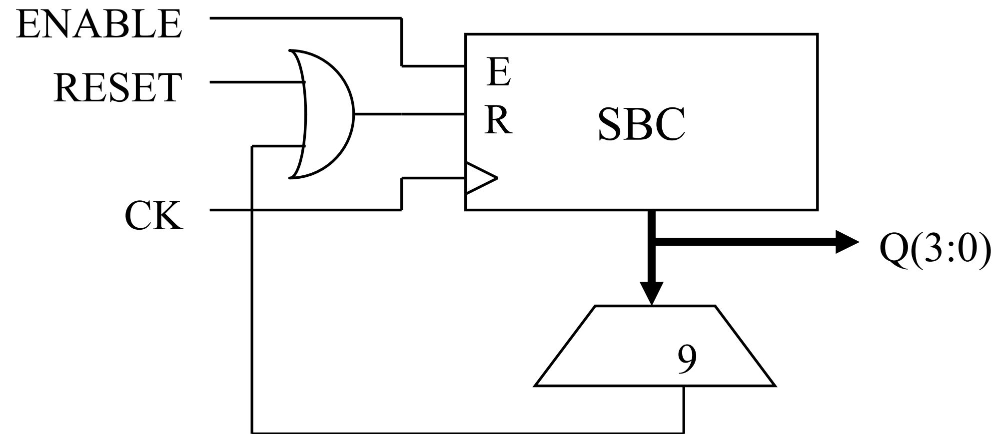
- Counter: Encodes the current state.
- Decoder: Activates lines related with the current state.

Example: Algorithmic State Machine (ASM)

Other control strategies as hardwired o microprogramming could also be applied with synchronous techniques.



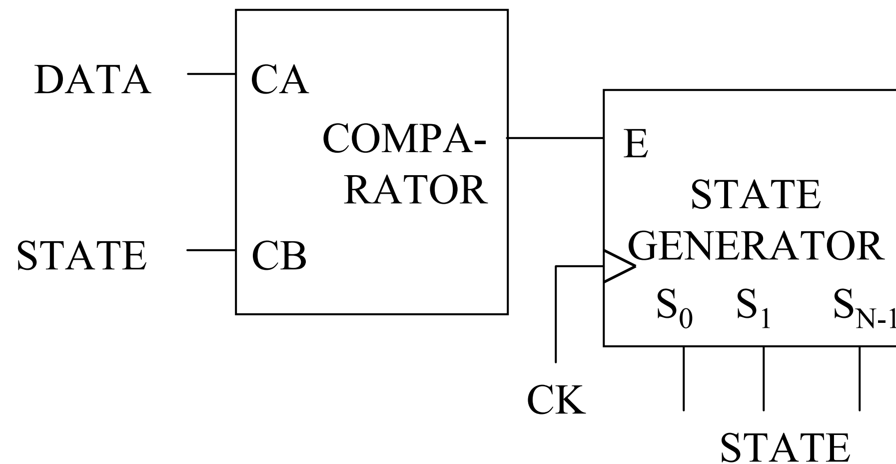
• **Modulus 10 counter**



• **Control conditional variation**

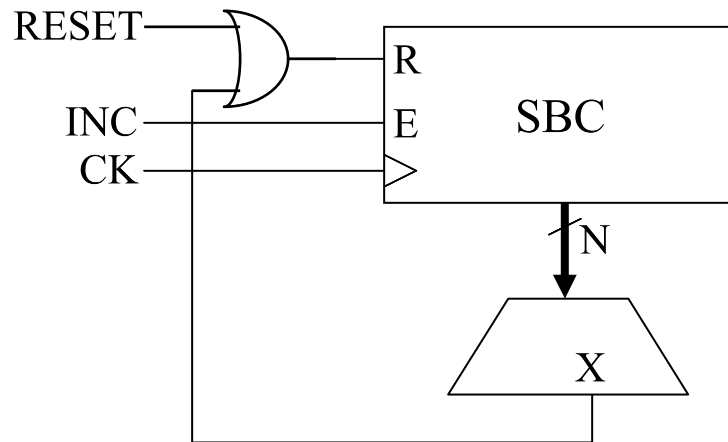
Depends on:
- Internal values
- External variables

Example:



Conditional execution modes

• **Incremental mode**



• **Conditional waiting mode**