**Master of Science in Information and Communication Technologies**

# VLSI Digital Design
# Spring-06 Term

## Course Objectives

- To introduce the IC design process.
- To identify the designs that require integrated solutions.
- To identify the constraints imposed by digital VLSI implementations.
  - Synchronous design
  - Electric aspects
  - High-performance circuits
  - Fundamental subsystems
  - Test techniques
- To use proper design styles for VLSI.
- To design using high-level hardware description languages (HDLs).
  - Simulation and validation tools.
  - Synthesis tools.

## Assessment

Theory: **50 %**

- **EX**: Proposed exercises **5 %**
- **PR**: Design project **15 %**
- **ME**: Mid-term exam: **10 %**
- **FE**: Final exam : **20 %**

Lab assignments: **50 %**

- **LV**: Lab VHDL exam **2.5 %**
- **LW**: Lab work **35 %**
- **LE**: Lab exam: **12.5 %**

**To pass, all the following requirements are necessary:**

- **FE ≥ 3 or weighted FE and ME ≥ 3**
- **Theory grade ≥ 4**
- **Lab grade ≥ 4**

# Theory syllabus (1/2)

**I. Introduction (2 weeks)**

- 1.1. Technologies for digital design
- 1.2. Integration capability and future trends
- 1.3. Design Techniques
- 1.4. State of the art
- 1.5. Synchronous design review
  - 1.5.1. Non-recommended digital design techniques
  - 1.5.2. Synchronous flip-flops
  - 1.5.3. Building synchronous systems

**II. CMOS Logic Design (3 weeks)**

- 2.1. Switching characteristics review
- 2.2. Delay, logical effort and buffering
- 2.3. Logic structures
- 2.4. Clock strategies

**III. Physical Design Issues (2 weeks)**

- 3.1 Low-power design
- 3.2 Power-supply and clock distribution

# Theory syllabus (2/2)

**IV. Arithmetic and Logic Subsystem Design (3 weeks)**

4.1 Algorithmic systems and structured design
4.2 Datapath operators: adders
4.3 Datapath operators: multipliers
4.4 Other operators

**V. Test Techniques (2 weeks)**

5.1 Introduction.
5.2 Manufacturing test principles.
5.3 Design for test.
5.4 Self-test.
5.5 System-level test

# Lab Syllabus

**LAB Objective: Description, Simulation and Synthesis with VHDL**

| | |
|---|---|
| 0. Introduction to the development environments<br>ModelSim, Precision and Xilinx ISE | (1 week) |
| 1. Practical Aspects of Synchronous Digital Design | (2 weeks) |
| 2. Arithmetic-Logic Unit (ALU) | (2 weeks) |
| 3. Timer Design | (2 weeks) |
| 4. AMBA Bus | (2 weeks) |
| 5. Register Bank | (1 week) |
| 6. Functional verification and application | (2 weeks) |
| 7. *Placement* and *routing* of an integrated circuit | (1 week) |

# References

**BASIC**

- **Digital Integrated Circuits. A Design Perspective**
  Jan M. Rabaey
  Prentice-Hall, 2003 (2a ed.)

- **The Designer's Guide to VHDL**
  Peter J. Ashenden
  Morgan Kaufmann Publishers, 2002 (2a ed.)

**COMPLEMENTARY**

- **Designing ASICS (Module 1)**
  P. Naish, P.Bishop
  Ellis Horwood, 1988

- **Computer Arithmetic Systems (Module 4)**
  A. R. Omondi
  Prentice-Hall, 1994

- **CMOS VLSI Design : A Circuits and Systems Perspective (Modules 2, 4, 5)**
  N.E. Weste, D. Harris
  Addison-Wesley, 2004 (3a. edició)

- **Low Power Digital CMOS Design (Module 3)**
  Chandrakasan A.P., Brodersen R.W.
  Kluwer Academic Publishers, 1998

- **Essentials of Electronic Testing (Module 5)**
  Bushnell. M.L.; Agrawal, V.D.
  Kluwer Academic Publishers, 2000

- **Digital Systems Engineering**
  Dally, W.J.; Poulton, J.W.
  Cambridge University Press, 1998

- **Surviving the SOC Revolution A Guide to Platform-Based Design**
  Chang H. et al.
  Kluwer Academic Publishers, 1999