VLSI Digital Design

LAB ASSIGNMENT 3

Timer Design

0. Objectives

In this laboratory assignment, the basic principles required for the implementation of sequential digital systems with ability to carry out timing tasks or system synchronization.

The ultimate laboratory objective is the design of a peripheral for the microprocessor considered in the course laboratory. This peripheral operates as a 16-bit programmable timer.

1. Specification

The structure of the timer to be designed is organized around the following functional basic blocks:

- **Counter.** It consists in a 16-bit synchronous binary descending counter. At any time, the contents of this counter can be loaded with the value stored in a special-purpose register (called data register). Also, it has to be possible to read or write the counter value by means of the input/output busses connected to the timer.
- **Data register:** The content of this 16-bit register can be loaded to the system counter. This register has to be readable and writable by means of the input/output busses connected to the timer.
- **Control register:** This 4-bit register controls the timer operation. The most significant bit enables (at level high) the timer operation. The second most significant bit establishes the timer operating mode: at low level ('0') it selects the free operating mode, and at high ('1') level, the cyclic operating mode. The two least significant bits of this register determine the counter timing. This register has to be readable and writable by means of the input/output busses connected to the timer.
- **Prescaler:** This component controls the 16-bit counter timing. To this purpose, it generates the enable signal of the counter as a function of the two least significant bits of the control register. When the content of these two bits is “01”, the enable signal has to be generated every 16 clock periods; when its content is “10” the enable signal has to be generated every 256 clock periods; finally, when its content is “00” the enable signal is continuously active, so that the counter will decrement its value every rising edge of the system clock signal. Code "11" is not used.

All the subsystems composing the timer have to operate synchronously and be active with the rising edge of the system clock.

As previously indicated, the timer supports two operating modes. In the free operating mode, when the counter reaches the value 0x0000, it will continue decrementing its value, so the following count value will be 0xFFFF. Conversely, in the cyclic operating mode, when the counter reaches the value 0x0000, in the next clock cycle it will load again the content of the timer data register. In both operating modes, when the 0x0000 value is reached, the so-called ***interrupt*** output signal has to be activated. This signal is used as a microprocessor interrupt. This output signal will remain active until being reset by a write operation addressed to the register that stores the ***interrupt*** signal.

In order to allow external access to the memory elements that constitute the timer, the following signals are provided: ***r_wn***, a two-bit address bus ***address(1:0)***, a 16-bit input data bus ***data_in(15:0)*** and a 16-bit output data bus ***data_out(15:0)***. The function implemented on the timer as a function of the values that the input signals take is defined in Table1.

r_wn	address(1:0)	Action
0	00	Control register is written with the 4 least significant bits of the input data bus.
0	01	Simultaneous write to the internal data register and to the counter of the input data bus content.
0	10	***interrupt*** register reset.
1	00	Control register read on the 4 least significant bits of the output data bus. The 12 most significant bits of this bus have to be forced to logic '0'.
1	01	Timer data register read on the output data bus.
1	10	The current value of the counter is read on the output data bus.

Table 1. Definition of the timer read/write operations.

The system to be designed should be assigned ***timer*** as entity name. Taking the former specifications into account, its input/output interface consists of the following signals:

- **clk:** System global clock signal (active at rising edge, 25 MHz).
- **clearn:** System global reset signal. Synchronous and active at level low ('0').
- **r_wn:** Signal that indicates the access mode to the timer subsystems: read (***r_wn='1'***) or write (***r_wn='0'***).
- **address(1:0):** Two-bit address bus used to address, in read or write mode, the timer subsystems.
- **data_in(15:0):** Input data bus. All the timer write operations take place on this bus.
- **data_out(15:0):** Output data bus. All the timer read operations take place on this bus.
- **interrupt:** Output signal generated from the timer counter. This signal is used as an interrupt request to the microprocessor. To disable this signal, a write operation has to be performed on the interrupt register.