VLSI Digital Design

Tutorial on compilation and physical verification

0. Introduction

This document provides information about the basic steps to be followed in order to complete the compilation process of the results obtained after the VHDL description of a digital system is synthesised. It also indicates how the results of the compilation process can be used in order to validate the final physical realisation of the system prior to its implementation.

1. Compilation

The compilation tool that will be used in the laboratory is called Xilinx ISE, and it can be launched through the icon labelled Xilinx ISE in the Windows desktop. Once it is opened it is possible to observe the organisation of its graphical, as depicted in figure 1.

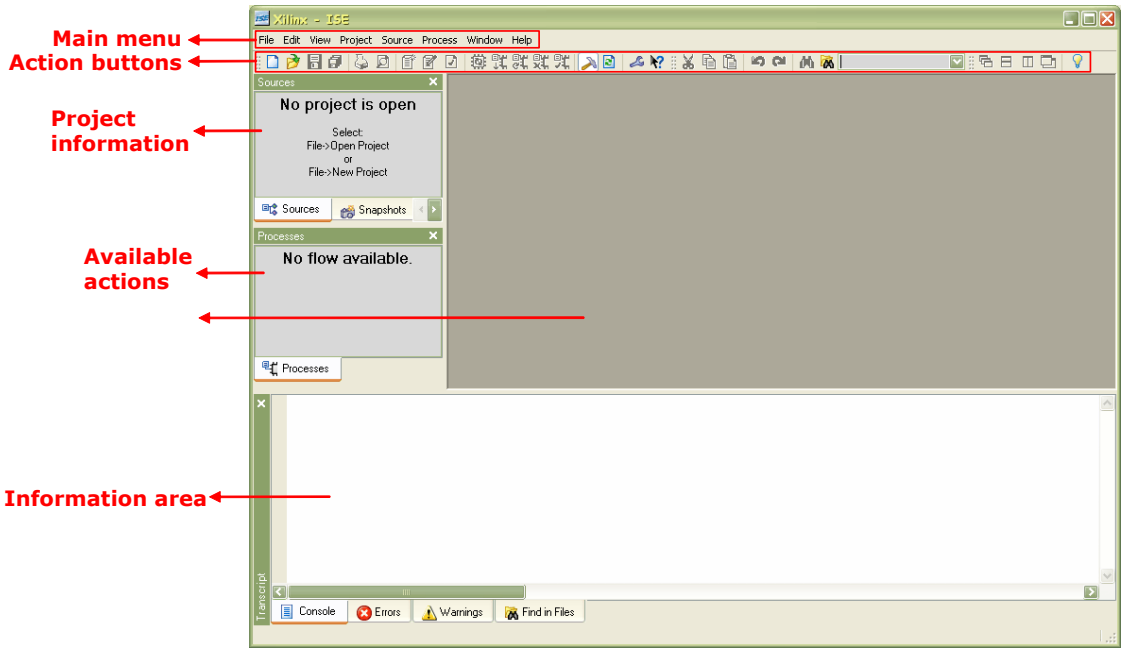

Figure 1. Organisation of the graphical interface of the Xilinx ISE compilation tool

The steps to be followed in order to compile the system are the following:

1. The first step consists in defining the project. To do this it is necessary to select the ***File -> New Project…*** in the main menu. A dialog box will be displayed where the basic features of the project have to be set. In the ***Project Name:*** section the name of the project has to be set (in our case, ***tutorial***). In the ***Project Location:*** section it is necessary to specify a convenient folder to save the results of the compilation. It is important to specify a file path without any space character. In the ***Top-Level Source Type:*** section it is required to select the type of input to be used for the compilation. The option to be chosen is ***EDIF***. Once these options are set it is possible to click on the button labelled as ***Next>*** in the bottom of the dialog window. In the next dialog window, in the ***Input Design:*** section it is necessary to browse the user folders in order to select the ***pwm.edf***

file generated during the synthesis process. Also, although not necessary in this tutorial, a UCF constraints file usually has to be specified. This file assigns the FPGA physical pins to the design input/output signals. After setting the EDIF file, it is possible to click on the button labelled as ***Next>*** in the bottom of the dialog window. In the next dialog window the following parameters have to be set: ***Family: Spartan2E***, ***Device: XCS200E***, ***Package: PQ208***, ***Speed: -6***. Then it is possible to click on the button labelled as ***Next>*** in the bottom of the dialog window. A final dialog window is displayed with the information that has been set for the project. In this window it is possible to click on the button labelled as ***Finish***. Then it is possible to observe that the areas corresponding to the project information and available actions in the user interface of the compilation tool have been modified.

2. The next step in the compilation process consists in defining the properties of the project. This can be done by clicking with the right mouse button on the ***Implement Design*** field of the available actions section (make sure that the design *pwm(pwm.edf)* is selected in the sources window), and then choosing ***Properties…*** in the context menu. In the dialog window that will appear thereafter it is necessary to select the ***Place & Route Properties*** section placed in the Category area (left part of the window). Then in the right part the option ***Generate Post-Place & Route Simulation Model*** has to be activated. By clicking on the button labelled OK in the bottom of the window the new option will be set. This option tells the tool to generate a new VHDL description of the compilation results and its associated delay file in SDF format. These files, called ***pwm_timesim.vhd*** and ***pwm_timesim.sdf***, respectively, are placed after the compilation process in the folder ***netgen\par*** that is created under the folder specified for the ***Project Location:*** option in step 1. The ***pwm_timesim.vhd*** file contains a structural netlist corresponding to the design implemented with the low-level resources (gates and registers) available in the programmable device. The ***pwm_timesim.sdf*** specifies the delays to be associated with these low-level resources, as well as the propagation delays corresponding to the signals present in the physical design.
3. The project is now ready for compilation. In order to start the compilation process it is necessary to click with the right mouse button on the ***Implement Design*** field of the available actions section and then selecting the Run option in the context menu. A series of information messages are displayed in the information area of the user interface of the compilation tool. Once the compilation process is finished an icon labelled as  will appear on the left of the ***Implement Design*** field of the available actions section.
4. Once the compilation of the design is completed it is possible to analyse the results obtained. By double-clicking on the View Design Summary field of the available actions section it is possible to browse the main features of the design after its physical implementation. Special attention must be paid to the value given under the section ***Timing Constraints***, since it represents the minimum clock period that can be used for the design.

2. Physical verification

Once the design has been translated to a physical representation, and prior to its final implementation, it s necessary to verify that the timing features associated with this new

representation still permit the system to meet the initial specifications. For this purpose a new simulation process with backannotated delays will be performed. During this simulation the two files generated during the compilation stage, called ***pwm_timesim.vhd*** and ***pwm_timesim.sdf***, will be used. The sequence of steps to be performed in order to complete the physical verification of the system is the following:

1. Open the ModelSim project that was used for the functional verification of the system.
2. Add the ***pwm_timesim.vhd*** file to the current project.
3. Compile all the files in the current project.
4. Start the elaboration of the project by choosing ***Simulate -> Start simulation…*** option in the main menu.
5. In the dialog window that will appear, first select the entity to be elaborated (***work -> pwm_test***). In the right part of this dialog window, in the ***Resolution*** section, change the simulation resolution from ***default*** to ***ps***. In the same dialog window, click on the ***SDF*** tab.
6. Once the ***SDF*** dialog window is opened, click on the ***Add…*** button. A new dialog window is opened. In the ***SDF File*** section choose the ***pwm_timesim.sdf*** file that was generated during the compilation process. In the ***Apply to Region*** section enter ***pwm_bloc***. This is the name given to the instance of the pwm entity that is used in the ***pwm_test.vhd*** testbench. Then click on the button labelled as ***OK*** in this dialog window and also in the button labelled as ***OK*** in the ***Start Simulation*** dialog window. Some messages corresponding to the elaboration of the design will be displayed in the ***Transcript*** window.
7. The design can now be simulated as it was explained in the simulation tutorial. It is interesting now to notice that the delay between the rising edge of the clock and the output pulse is no more 0, as it was the case for the functional verification, since the actual values for the delays in the system are used now.