TEXAS INSTRUMENTS

Linear Products

Automotive Anti-Lock Brake System Control Using Power+™ Control Devices

Many of the electronic systems in today's automobiles require fault protection and diagnostics to meet environmental and safety regulations. The anti-lock brake system (ABS) is one area where safety is a key concern. The ABS designer is faced with requirements to insure that the system functions properly under strict operating conditions and that failures are detected and handled properly. The ability to quickly identify and diagnose a problem is also an important consideration in reducing the time and effort required to correct the failure.

Four new Texas Instruments' Power+™ Control devices that are well-suited for ABS control applications are the TPIC46L01/02 (6-channel) and TPIC44L01/02 (4-channel). These power ICs are low-side pre-FET drivers that provide serial and parallel interfaces. Each predriver can control either Power+ Arrays™ devices or discrete power FETs allowing the system designer the flexibility to select the power output stage that best fits the system's load requirements.

An ABS control block diagram is shown in Figure 1. Some of the typical inputs for an ABS control system are front and rear wheel speeds, steering rate and position, and an acceleration switch. Typical loads of these applications are a pump motor, LEDs/lamps, and ABS solenoids. The pump motor is responsible for providing the fluid pressure for the brakes. The lamps/LEDs are used in the warning light to indicate proper function of the ABS system. Focusing on the ABS solenoids, the TPIC46L01/02 and TPIC44L01/02 provide fault protection and isolation to drive the discrete FETs for flexible control of these loads. The ABS solenoids are enabled/disabled by means of a fail-safe relay switch if the ABS controller malfunctions. The TPIC46L01/02 and TPIC44L01/02 receive pulse-width-modulated (PWM) signals from the ABS controller to turn the solenoids on and off to control the brakes, hence pulsing the brakes to prevent skidding. The scope of this application brief will discuss the 6-channel control of an ABS application using the TPIC46L01/02. The last section of the brief will expand on the implementa-

SYSTEM BENEFITS

- Design flexibility to select power output stage that matches system load requirements
- Fault diagnostics to increase fault isolation capability
- Serial and parallel interfaces to increase control flexibility

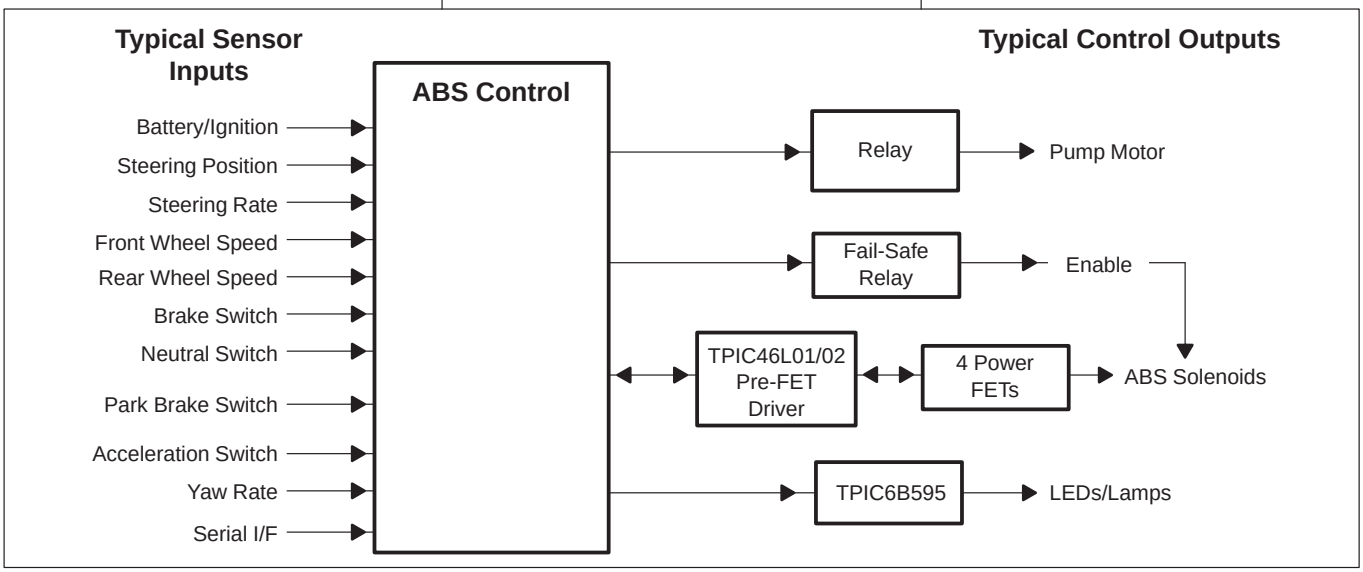

Figure 1. ABS Control Block Diagram

Application Brief

tion of the 4-channel control with the TPIC44L01/02.

Using the TPIC46L01/02 for ABS Control

One of the key factors in achieving optimal switching performance is the option to operate in either serial or parallel mode. The microcontroller can use the parallel control interface in applications where real-time control is required. Likewise, the serial interface can be used for control in applications where the response time is not as critical and the pin count needs to be minimized. In this application, control data will be transferred via the serial interface to the microcontroller. This closes the loop between the predriver and microcontroller to accomplish the communication of output fault data back to the controller. Multiple predrivers may be cascaded to minimize system interconnects. When cascading the predrivers, serial data is input to the device and is transferred out the serial data output (SDO) terminal following the fault data.

The TPIC46L01/02 also provide gate drive and protection necessary to switch discrete FETs used for high current requirements. The gate drive capability is well-suited for the typical ABS control application requiring from 3–8 A of continuous current. The protection comes in the form of real-time fault indicators through a fault interrupt line ($\overline{FLT}$) which serves as a flag to the microcontroller. The faults include over/under-battery-voltage shutdown and open/shorted-load detection. The TPIC46L02 enters a low duty cycle PWM state when encountering a shorted/open-load condition whereas the TPIC46L01 disables all gate outputs.

Serial data transfer

The interfaces responsible for proper serial input data transfer (see Figure 2) are chip select ($\overline{CS}$), serial clock (SCLK), serial data input (SDI) and SDO. To enable a serial data input transfer, the $\overline{CS}$ is brought low while the SCLK is also low. At this time, the serial data register will contain the current fault status while the parallel register remains latched in its previous condition and is unaffected. The most significant bit (MSB) of fault data, the over-battery-voltage bit, is immediately available on the SDO once $\overline{CS}$ goes low. As the first low-to-high transition of SCLK occurs, the new data on the SDI is shifted in most significant bit first. The

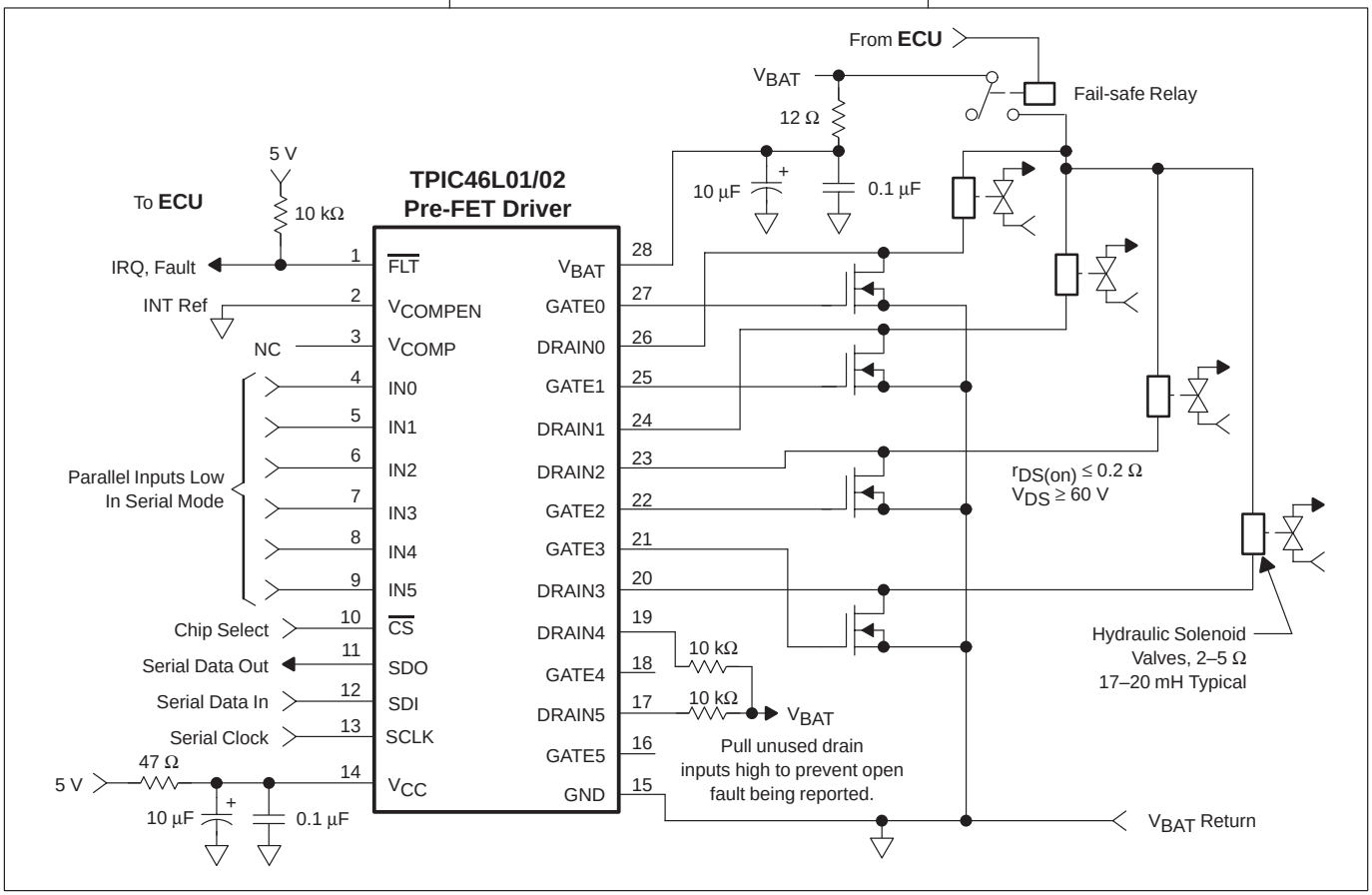

Figure 2. Circuit Schematic of the TPIC46L01/02 Pre-FET Driver and Four Discrete FETs

next bit of fault data, the under-battery-voltage bit, is available on SDO as SCLK transitions from high to low.

This sequence of events continues for eight consecutive SCLK pulses. On the falling edge of the seventh SCLK, the last bit of fault data (FLT0) is available on the SDO port. The final sequence begins with the rising edge of the eighth SCLK transferring the last bit of input data, BIT0, into the serial register. It is then complete on the falling edge of the eighth SCLK when the most significant bit of the input data is made available on the SDO. This last bit of data on the SDO is important only when cascading two or more devices. In this case, it is the first bit of input data for the SDI of the second device.

To avoid erroneous data transfer, three key operations must be performed. The first is that there must always be exactly eight SCLK pulses or a multiple of eight when two or more devices are cascaded. The second is that $\overline{CS}$ must be taken high after the SCLK transitions low. The rising edge of $\overline{CS}$ transfers the last six bits of the new data from the serial register to the gate outputs while at the same time re-enabling fault detection. The last is the parallel inputs must be held low or left unconnected when using the serial interface to control the outputs.

Parallel data transfer

Parallel data transfer is enabled by applying input control data to each respective parallel input (IN0–IN5) to asynchronously switch the gate outputs (GATE0–GATE5). The channel is enabled with a logic "1" and disabled with a logic "0". The parallel input port and serial control data are OR'ed in the output control register to allow either interface to control the gate outputs. While the serial interface is not required for parallel control, it is still available to transfer fault data back to the microcontroller.

Operational characteristics of ABS

Most ABS systems have a high-side fail-safe switch and low-side activation switches. The low-side switches are usually implemented using FET devices. The TPIC46L01/02 offer a parallel input interface for real-time control of the gate outputs to the FETs. These devices also provide a serial interface for fault isolation and serial control of the gate outputs.

For ABS application, the serial interface will be used for both output control and fault isolation. A serial peripheral type interface (SPI) (see Figure 2) is used to connect the predriver to the microcontroller inputs. Control data is input to the SDI port to enable or disable an output. A "0" will disable the output and a "1" will enable it. Figure 3 shows an example waveform of enabling channels 0–3 of the device. Trace 1 shows the SCLK; trace 2 shows the $\overline{CS}$; trace 3 shows the SDI high during the SCLK pulses 5–8; and trace 4 shows the corresponding gate drive output for GATE0.

The drain voltage and current limitations of the power FETs comprising the output stage are governed by the characteristics of the ABS solenoids. Figures 4a and 4b show the waveforms for the output stage and the FET for channel 0. The drain current at the time of turn-on can be seen in trace 3 of Figure 4a and the gate drive output (GATE0) in trace 2. The battery voltage and the solenoid inductance are two factors that affect the amount by which the drain current will increase. The slight perturbation in the rising slope is caused by the inductance change as the solenoid armature pulls in to open the valve. The current then continues to rise until the maximum value is reached, a result of the solenoid resistance.

Once the solenoid has turned off, the magnetic field collapses inducing a voltage at the DRAIN0 node of the power transistor. Figure 4a has been expanded ten times at the point of turn off to illustrate the inductive transient when the gate turns off. The result can be seen in Figure 4b. The drain current (DRAIN0) for the off time can be seen in trace 3 of Figure 4b. As the drain current decays to zero, the power transistor absorbs the energy stored in the solenoid inductance. Trace 4 of Figure 4b illustrates the clamping of the induced voltage at approximately 55 V to 60 V.

The clamping of the induced voltage just described is better known as the act of snubbing. Snubbing is necessary in order to dissipate the energy stored in the solenoid which could otherwise damage the power transistor by exceeding its maximum drain-to-source voltage rating. A delay time of

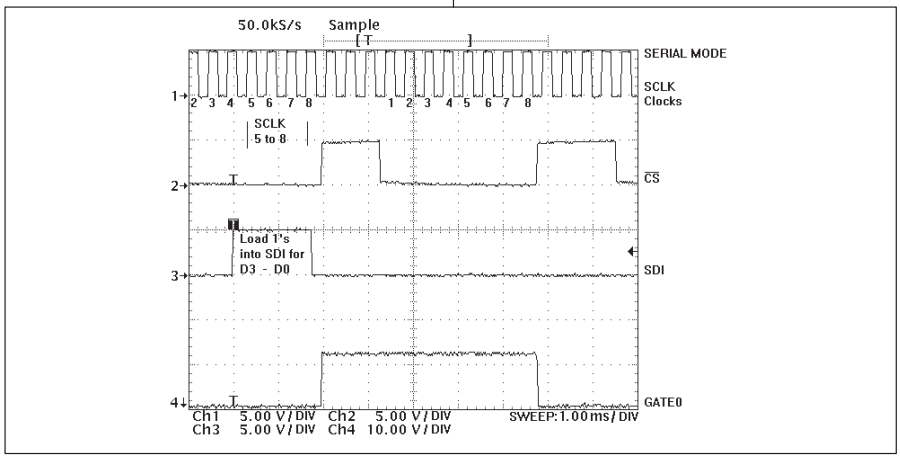

Figure 3. Enabling Output Channels 0–3

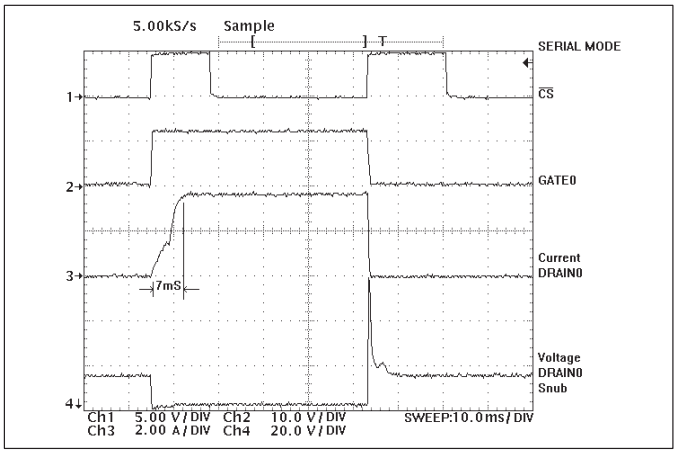

Figure 4a. Power During On Time

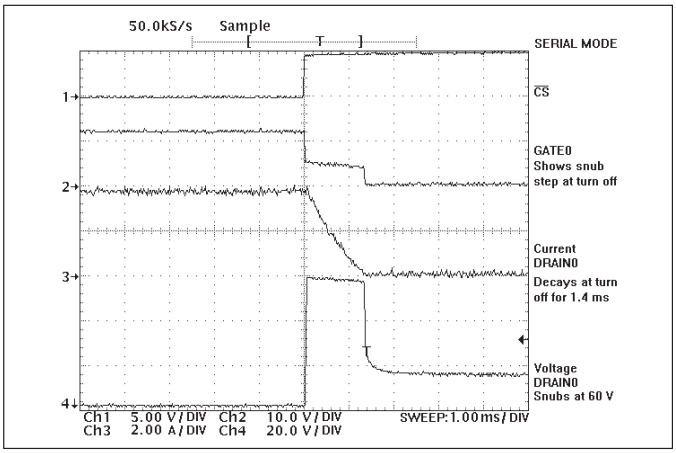

Figure 4b. Power During Off Time

approximately 1.4 ms occurs before the gate turns off completely. The drain voltage of the power transistor is monitored by the predriver to detect the inductive transient as well as other faults. The drain inputs complete an internal clamp circuit used to pull the gate up and accomplish the snubbing. An example of the snub can be seen in trace 2 of Figure 4b.

Fault Isolation

To ensure that errors in an ABS system do not go unnoticed, high safety standards are a requirement in maintaining the proper level of operation. The TPIC46L01/02 provides the capability to detect the various fault conditions mentioned earlier. The detection of these conditions are done in conjunction with the $\overline{FLT}$ line. A fault condition results in the predriver notifying the microcontroller of the error by going low.

The microcontroller can then check the fault data to know which output is operating at unsatisfactory conditions. Figure 5 illustrates a shorted-load condition. In this case, channel 0 is open and channel 3 (trace 4) is shorted. Fault data is constantly updated as the conditions occur. The loads are monitored while $\overline{CS}$ remains high to disable the serial interface. The most recent fault data is locked in the fault register as $\overline{CS}$ goes low. It is then available on the SDO at each high-to-low transition of SCLK.

Fault availability for the TPIC46L01 and the TPIC46L02 are slightly different. For the TPIC46L01, the microcontroller is immediately flagged by the fault line when the fault occurs (see Figure 6) and is available on the SDO port whenever $\overline{CS}$ transitions low to enable the serial interface. The gate output then turns off after 60 ms and remains off until the input is turned off and back on.

The TPIC46L02 captures the most recent fault condition. The fault that is that will be reported in the serial data output information. The fault interrupt ($\overline{FLT}$) will remain active (see Figure 7) until cleared by $\overline{CS}$. When a shorted-load fault occurs, the gate drive output goes into a low duty cycle PWM mode

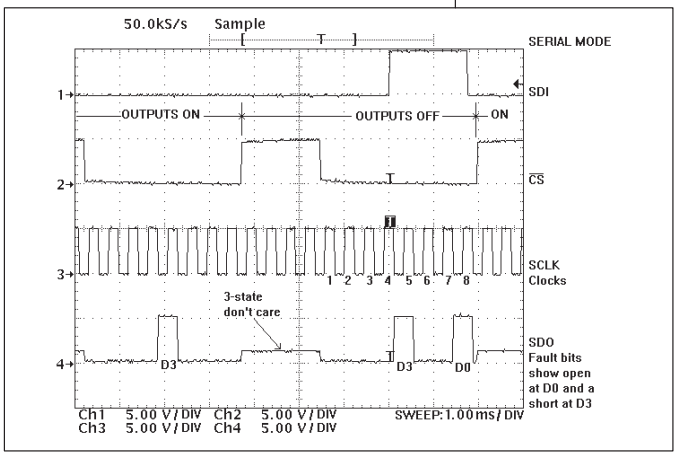

Figure 5. Open/Short-Fault Conditions

Note that FLT0 occurs in the second byte of data.

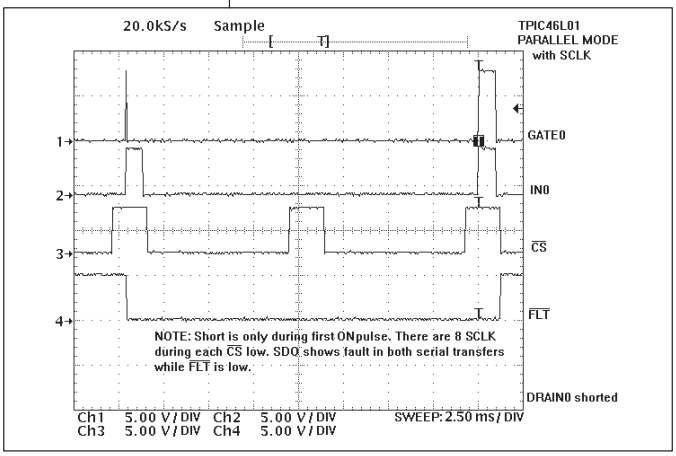

Figure 6. Fault is Captured

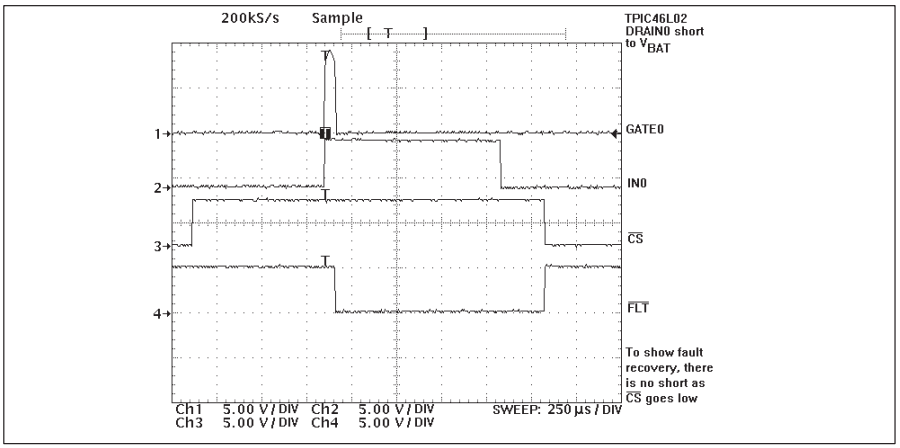

Figure 7. Fault Clears

and will remain there as long as the output is enabled and the fault condition is still present. The $\overline{FLT}$ is refreshed when $\overline{CS}$ transitions low after the fault has been cleared.

As stated earlier in the serial data transfer section, care must be taken to ensure that eight bits of data are clocked into the SDI port if $\overline{CS}$ transitions low when using either the serial or parallel port for control. Less than eight bits of data may result in unknown data being transferred into the output control register as $\overline{CS}$ transitions high. To illustrate the fault status in trace 4 of Figure 5, there are two bytes of fault data shown; one indicating a short present at channel 3 (BIT3) and the other indicating an open at channel 0 (BIT0). As $\overline{CS}$ goes low, the bit representations are: left to right, over-battery (MSB), under-battery, and FLT5 to FLT0 (LSB).

Open-load condition

The test for an open load is performed only when the output transistor is off. The test is not enabled until the drain has had a sufficient amount of time to stabilize. The stabilization time is set at 60 ms, after which a fault flag is issued to the microcontroller if an open-drain has been detected. The means of detection are done by placing a 60 mA current source on the drains of each of the FET's. An open drain results in sufficient current sink to pull the drain of the transistor below the 1.25 V reference threshold. As can be seen in Figure 2, normal operation is defined by the load pulling the drain high. False reporting of open load conditions would result if the previous condition is not met.

Figure 8a illustrates the result of an open load at channel 0. Trace 4 shows the bit position for channel 0 with the fault information high indicating a shorted/open-load condition. At this time the $\overline{FLT}$ line goes high notifying the microcontroller of the error (trace 3).

Shorted load condition

The test for a shorted solenoid is performed when the output transistor is on. Once the output is turned on, a delay of 60 ms is used to allow the output to stabilize. A drain voltage of 1.25 V is used as a reference to determine if an over-current or shorted-load condition exists. If the drain voltage of interest is greater than the reference of 1.25 V, the microcontroller is notified by the $\overline{FLT}$ line transitioning low. Trace 4 of Figure 8b illustrates the gate of the output transistor controlled by channel 0 (BIT0) shorted to V_{BAT}.Although not shown in the figure, it is understood that the serial input is held high for the duration of SCLK pulses 5–8. BIT0 (trace 3) of the SDO transitions high to indicate a fault as the output is commanded to turn on.

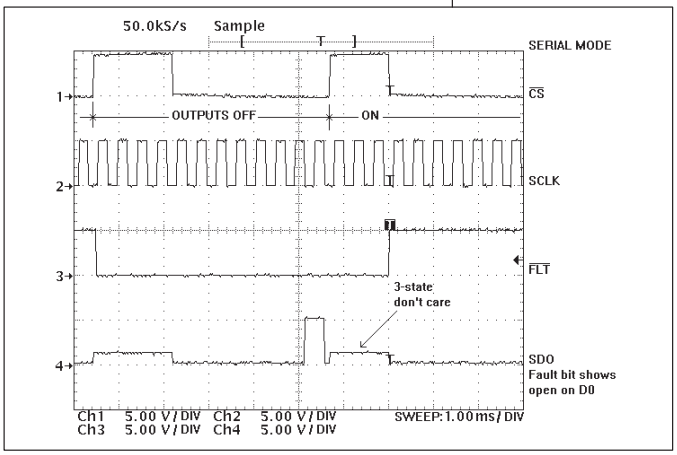

Figure 8a. Open-Load Condition

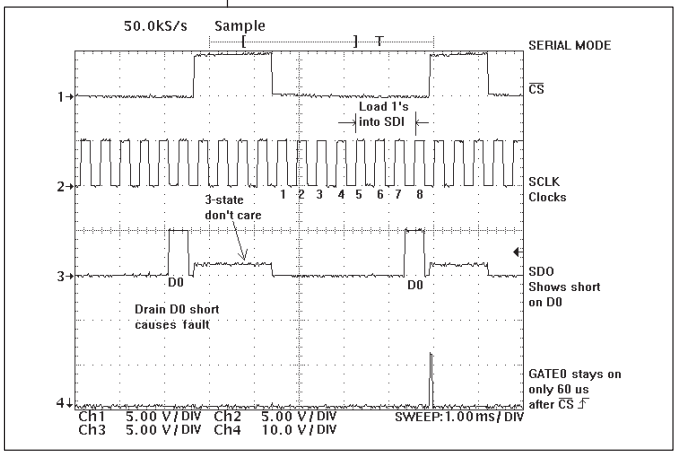

Figure 8b. Shorted-Load Condition

A common concern associated with shorted-load conditions is the risk of exceeding the maximum power dissipation ratings of the output transistor and causing permanent damage. The TPIC46L01 limits the on-time of the transistor to 60 ms if this fault occurs. It limits the on–time by disabling the gate output until the microcontroller turns it back on. An example is shown in trace 4 of Figure 8b. The TPIC46L02 protects the transistor against the same fault condition in a different manner. It transitions into a low duty cycle PWM state to protect the FET from overheating.

Over/Under-battery-voltage detection and shutdown

In addition to open-load and shorted-load conditions, the predriver monitors the battery voltage to protect the load and power transistor from over-battery conditions. To protect the output transistor and load from thermal stress, the under-battery voltage threshold is set at 4.8V. This safeguard would help to prevent enabling of the power FETs in the event the battery voltage is too low. The over-battery voltage detection threshold is set at 34 V. An example of this condition is a loose battery connection that may result in a voltage transient. Regardless of the battery voltage condition, an error results in all gate outputs being disabled until the problem is corrected. The act of disabling the gate outputs prevents erroneous fault data from being reported. Trace 4 of Figure 9 shows an under-battery voltage fault condition.

Internal/External fault reference

The TPIC46L01 and TPIC46L02 detect fault conditions by comparing the output channel's drain voltage to a threshold reference. The internal reference, as stated earlier, is set at 1.25 V and is monitored 60 ms after a gate transition. It is selected by grounding the voltage compare enable (V_{COMPEN}, pin 2, Figure 2). However, depending on system requirements, a reference level may need adjusted. The various power transistors capable of driving ABS loads have different on-resistances which may require a different level of detection. The external reference capability is enabled by pulling the V_{COMPEN} pin high and using the voltage compare (V_{COMP}, pin 3) as the external reference. For example, an external reference set at 1.5 V would give a maximum allowable drain current of:

$$I_{D(trip)} = V_{COMP} / r_{DS(on)}$$
$$= 1.5\ V / 0.2\ \Omega = 7.5\ A$$

where the on-resistance, $r_{DS(on)}$, is for a 0.2 Ω discrete FET.

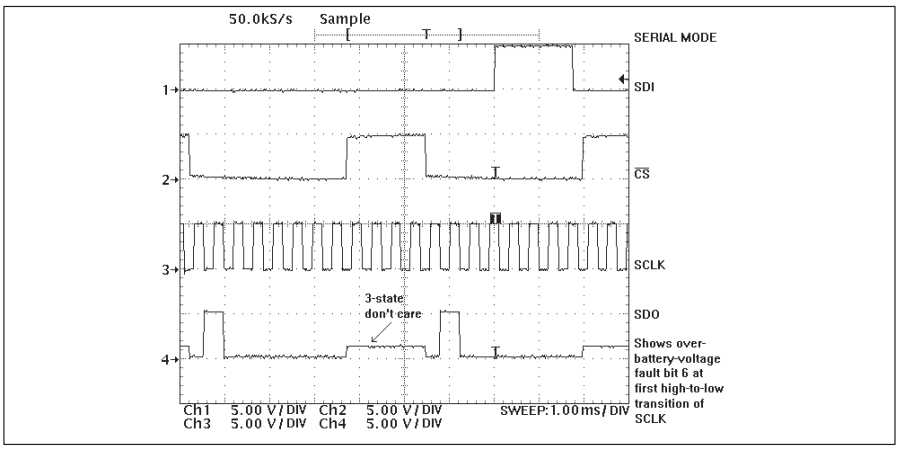

Figure 9. Under-Battery Fault Condition

TPIC44L01 and TPIC44L02

ABS system control is also well-suited for the TPIC44L01 and TPIC44L02, 4-channel devices. The serial mode operation is advantageous for a 4-channel application such as this. Functional differences between the 4 and 6-channel low-side pre-FET drivers are minimal and present the flexibilty necessary for different applications.

Increasing system throughput

System throughput is an area of interest when considering the control of solenoid operated valves for an ABS system. Cascading the TPIC44L01/02 makes it possible to achieve nearly double the system throughput when operating in the serial mode versus the parallel mode. This is due to the absence of the over/under-battery-voltage bits. The 4-channel devices transmit and receive at a minimum of 4-bit serial words per device.

The scheme of data transmission for two 4-channel cascaded devices is similar to that for 6-channel devices. Control information is input to the SDI of the first device. Fault data transfers from the SDO of the first device into the SDI of the second device. Control data for the second device follows the fault data in the serial transfer. When $\overline{CS}$ transitions high, all 8 bits of fault data have been transferred out the SDO of the second device.

The first bit of fault data (FLT3) available is the most significant bit (MSB). This bit represents a shorted/open-load fault for output channel 3. The remaining bits are for channel 2–0 and are represented by FLT2–0, respectively. An example of 8-bit serial word operation can be seen in Figure 10.

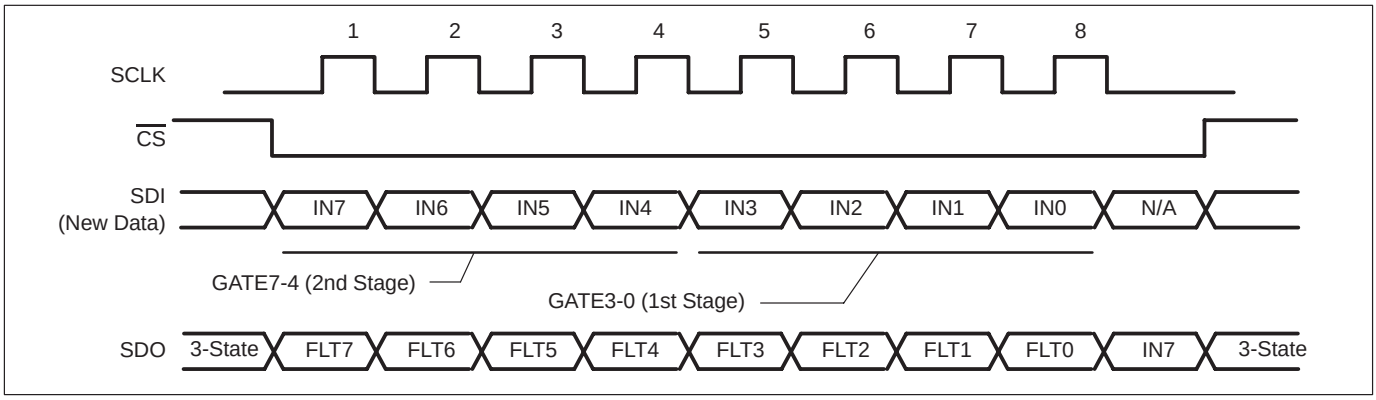

Figure 10. 8-Bit Serial Word Operation

As with the 6-channel devices, the notification of an error for the microcontroller is accomplished by the $\overline{\text{FLT}}$ line. It provides the information necessary for real-time control of the outputs.

An additional feature on the 4-channel devices is an active low reset line ($\overline{\text{RESET}}$). The $\overline{\text{RESET}}$ line clears the fault register, the control register, and the fault interrupt line when transitioned low. This provides the means to disable the outputs and clear the device by toggling a single input.

Conclusions

The 6-channel, TPIC46L01/02, or the 4-channel, TPIC44L01/02, offer an enhanced approach to switching 3–8 A load current applications. These devices present an alternative for the designer to select a power output stage that better matches the load requirements than may be available when using an integrated device. The TPIC44L01/02 offers a serial input interface with the ability to increase system throughput by means of cascading two devices. Reset capabilities make it possible to disable the outputs in time-critical situations.

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