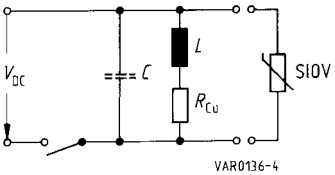
3 Application and design examples

3.1 Switching off inductive loads

The discharge of an inductor produces high voltages that endanger both the contact breaker (switching transistor and the like) and the inductor itself. According to equation 16 the energy stored in the coil is $^1/_2\ L\ i^2$. So, when the inductor is switched off, this energy charges a capacitor in parallel with the inductor (this capacitor can also be the intrinsic capacitance of the coil). Not allowing for the losses, and for $^1/_2\ C\ v^2 = {}^1/_2\ L\ i^2$, the values of figure 23 produce:

$$v^* = i^* \sqrt{\frac{L}{C}} = 1 \sqrt{\frac{0{,}1}{250 \cdot 10^{-12}}} = 20\,000\ \text{V}$$

To suppress this transient, a varistor is to be connected in parallel with the inductor as a fly-wheel circuit.



V_{DC} = 24 V
L = 0,1 H
R_{Cu} = 24 Ω
I = 1 A
C = 250 pF

Required switching rate = 10^6
Period = 10 s
Required protection level < 65 V

Figure 23 Limiting switching transients with a varistor as fly-wheel circuit

Operating voltage

The DC operating voltage is given as 24 V (cf. figure 23). If the possible increase in operating voltage is no more than 2 V, types with a maximum permissible DC operating voltage of 26 V should be chosen from the product tables to arrive at as low a protection level as possible. The types available in this category are

– disks S..K20
– SMDs CU....K20G2, CN....K20G
– hicaps SR.K20M...

Surge current

When it is cut off, the current through an inductor cannot change abruptly, so it flows across the varistor initially with the value of the operating current (here 1 A) , then decaying towards zero following an exponential function.

The simplest ways of determining the current duration are simulation or measurement ($\tau = t^*_r$).

The time constant can also be calculated to an approximation with equation 13.
Here the varistor resistance of voltage class K20 is calculated for 1 A. As the protection levels of the various type series do not differ much, the S10K20 has been chosen arbitrarily to determine the resistance (the voltage is taken from the appropriate *V/I* characteristics).

$$R_{SIOV} = \frac{55\ V}{1\ A} = 55\ \Omega$$

So τ according to equation 13 is

$$\tau = t^*_r = \frac{0{,}1\ H}{24\ \Omega + 55\ \Omega} \approx 1{,}3\ ms$$

For S10K20 with t^*_r = 1,3 ms and 10^6 load repetitions, one can derive

i_{max} = 3 A > i^* = 1 A

from the derating curves.

Taking this result, one should check whether other types with lower current ratings satisfy the selection criterion:

S05K20: i_{max} = 0,5 A < i^* = 1 A
S07K20: i_{max} = 1,4 A > i^* = 1 A

So the selection criterion of equation 9 is met by SIOV-S07K20 and all types with higher current ratings.

If an SMD is to be used, this can be selected from either the SIOV-CU or SIOV-CN ranges.

SIOV-CU: CU4032K20G2 is the electrical equivalent of S07K20.
SIOV-CN: CN1206K20G, with i_{max} = 1,5 A > i^* = 1 A fulfills the selection criteria.

Energy absorption

The maximum energy absorption capacity of SIOV-S07K20 for t^*_r =1,3 ms, i_{max} = 1,4 A and 10^6 repetitions according to equation 17 is

$W_{max} = v_{max} \cdot i_{max} \cdot t_{r\,max}$ = 60 · 1,4 · 0,0013 = 0,11 J (with $t_{r\,max} = t^*_r$ according to 2.5.3)

According to equation 16 the varistor must in the worst case absorb an energy of

$W^* = {}^1/_2\ L\ i^{*2} = {}^1/_2 \cdot 0{,}1\ H \cdot 1\ A^2 = 0{,}05\ J < W_{max} = 0{,}11\ J$

per switching cycle. Thus SIOV-S07K20 and CU4032K20G2 also satisfy the selection requirement of equation 10.

For CN1206K20G the result is W_{max} = 58 · 1,5 · 0,0013 = 0,11 J > 0,05 J.
This varistor is therefore also suitable.

Average power dissipation

According to equation 18, applied energy of 0,05 J every 10 s produces an average power dissipation of

$$P^* = \frac{W^*}{T^*} = \frac{0{,}05}{10} = 0{,}005 \text{ W}$$

The product table shows a maximum dissipation capability of 0,02 W for SIOV-S07K20 and CU4032K20G2. So on this point too, the choice is correct (equation 11).

For the sake of completeness, the minimum permissible time between two applications of energy is calculated (equation 19):

$$T_{min} = \frac{W^*}{P_{max}} = \frac{0{,}05 \text{ J}}{0{,}02 \text{ W}} = 2{,}5 \text{ s}$$

For CN1206K20G, with P_{max} = 0,008 W the result is

$$T_{min} = \frac{W^*}{P_{max}} = \frac{0{,}05 \text{ J}}{0{,}008 \text{ W}} = 6{,}2 \text{ s}$$

Maximum protection level

The *V/I* curve for S07K20 and/or CU4032K20G2 shows a protection level of 60 V at 1 A for the worst case position in the tolerance field (PSpice supplied by S+M: TOL = +10).
The protection level for CN1206K20G is 55 V.
This means that all three types meet the requirement for a protection level < 65 V.

The hicap varistors SHCV-SR.K20... also satisfy all the selection criteria. Their use can have a positive effect as far as contact erosion and RFI are concerned. They also mean a reduction of the maximum protection level to 50 V.

3.2 CE conformity

A wide range of legislation and of harmonized standards have come into force and been published in the field of EMC in the past few years. In the European Union, the EMC Directive 89/336/EEC of the Council of the European Communites has come into effect on the 1st of January 1996. As of this date, all electronic equipment must comply with the protective aims of the EMC Directive. The conformity with the respective standards must be guaranteed by the **manufacturer or importer** in the form of a declaration of conformity. A CE mark of conformity must be applied to all equipment [1].

As a matter of principle, all electrical or electronic equipment, installations and systems must meet the protection requirements of the EMC Directive and/or national EMC legislation. A declaration of conformity by the manufacturer or importer and a CE mark are required for most equipment. Exceptions to this rule and special rulings are described in detail in the EMC laws.

[1] Kohling, Anton “CE Conformity Marking”
ISBN 3-89578-037-5, Ordering code: A19100-L531-B666

New, harmonized European standards have been drawn up in relation to the EEC's EMC Directive and the national EMC laws. These specify measurement techniques and limit values or severity levels, both for interference emission and for the interference susceptibility (or rather, immunity to interference) of electronic devices, equipment and systems.

The subdivision of the European standards into various categories (cf. table 1) makes it easier to find the rules that apply to the respective equipment.
The generic standards always apply to all equipment for which there is no specific product family standard or dedicated product standard.

Adherence to the standards for electromagnetic compatibility (EMC) is especially important.
These are:

– Interference emission EN 50081
– Immunity to interference EN 50082

Whereas regulations concerning maximum interference emission have been in existence for some time, binding requirements concerning immunity to interference have only come into existence since 1996 for many types of equipment. In this respect, in addition to having an optimum price/performance ratio, SIOV varistors have proved themselves to be a reliable solution for all requirements concerning overvoltages:

- ESD (electrostatic discharge)
- Burst (fast transients)
- Surges, high-energy transients

The basic standards contain information on interference phenomena and general measuring methods.

The following standards and regulations form the framework of the conformity tests:

Table 1

EMC standards		Germany	Europe	International
Generic standards define the EMC environment in which a device is to operate according to its intended use				
Emission	residential industrial	DIN EN 50081-1 DIN EN 50081-2	EN 50081-1 EN 50081-2	—
Susceptibility	residential industrial	DIN EN 50082-1 DIN EN 50082-2	EN 50082-1 EN 50082-2	—

Table 1 (continued)

EMC standards	Germany	Europe	International

Basic standards
describe physical phenomena and measurement techniques

Basic principles		DIN VDE 0843	EN 61000	IEC 1000
Measuring equipment		DIN VDE 0876		CISPR 16-1
Measuring methods	emission	DIN VDE 0877		CISPR 16-2
	susceptibility		EN 61000-4-1	IEC 1000-4-1
Harmonics		DIN VDE 0838	EN 60555-2	IEC 1000-3-2
Interference factors				
e. g.	ESD	DIN VDE 0843-2	EN 61000-4-2	IEC 1000-4-2
	EM fields	DIN VDE 0843-3	EN 61000-4-3	IEC 1000-4-3
	Burst	DIN VDE 0843-4	EN 61000-4-4	IEC 1000-4-4
	Surge	DIN VDE 0843-5	EN 61000-4-5	IEC 1000-4-5

Product standards
define limit values for emission and susceptibility

EMC standards		Germany	Europe	International
ISM equipment[2)]	emission	DIN VDE 0875 T11	EN 55011	CISPR 11
	susceptibility	1)	1)	1)
Household	emission	DIN VDE 0875 T14-1	EN 55014-1	CISPR 14-1
appliances	susceptibility	DIN VDE 0875 T14-2	EN 55014-2	CISPR 14-2
Lighting	emission	DIN VDE 0875 T15-1	EN 55015-1	CISPR 15
	susceptibility	DIN VDE 0875 T15-2	EN 55015-2	IEC 3439
Radio and	emission	DIN VDE 0872 T13	EN 55013	CISPR 13
TV equipment	susceptibility	DIN VDE 0872 T20	EN 55020	CISPR 20
High-voltage				
systems	emission	DIN VDE 0873	EN 55018	CISPR 18
IT equipment[3)]	emission	DIN VDE 0878	EN 55022	CISPR 22
	susceptibility	DIN VDE 0878	EN 55022	CISPR 22
Vehicles	emission	DIN VDE 0879	EN 72245	CISPR 25
	susceptibility	DIN VDE 0839		ISO 11451/S2

1) Is governed by the safety and quality standards of the product families
2) Industrial, scientific and medical devices and equipment
3) Information technology facilities

Table 1 (continued)

The following table shows the most important standards in the field of immunity to interference.

Standard	Test characteristics	Phenomena
Conducted interference		
EN 61000-4-4 IEC 1000-4-4	5/50 ns (single pulse) 15 kHz burst	Burst Cause: switching processes
EN 61000-4-5 IEC 1000-4-5	1,2/50 µs (open-circuit voltage) 8/20 µs (short-circuit current)	Surge (high-energy transients) Cause: lightning strikes mains lines, switching processes
EN 61000-4-6 (ENV 50141) IEC 801-6	1 V, 3 V, 10 V 150 kHz to 80 MHz	High-frequency coupling Narrow-band interference
Field-related interference		
EN 61000-4-3 (ENV 50140) IEC 801-3	3 V/m, 10 V/m 80 to 1000 MHz	High-frequency interference fields
Electrostatic discharge (ESD)		
EN 61000-4-2 IEC 1000-4-2	Up to 15 kV figure 24	Electrostatic discharge

The IEC 1000 or EN 61000 series of standards are planned as central EMC standards into which all EMC regulations (e. g. IEC 801, IEC 555) are to be integrated in the next few years.

3.2.1 ESD

The trend to ever smaller components and lower and lower signal levels increases the susceptibility of electronic circuits to interference due to electrostatic disturbances. Simply touching the device may lead to electrostatic discharge causing function disturbances with far-reaching consequences or to component breakdown. Studies have shown that the human body on an insulated ground surface (e. g. artificial fiber carpeting), can be charged up to 15 kV.
In order to safeguard the immunity to interference and thus ensure CE conformity, measures are needed to prevent damage due to **e**lectro**s**tatic **d**ischarge (ESD). This applies to both the circuit layout and to selection of suitable overvoltage protection.

EN 61000-4-2 describes the test procedures and specifies severity levels:
Figure 24 shows the discharge circuit, figure 25 the waveform of the discharge current with an extremely short rise time of 0,7 to 1,0 ns and amplitudes of up to 45 A. Secondary effects caused by this edge steepness are high electrical and magnetic fields strengths.
In the ESD test, at least 10 test pulses of the polarity to which the device under test is most sensitive are applied.

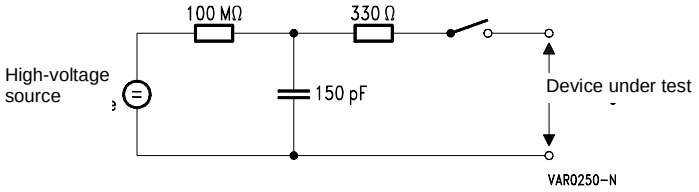


Figure 24 ESD discharge circuit according to EN 61000-4-2

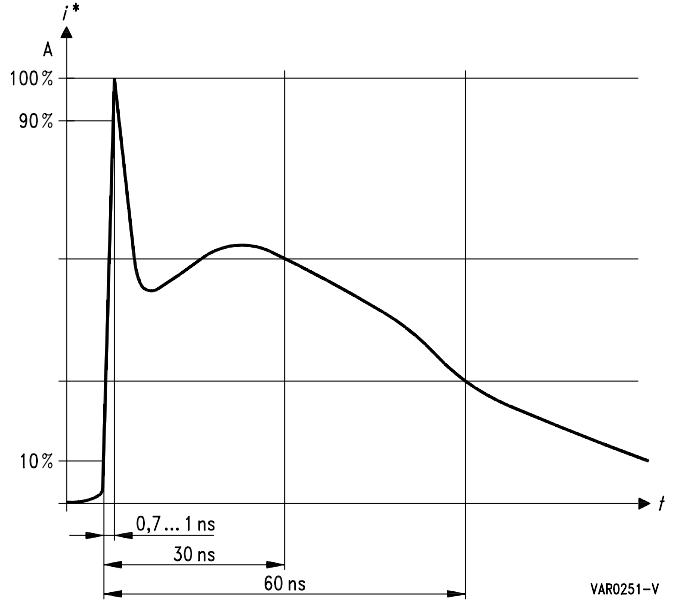


Figure 25 ESD discharge current according to EN 61000-4-2

For this reason, suitable overvoltage protection elements must meet the following requirements:

– response time < 0,5 ns
– bipolar characteristics
– sufficient surge current handling capability
– low protection level

In addition, the following requirements are desirable:

– smallest possible component size
– SMD design
– high capacitance values for RF interference suppression, or low capacitance values for systems with high-speed data transmission rates, respectively
– wide operating voltage range
– high operating temperature

All these requirements are optimally fulfilled by SIOV multilayer varistors (CN series). The extremely low inductance of their construction reduces the response time to < 0,5 ns. Consequently, in order to utilize this advantage to the full, the lowest possible connection inductance is required.

The fields of application are, in particular:

– cordless and cellular phones (“handies”)
– SCART sockets
– data transmission lines
– interfaces such as RS232, CENTRONICS
– PC (keyboard, mouse, printer ports etc.)
– LANs, modems, sensors
– interface circuits

Often, for example in SCART sockets of TV sets and video recorders, signal lines are connected with two Z diodes in serial and opposing polarity and a decoupling capacitor. Replacing these three components by a multilayer varistor leads to considerable cost and space savings (figure 26).

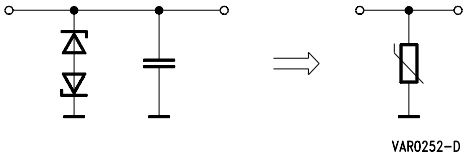


Figure 26 A multilayer varistor can replace three components

The adaptation to the capacitance values of the decoupling capacitor can be achieved by correct selection of the model and/or the voltage class:

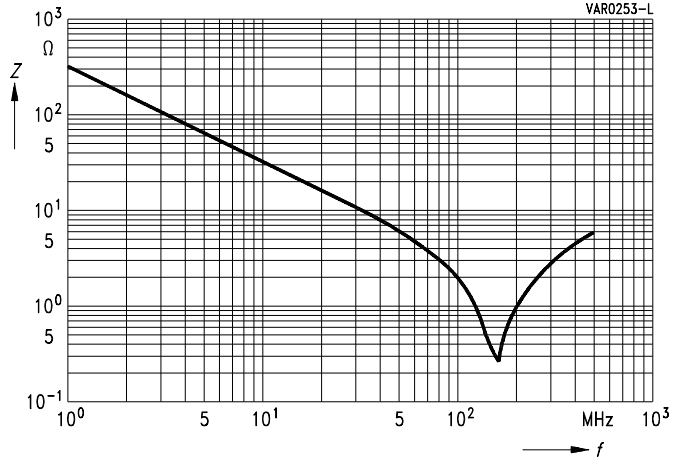
- higher capacitance values are achieved by selecting a larger model,
- lower capacitance values are achieved by selecting a smaller model, or, where this is not possible, a higher voltage class.

In addition, multilayer varistors with defined capacitance tolerances are available:

LC	**L**ow **C**apacitance	(C < defined value)
CC	**C**ontrolled **C**apacitance	(C within a defined tolerance band)
HC	**H**igh **C**apacitance	(C > defined value)

Figures 27a and 27 b show the typical RF behavior of multilayer varistors with a capacitance value which remains practically constant over a wide frequency range.

a



b

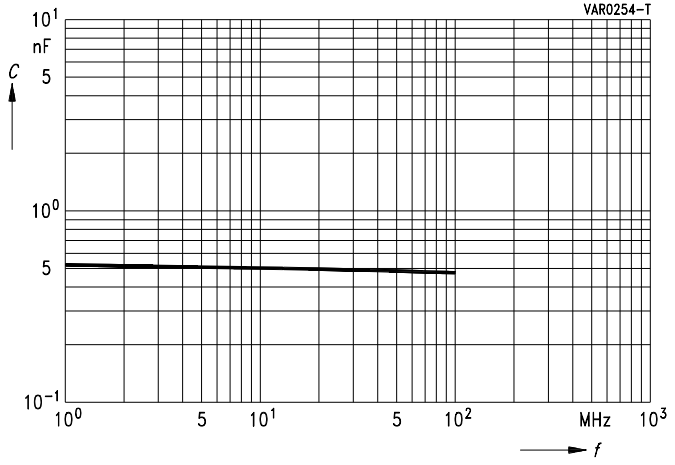


Figure 27 Typical frequency response of the impedance (a) and the capacitance (b), using the multilayer varistor SIOV-CN0805M6G as an example

3.2.2 Energy of an ESD pulse

EN 61000-4-2 specifies 15 kV as the highest charging voltage (severity level 4, air discharge) for the 150 pF discharge capacitor according to figure 24.

This means that the stored energy is

$W^* = 0{,}5 \cdot C \cdot V^2 = 0{,}5 \cdot 150 \cdot 10^{-12} \cdot 15^2 \cdot 10^6 < 0{,}02$ J

The 330-Ω resistor limits the surge current to a maximum of

$$\hat{i}^* = \frac{V^*}{R} = \frac{15\,000\ [V]}{330\ [\Omega]} \approx 45\ \text{A}$$

If this surge current is to be handled by a multilayer varistor, then, according to equation 12, the effect of the varistor on this value of the current amplitude is negligible.

For CN0805M6G, for example, this means that:

$$\hat{i}^* = \frac{V_s - V_{SIOV}}{Z_{source}} = \frac{15\,000\ [V] - 45\ [V]}{330\ [\Omega]} \approx 45\ \text{A}$$

By transforming the discharge current (figure 25) into an equivalent rectangular wave, we obtain $t^*_r \approx 40$ ns.

No value can be deduced from the derating curves for such an extremely short current flow time.

The energy absorption of multilayer varistors during ESD discharges lies in the region of μJ.

For the SIOV-CN0805M6G, for example, according to equation 15 this means that:

$W^* = \hat{V}^* \hat{i}^* t^*_r = 45 \cdot 45 \cdot 40 \cdot 10^9 = 80$ μJ

Thus one can expect the largest part of the energy content of the ESD pulse to be absorbed by the 330-Ω discharge resistor.

If EN 61000-4-5 (surge voltage) is taken into consideration when selecting the varistor, it can be assumed that, where applicable, ESD specifications are also covered by the varistor. Due to the steep edge of the ESD pulse, the mechanical construction of a device is of great importance for the test result. The ESD varistor selection should therefore always be verified by a test circuit.

3.2.3 Burst

According to EN61000-4-4 (IEC 1000-4-4), burst pulses are low-energy transients with steep edges and high repetition rate. Thus, for equipment to pass burst testing successfully, design and construction are as critical as the choice of the varistor. If EN 61000-4-5 has been taken into account when selecting varistors, they will normally also handle the burst pulse energy without any problems. Due to the steepness of the pulse edges, the varistors must be connected in a way which keeps parasitic circuit inductance low. Our EMC laboratory in Regensburg will carry out tests on request (cf. 3.2.6).

3.2.4 Surge voltages

The immunity to interference against (high-energy) surge voltages is tested in accordance with EN 61000-4-5 (IEC 1000-4-5). The overvoltage is generated using a hybrid generator such as specified in EN 61000-4-5 and is then coupled in via the individual leads of the device under test.

The severity level of the test (i.e. the charging voltage and thus the energy content) is defined in relation to the installation conditions. In most cases, the respective product standards demand 5 positive and 5 negative voltage pulses.

Varistors suitable for 230 V and 400 V mains are given in tables 2a and 2b, in each case as a function of the required severity levels and the source impedance. An impedance of 2 Ω is used in the line-to-line test.

12 Ω is specified for the line-earth test:

The tables show that smaller components may be used.

Note:
Connection of varistors to earth may be subject to restrictions. This must be clarified with the respective authorization offices.

For all lines which do not serve to supply electricity, EN 61000-4-5 specifies 42 Ω as the generator impedance.

The extremely high suitability of SIOV varistors for ensuring immunity to interference can be seen in table 2a:

Even for test severity level 4 (4 kV via 2 Ω), the very cost-efficient model S20 (type S20K275) is adequate. Here the “overvoltage” of 4 kV is reduced to a maximum of 900 V.

Table 2a

		230 V rms					
		Connection via					
		2 Ω			12 Ω		
		10 load cycles			10 load cycles		
Severity level	kV	Type	i_{max} A	v_{max} V	Type	i_{max} A	v_{max} V
1	0,5	Overvoltage protection not required					
2	1	S07K275	135	820	S05K275	28	790
3	2	S10K275	590	920	S07K275	110	830
4	4	S20K275	1560	900	S07K275	270	850

Table 2b

		400 V rms					
		Connection via					
		2 Ω			12 Ω		
		10 load cycles			10 load cycles		
Severity level	kV	Type	i_{max} A	v_{max} V	Type	i_{max} A	v_{max} V
1	0,5	Test makes no sense					
2	1	S05K460	3	1000	S05K460	2	990
3	2	S10K460	360	1430	S05K460	60	1450
4	4	S20K460	1300	1530	S07K460	230	1410

Selection example

How to determine suitable varistors for each case covered by tables 2a and b is demonstrated by the example of the S20K275.

Operating voltage

According to IEC 38, from the year 2003 onwards the operating voltage tolerance in Europe will be 230 V ± 10%, i.e. a maximum operating voltage of 253 V can be expected. This means that only varistors of the voltage classes “K275” (or higher) may be selected.

Surge current

The surge current caused by the hybrid generator depends to a large extent on the load, i.e. on the varistor, in this case. It is easy to determine amplitude and current duration by simulation. Here, one should take into account that the greatest current flows across the varistor whose *V/I* characteristic is at the lower limit of the tolerance band.

In this case, the resulting current amplitude for S20K275 is approx. $\hat{i}^*$ = 1560 A, the current duration of the equivalent rectangular wave is < 20 µs. For 10 repetitions, the value of ($t_r \leq 20$ µs) i_{max} = 2500 A can be deduced from the derating curve for S20K275.

Since $i_{max} > \hat{i}^*$ the selection criterion for the surge current is fulfilled.

If no simulation is available, then the surge current has to be determined by a test circuit or by mathematical approximation.

The approximation solution (equation 12) results in:

$$i^* = \frac{V_s - V_{SIOV}}{Z_{source}} = \frac{4000 - 750}{2} = 1625\ \text{A} < i_{max}$$

A maximum value of 940 V is obtained from the *V/I* characteristic for the S20K275 at 2000 A; the lower tolerance limit will then be approx. 940 V – 20 %.

The current duration can be estimated on the basis of the fact that the hybrid generator produces a short-circuit surge current wave of 8/20 µs. Under load with a low-resistance varistor one can expect a waveform similar to that of the 8/20 µs wave, whose transformation into an equivalent rectangular wave has a t^*_r < 20 µs. Again this leads to a reading of i_{max} = 2500 A for 10 times in the derating curve. With i^* = 1625 A < i_{max} the selection criterion of equ. 9 is fulfilled. The difference between the results of this calculation and the simulation results is negligible.

Energy absorption

The energy absorption of the S20K275 varistor can be calculated directly by simulation.

It is possible to estimate the value by means of equation 15 (lower tolerance field limit):

$W^* = \hat{v}^* \hat{i}^* t^*_r = 750 \cdot 1625 \cdot 20 \cdot 10^{-6} = 24$ J

Minimum time interval between energy loads

The minimum time interval between loads to the S20K275 can be deduced from equation 19:

$$T_{min} = \frac{W^*}{P_{max}} = \frac{24\ J}{1\ W} = 24\ s$$

Protection level

The highest possible protection level, which the S20K275 will achieve, can be deduced from the + 10 % tolerance curve simulation. According to table 2a, the maximum voltage v_{max} is 900 V.

Similar results are obtained for a current of approx. 1600 A in the V/I characteristic curve field.

3.2.5 Interference emission

The switching off inductive loads can lead to overvoltages which may become sources of line interference as well as of inductively and/or capacitively coupled interference. This kind of interference can be suppressed using varistors connected as a fly-wheel circuit.

SHCV varistors are especially well-suited for radio-frequency interference suppression.

3.2.6 EMC systems engineering

S+M Components is your competent partner when it comes to solving EMC problems.

Our performance range covers
– systems for measuring and testing EMC
– shielded rooms for EMP measures
– anechoic chambers
– EMC consultation services and planning

For further details, please refer to the EMC Components Data Book (ordering no. B424-P2414-X-X-7600).

3.3 Protection of automotive electrical systems

3.3.1 Requirements

Electronic equipment must work reliably in its electromagnetic environment without, in turn, unduly influencing this environment. This requirement, known as electromagnetic compatibility (EMC), is especially important in automotive electrical systems, where energy of mJ levels is sufficient to disturb or destroy devices that are essential for safety. S+M Components has devised a wide range of special models matched to the particular demands encountered in automotive power supplies:

- extra high energy absorption (load dump)
- effective limiting of transients
- low leakage current
- jump-start capability (no varistor damage at double the car battery voltage)
- insensitive to reverse polarity
- wide range of operating temperature
- high resistance to cyclic temperature stress
- high capacitance for RFI suppression

S+M automotive varistors (SIOV-…AUTO) and SHCVs suit all these demands. They are specified separately in the product tables.

3.3.2 Transients

Standard ISO 7637-1 (DIN 40839, part 1), details “Conducted interference on supply lines in 12-V automotive electrical systems”. The toughest test for transient suppression is pulse 5, simulating load dump. This critical fault occurs when a battery is accidentally disconnected from the generator while the engine is running, e. g. because of a loose cable. Voltages of as much as 200 V can result, lasting for a few hundred ms with energy levels of up to 100 J. This worst case can be mastered with SIOV-AUTO varistors of the S20 series. The lower energy pulses 1 to 3 are equally covered.

3.3.3 Fine protection

Electronic components are often far apart, so EMC cannot be implemented with a central suppressor module alone. Instead one has to provide extra fine protection directly on the individual modules. Here energy absorption of a few Joules to some tens of Joules is adequate, meaning that lower rated and thus smaller components can be chosen, like the SMD series SIOV-CU/CN or SHCVs. Figure 28 illustrates a concept for suppression with varistors.

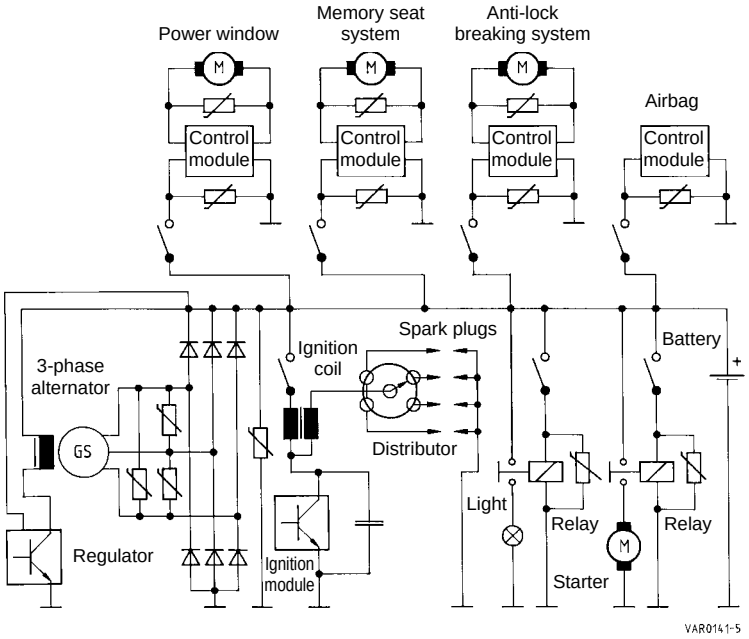


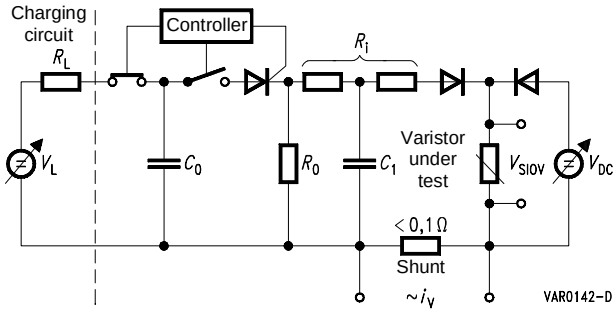
Figure 28 Automotive electrical system, complete EMC concept with varistors

3.3.4 Tests

Maintenance of EMC requirements can be checked with conventional test generators. Figures 29a and b show block diagrams for load dump tests with operating voltage applied. The electrical performance associated with a load dump of 100 J is illustrated in figures 30a to c.

Note

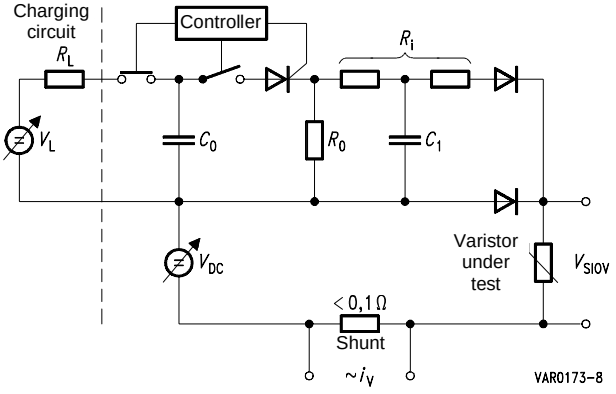
Circuit 29b produces the test pulse according to ISO 7637-1 (DIN 40 839); the 10 % time constant t_d can be set independently of the battery voltage. Note that the maximum discharge current is not limited by the source V_{DC}.



Typical values

C_0	20 … 35 mF
R_0	4 … 10 Ω
C_1	0 … 10 µF
R_i	0,5 … 4 Ω
V_L	0 … 200 V
V_{DC}	12 … 28 V
v_{SIOV}	Protection level of varistor
i_v	Current through varistor

Figure 29a Principle of load dump generator with battery connected in parallel

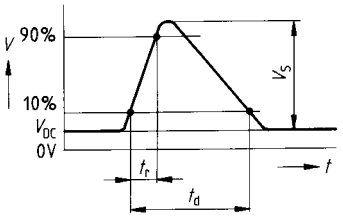


Typical values

C_0	4,7 … 47 mF
R_0	4 … 5 Ω
C_1	47 … 470 µF
R_i	0,5 … 5 Ω
V_L	0 … 200 V
V_{DC}	12 … 28 V
v_{SIOV}	Protection level of varistor
i_v	Current through varistor

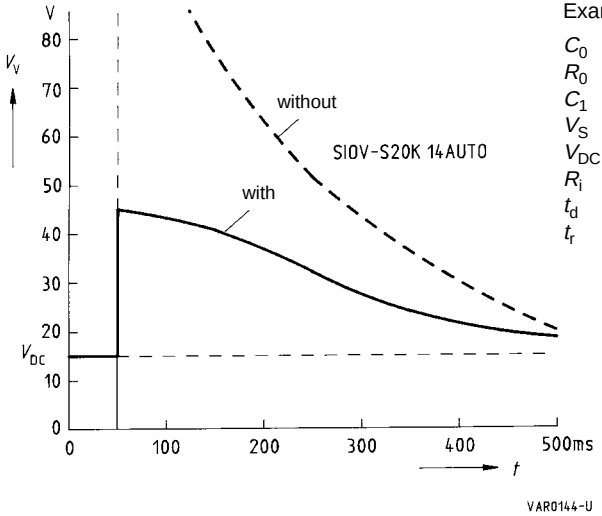
Figure 29b Principle of load dump generator with battery connected in series

30a



Test pulse 5
acc. ISO 7637-1
(DIN 40 839)

30b



Example:

C_0	37,6 mF
R_0	4,6 Ω
C_1	47 µF
V_S	146 V
V_{DC}	14 V
R_i	2 Ω
t_d	400 ms
t_r	0,1 ms

30c

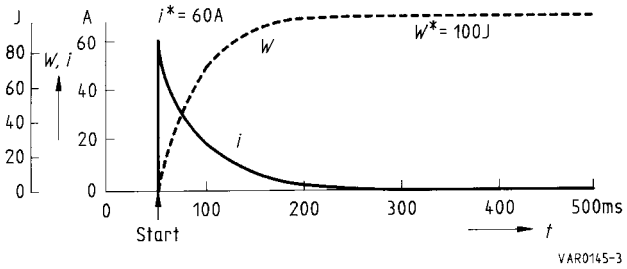


Figure 30a – c Voltage (b), current and energy absorption (c) on SIOV-S20K14AUTO with test pulse 5 (a), load dump generator as in figure 29 b

3.3.5 RFI suppression

The capacitance of varistors alone (some nF) is not enough for RFI suppression. Therefore S+M has developed the high-capacitive varistors SHCV (**S**iemens Matsushita **H**i**C**ap **V**aristors) that offer transient protection and RFI suppression in very compact form. These components are comprised of a multilayer varistor connected in parallel with a multilayer capacitor. SHCVs are especially suitable for handling RFI from small motors of windscreen wipers, power windows, memory seats, central locking, etc. Figure 31 shows an example of the suppression effect.

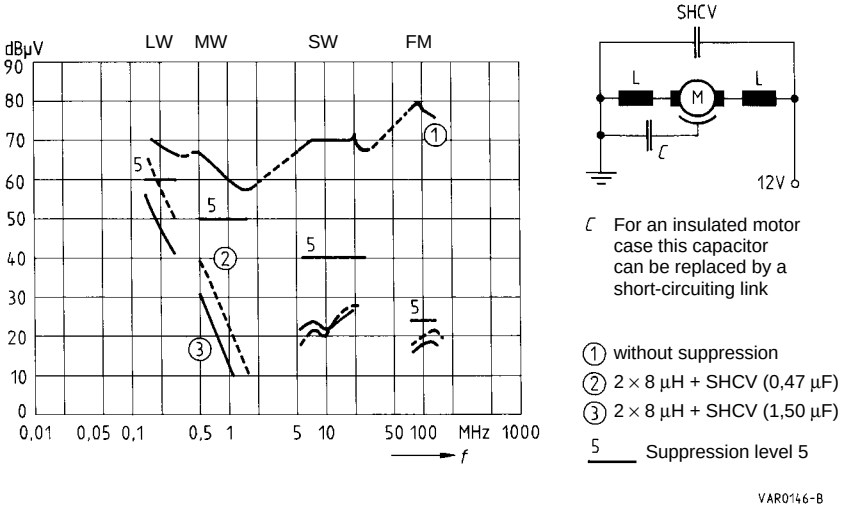


Figure 31 Example of RFI suppression in small motors with chokes and SHCVs (measured to VDE 0879, part 3)

3.4 Telecom

3.4.1 Requirements

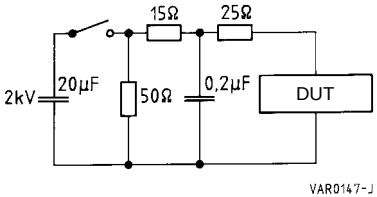
Electromagnetic interference on telecommunications, signal and control lines can be quite considerable as these lines tend to be long and exposed. So the requirements are correspondingly high when it comes to the electromagnetic compatibility of connected components or equipment.

According to the directives of the Deutsche Telekom, the interference or noise immunity of equipment is tested by application of a surge voltage with a wave form according to CCITT and IEC 1000-4-5. Figure 32 shows a simplified circuit diagram. The test is made with five pulses of either polarity, at least 60 s apart. According to equation 12, a voltage of 2 kV produces a surge current amplitude of approx. 45 A. SIOV varistors are capable of handling this surge current (and of absorbing the accompanying energy).

The choice of voltage class will depend on

– minimum required resistance in undisturbed operation
– maximum permissible protection level at 45 A.

Both figures can be derived from the *V*/*I* characteristics. (example of application 3.5.2).



e. g. telephone terminal device
DUT Device under test

Figure 32 Circuit for generating 10/700 µs test pulse to CCITT and IEC 1000-4-5

3.4.2 Telecom varistors

If requirements for minimum resistance and protection level cannot be met by standard types, it is possible to specify an application-oriented type. In such cases the tolerance bandwidth at 1 mA is of no interest, so it is not stated for telecom varistors.

The following special types have gone into wide use:

Design	Type	Ordering code	R_{min} (95 V)	v_{max} (45 A)
Disk	SIOV-S07S60AGS2	Q69X3815	250 kΩ	200 V
SMD	SIOV-CU4032S60AG2	Q69660-M600-S172	250 kΩ	200 V
SMD	SIOV-CN1812S60AG	Q69580-V600-S162	250 kΩ	200 V

Design	Type	Ordering code	R_{min} (150 V)	v_{max} (45 A)
Disk	SIOV-S07S95AGS2	Q69X4574	150 kΩ	270 V
SMD	SIOV-CU4032S95AG2	Q69660-M950-S172	150 kΩ	270 V
SMD	SIOV-CN1812S95AG2	Q69580-V950-S172	150 kΩ	270 V

Contact us if these types do not meet your requirements; we offer design to customer specifications.

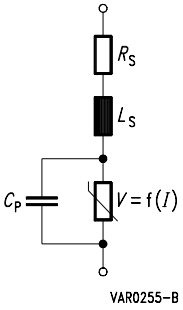
3.5 S+M's PSpice simulation model

3.5.1 Varistor model

The development of an SIOV model for the “PSpice Design Center” circuit simulation program allows varistors to be integrated into the computer-assisted development of modern electronic circuitry.

In the PSpice modelling concept, the varistor is represented by its V/I characteristic curve, a parallel capacitance and a series inductance.

The structure of this equivalent circuit is shown in figure 33.



$V = f(I)$ V/I characteristic
C_p Varistor capacitance
L_s Series inductance
R_S = 100 µΩ Series resistance

Figure 33 Varistor model, basic structure

In the model, the V/I characteristic curve is implemented by a controlled voltage source $V = f(I)$. An additional series resistance R_s = 100 µΩ has been inserted In order to prevent the unpermissible state which would occur if ideal sources were to be connected in parallel or the varistor model were to be connected directly to a source.

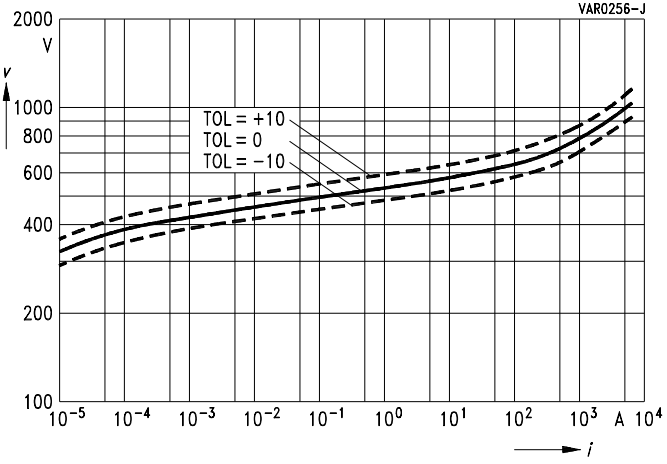
The following approximation is used for the mathematical description:

$$\log V = b1 + b2 \cdot \log(I) + b3 \cdot e^{-\log(I)} + b4 \cdot e^{\log(I)} \qquad I > 0 \qquad \text{(equ. 20)}$$

This means that the characteristic curve for any specific varistor can be described by the parameters b1 … b4. Figure 34 shows the typical V/I characteristic curve for the varistor SIOV-S20K275 and the corresponding parameters b1 … b4.

The tolerance bandwidth of the V/I characteristic curve can be shifted (cf. figure 7) in order to include cases of

– upper tolerance bandwidth limit:
  highest possible protection level for a given surge current, and
– lower tolerance bandwidth limit:
  highest possible (leakage) current for a given voltage.



b1 = 2.7233755
b2 = 0.0258453
b3 = 0.0005746
b4 = 0.0046033

Figure 34 *V/I* characteristic curve of SIOV-S20K275 with tolerance band

In the model, the capacitance values stated in the product tables are used. The dependence of the capacitance on the applied voltage and frequency is extremely low and can be neglected here.

It is not permissible to neglect the inductance of the varistor in applications with steep pulse leading edges. For this reason, it is represented by a series inductance and essentially is determined by the lead inductance. As opposed to this, the internal inductance of the metal oxide varistor may be neglected. The inductance values in the model library are chosen for typical applications, e.g. approx. 13 nH for the S20K275. If longer leads are used, insertion of additional inductances must be considered, if necessary. In the case of disk varistors, the inductance of the leads is approx. 1 nH/mm.

The PSpice simulation models (Version 6.1 for Windows 3.2) can be obtained from S+M together with a data book. Ordering code: B462-P6214-V1-X-7600.

They can also be downloaded from the INTERNET (WWW) under http://www.siemens.de/pr/index.htm.

Limits of the varistor model

For mathematical reasons, the *V/I* characteristic curves are extended in both directions beyond the current range (10 µA up to I_{max}) specified in this data book, and cannot be limited by the program procedure. The validity of the model breaks down if the specified current range is exceeded. For this reason, it is imperative that the user takes consideration of these limits when specifying the task; the upper limit depends on the type of varistor. Values of < 10 µA may lead to incorrect results, but do not endanger the component. In varistor applications, it is only necessary to know the exact values for the leakage current in the < 10 µA range in exceptional cases. As opposed to this, values exceeding the type-specific surge current I_{max}, may lead not only to incorrect results in actual practice but also to destruction of the component. Apart from this, the varistor model does not check adherence to other limit values such as maximum continuous power dissipation or surge current

deratings. In addition to carrying out simulation procedures, the adherence to such limits must always be ensured, observing the relevant spec given in the data book.

In critical applications, the simulation result should be verified by a test circuit.

The model does not take into account the low temperature coefficient of the varistors (equ. 7).

3.5.2 Application example

In accordance with CCITT /IEC 1000-4-5, the test pulse 10/700 µs is frequently used to ensure the interference immunity of equipment used in telecommunications applications. Five load pulses of each polarity are required, with a minimum interval of 60 s between loads. This test pulse is defined by the circuit of the test generator and the open-circuit voltage. Figure 32 shows the circuit of the test generator, figure 35 the implementation in PSpice.

In order to achieve an open-circuit voltage of 2 kV, the charging capacitor must be charged to 2,05 kV. In order to prevent an undefined floating of R_{m2}, an additional resistor R_1 = 10 MΩ is inserted at the output end.

The voltage level “K95” is given as an example. The suitability of S10K95 for the test pulses is to be tested.

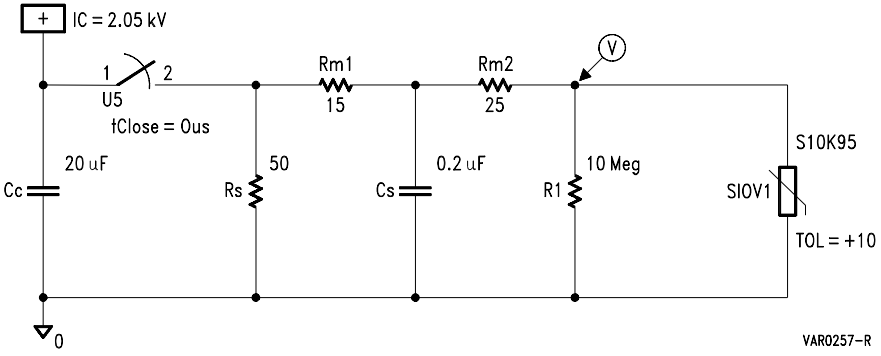


Figure 35 Simulation of the test pulse 10/700 µs applied to the device under test S10K95

For the varistor, the upper characteristic curve tolerance (TOL = +10) limit is used to simulate the worst case i.e. highest possible protection level. It is not considered necessary to model the device to be protected in this diagram, since, in relation to the varistor, this is generally of higher resistance for pulse loads.

Figure 36 shows the curve of the open-circuit voltage (varistor disconnected) and the maximum protection level (with varistor).

Surge current

Figure 37 shows the voltage and current curves, with the $\int i^* d\,t$ included in the drawing.

A maximum current of 44 A can be deduced from the curves.

Then, according to equation 14:

$$t^*_r = \frac{\int i^* d\,t}{\hat{i}^*} = \frac{17\ \text{mAs}}{44\ \text{A}} \approx 386\ \mu\text{s}$$

According to figure 38, the resulting maximum surge current for 10 loads is $i_{max} = 48\ \text{A} > \hat{i}^* = 44\ \text{A}$.

The selection criterion of equ. 9 is fulfilled.

Energy absorption

PSpice displays the energy absorption directly as $W^* = \int v^* i^* d\,t = 4{,}2\ \text{J}$.

The resulting permissible time interval between two pulses according to equ. 19 is:

$$T_{min} = \frac{W^*}{P_{max}} = \frac{4{,}2\ \text{J}}{0{,}4\ \text{W}} = 10{,}5\ \text{s}$$

This means that the requirement of a minimum time interval between pulses of 60 s or more is fulfilled.

Highest possible protection level

Figure 36 shows the highest possible protection level to be 260 V. Thus it is possible to reduce the "overvoltage" of 2 kV to 13 % of its value.

Note: The specification stated above can also be met using the specially developed telecom varistors (cf. section 3.4.2).

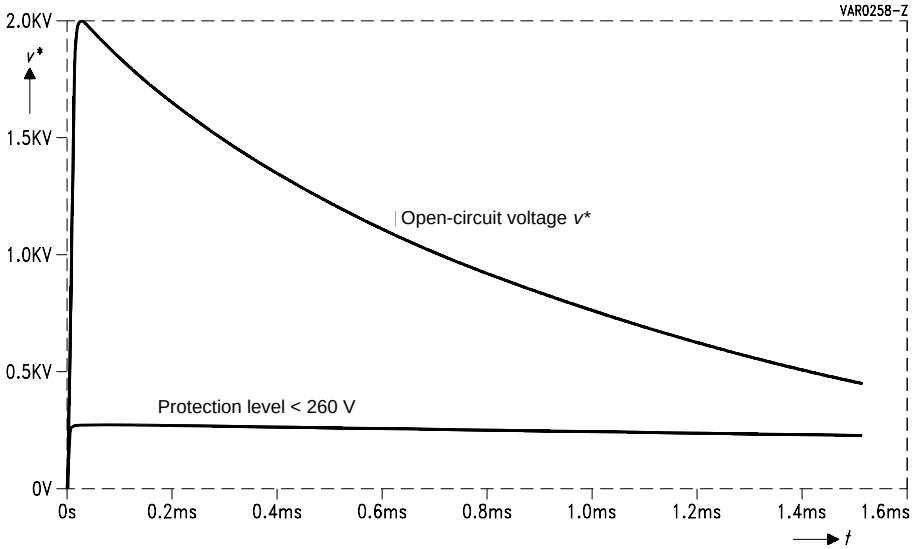


Figure 36 Open-circuit voltage (varistor disconnected) and maximum protection level (with varistor) achieved by the SIOV-S10K95 varistor

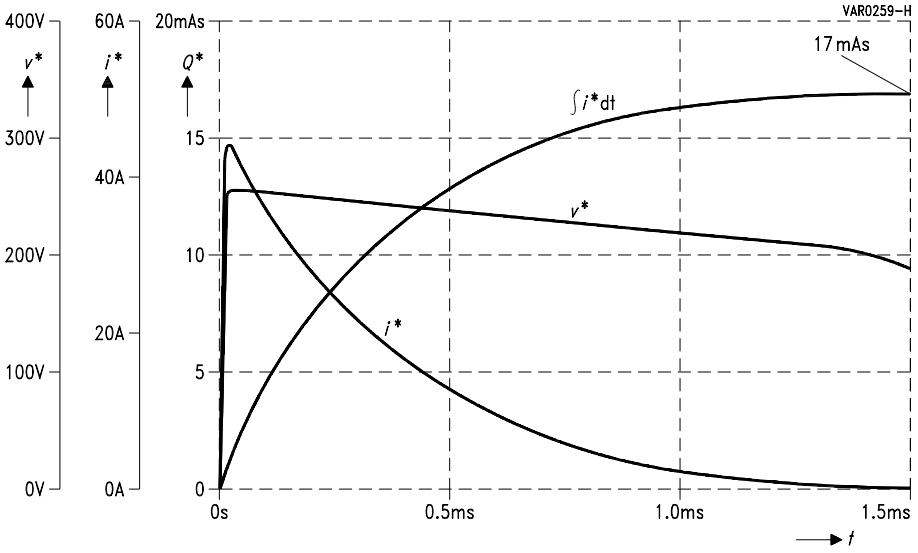


Figure 37 PSpice simulation: voltage, current and $\int i^* dt$ curves for the S10K95

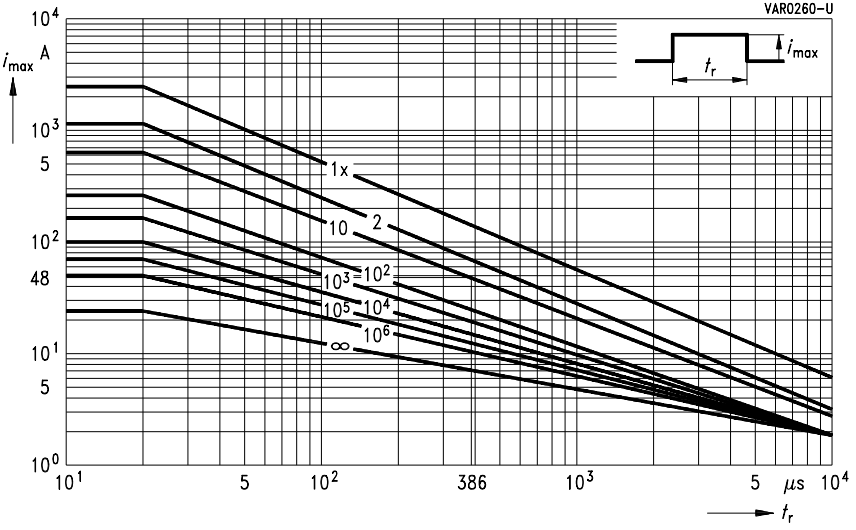


Figure 38 A maximum surge current i_{max} = 48 A (10 times) can be deduced for t^*_r = 386 µs from the derating curves for S10K50 … 320

3.6 High-performance varistors for power electronics

The introduction of the first semiconductor components more than 30 years ago ushered in an era of rapid electronics development. With the emergence of high-performance thyristors, in particular of GTO (Gate Turn Off) thyristors in the mid-eighties, power electronics technology began to establish itself in fields from which it had been excluded up to then: since then, applications in high-performance power converters and pulse-width-modulated inverters for railway vehicles are state-of-the-art.

With the wide distribution of high-performance semiconductors and the compressing of ever higher power ratings into ever smaller volumes, overvoltage protection has also attained a significant role. Admittedly, the risk of damage can be limited by appropriate dimensioning of the individual components. However, in most cases this approach fails due to the over-proportionately increased costs for semiconductor components with higher power ratings. A ratio of ≤ 2,5 has proved to be satisfactory as a safety factor between the maximum overvoltage to be expected and the highest periodic peak inverse voltage (V_{DSM} or V_{RRM}) in many applications. If there is a risk of overvoltages exceeding the level given by the selected safety factor, the use of an overvoltage protection circuit is necessary.

In the field of power electronics, the types of overvoltages can be categorized into the following groups:·

- overvoltages due to carrier storage effect (CSE)
- overvoltages caused by surge voltage waves
- switching transients

RC-elements, protective thyristors and protective diodes as well as voltage-dependent resistors have become the most commonly used protective elements.

Overvoltage protection with varistors

In the early days of power electronics, applications were frequently equipped with selenium overvoltage limiters. These components were available in various plate sizes and the size of the plate was determined by the maximum permissible peak current.

With the introduction of block varistors, components which showed considerably better performance with respect to leakage current and protection level became available.

In some application cases, block varistors in conventional housings still had the disadvantage that their continuous power dissipation capability was lower than that of selenium limiters.

PowerDisk

In order to increase the capability of handling periodic continuous loads, S+M Components has developed the PowerDisk, incorporating SIOV technology into a disk diode housing. The advantages of the construction translate into:

– excellent thermal conductivity
– easy mounting
– mechanical reliability
– high immunity to environmental influences

This means that the same mounting and cooling methods can be used for PowerDisks as for power semiconductors.

The PowerDisk PD80, when cooled on both faces, can dissipate 100 W, fifty times as much as the corresponding block varistor series B80. Upon special request, the PowerDisks can be supplied with the same operating voltages as the type series SIOV-B80. In this data book only the SIOV-PD80K1100 is specified.

Figure 39 shows the typical voltage and current as a function of time for a PowerDisk with 100 W power dissipation.

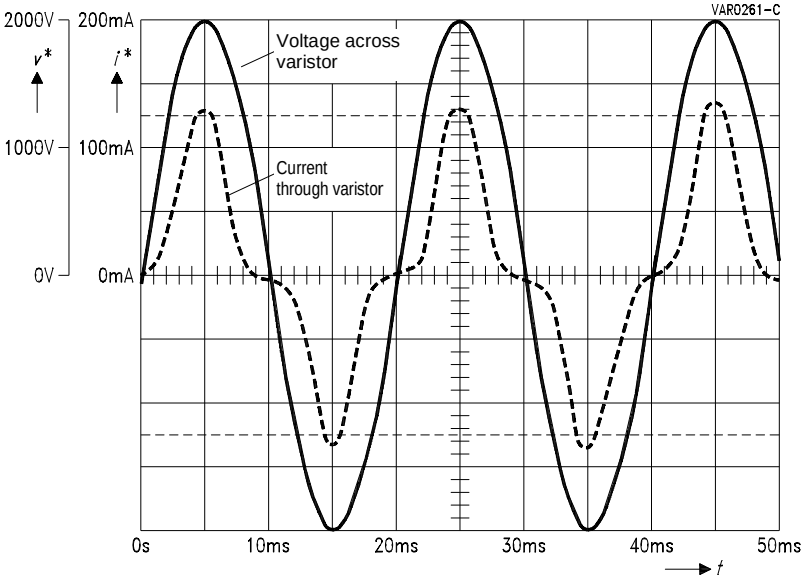


Figure 39 PowerDisk with power dissipation of approx. 100 W

3.7 Combined circuits

3.7.1 Stepped protection

If transient problems cannot be resolved with a single component like a varistor, it is always possible to combine different components and utilize their respective advantages. As an example, figure 40 illustrates the principle of stepped protection of a telemetering line with a gas-filled surge arrester [1], a varistor and a suppressor diode*):

The voltage of 10 kV is limited in three stages

- "coarse" surge arrester
- "standard" varistor
- "fine" suppressor diode, zener diode or filter [2]

to less than 50 V. The series inductors or resistors are necessary to decouple the voltage stages. For more details refer to Siemens publication [3].

Note
According to the specifications in [1] gas-filled surge arresters may not be used on low-impedance supply lines.

A PROTECTOR TESTER is available to test the function state of the above-mentioned protection components. This can be ordered using ordering code B84298-P1-A1.

3.7.2 Protective modules

Application-specific circuits for stepped protection assembled as modules, some incorporating overload protection and remote signaling, are available on the market.

Figures 41 a and b show some practical examples.

[1] Shortform catalog "Gas-Filled Surge Arresters", ordering no. B448-P4806-X-X-7400
[2] Data book "EMC Components", ordering no. B424-P2414-X-X-7600
[3] Pigler, Franz "EMV und Blitzschutz leittechnischer Anlagen" (only available in German), ordering no. A19100-L531-F503, ISBN 3-8009-1565-0
*) Not in the S+M range

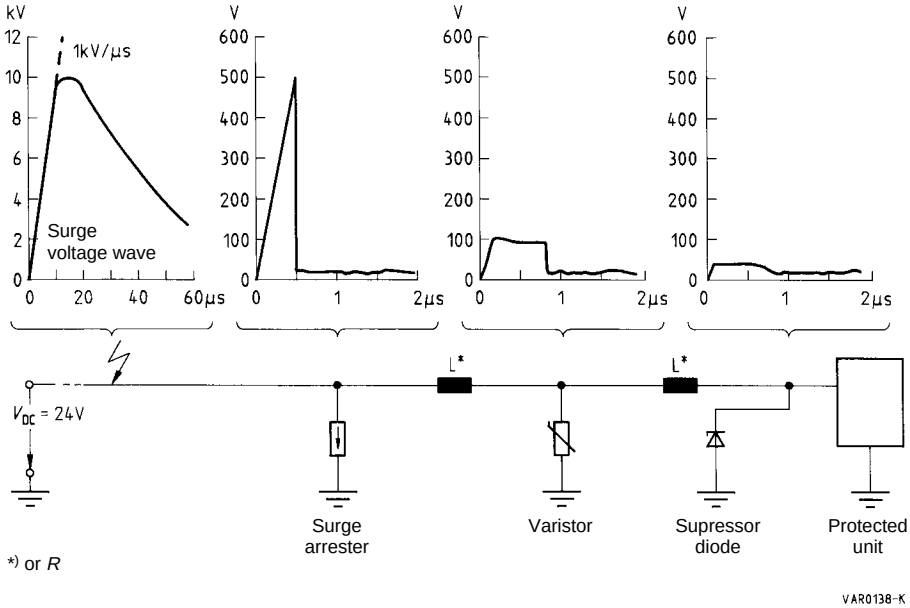
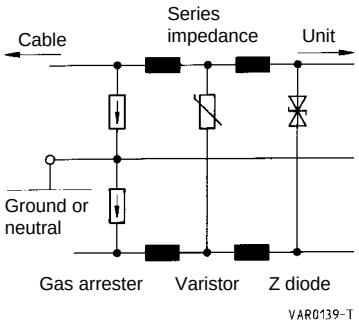
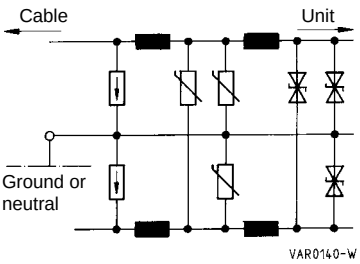


Figure 40 Principle of stepped protection with surge arrester, varistor and suppressor diode

41a



41b



Figures 41a and b Examples of transient protective modules
a) Circuit with coarse protection plus fine transverse voltage protection
b) Circuit with coarse protection plus fine longitudinal voltage and transverse voltage protection

Siemens Matsushita Components

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