

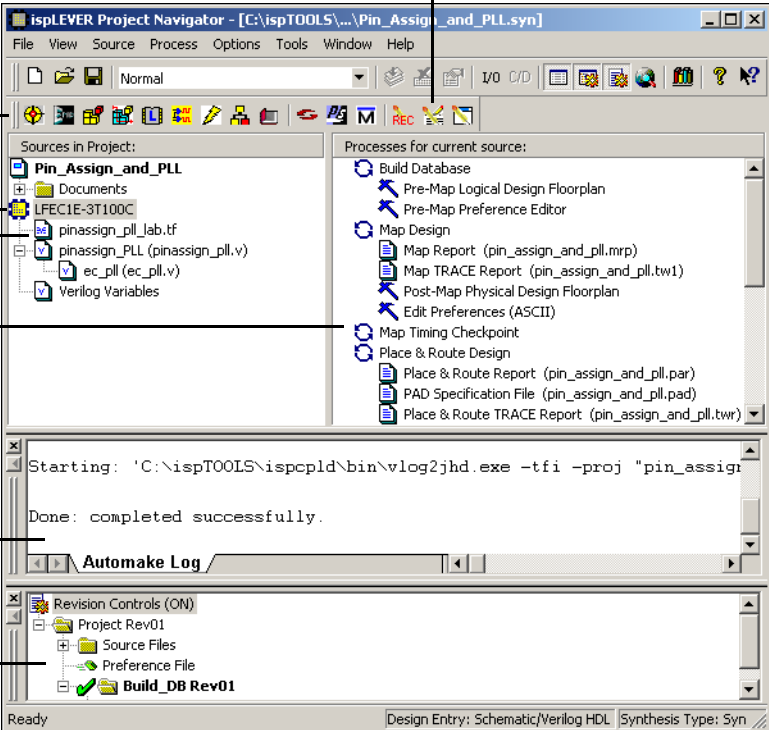
# Quick Start Guide for ispLEVER Software

This guide offers a quick overview of using ispLEVER<sup>®</sup> software to implement a design in a Lattice Semiconductor device. For more information, check the ispLEVER Help in the Help menu.

## ispLEVER Project Navigator

Project Navigator is the primary interface for the ispLEVER software. It organizes the files, gives access to the tools, and delivers messages. To start Project Navigator:

- ◆ Windows: select **Start > Programs > Lattice Semiconductor > ispLEVER Project Navigator**.
- ◆ UNIX or Linux: on a command line, enter **ispgui**.



Prepare Tcl scripts

Open ispLEVER tools

**Sources Window**  
Select the device or design modules

**Processes Window**  
For the selected item:

- Run process
- Generate report
- Generate file
- Open tool

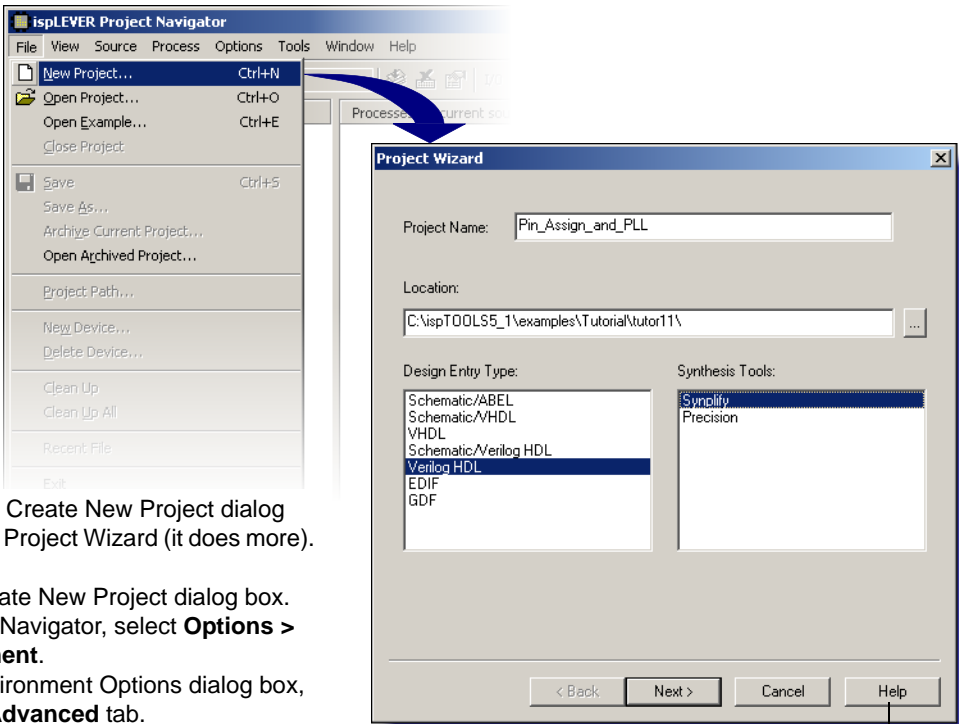
**Output Panel**  
Review process status and reports

**Revision Window**  
Select project versions

Ready Design Entry: Schematic/Verilog HDL Synthesis Type: Syn

# Creating a Project

Select **File** >  **New Project**.



For more information, click **Help**

If you see the Create New Project dialog box, switch to Project Wizard (it does more). To switch:

1. Close Create New Project dialog box.
2. In Project Navigator, select **Options > Environment**.
3. In the Environment Options dialog box, click the **Advanced** tab.
4. Select **Use Project Wizard to Create New Design**.
5. Click **OK**.

With the Project Wizard, set initial values for:


- ◆ Project name
- ◆ Design language
- ◆ Target device
- ◆ Location of the files
- ◆ Synthesis tool
- ◆ Source files

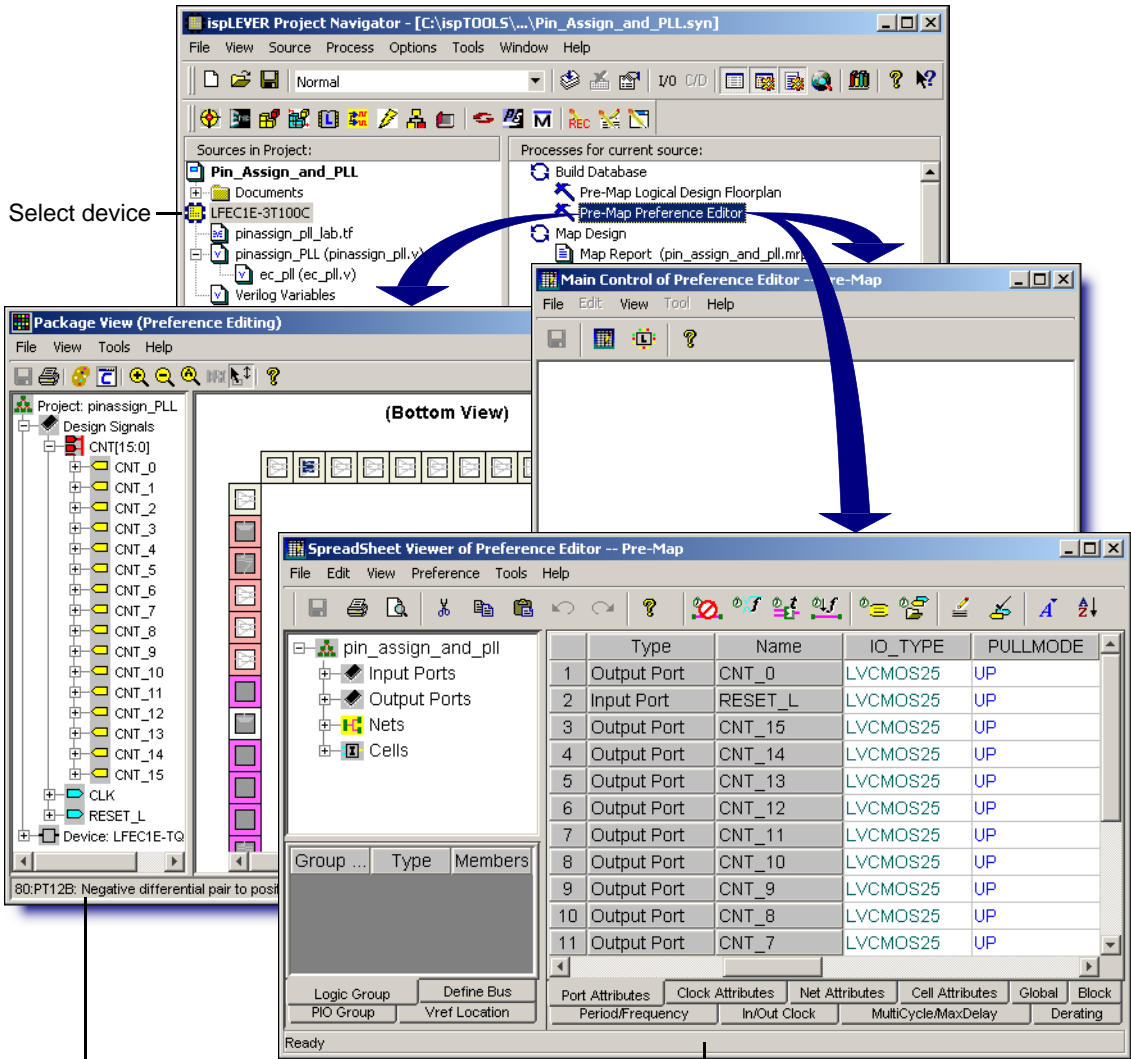
Design Entry Type (language) depends on the target device:

Target Device	Verilog	VHDL	EDIF	Schematic/Verilog	Schematic/VHDL	Schematic/ABEL
FPGA	◆	◆	◆	◆	◆	
ispXPGA®	◆	◆	◆			
CPLD/SPLD	◆	◆	◆	◆	◆	◆
ispXPLD®	◆	◆	◆	◆	◆	
ispGDX2™	◆	◆	◆			



# Setting Timing and I/O

Select the device . Then, in the Processes Window, double-click **Preference Editor** (for FPGAs) or **Constraint Editor** (for all other devices). The Preference Editor has three windows, as shown below; the Constraint Editor combines them as three panes in one window.



## Package View

Assign pinouts by drag-and-drop.

In Constraint Editor, select

**Device >**  **Package View.**

## Preference Editor's Spreadsheet Viewer

To set preferences, enter them in the sheet or through the **Preference** menu.

## Constraint Editor's Constraint Sheet

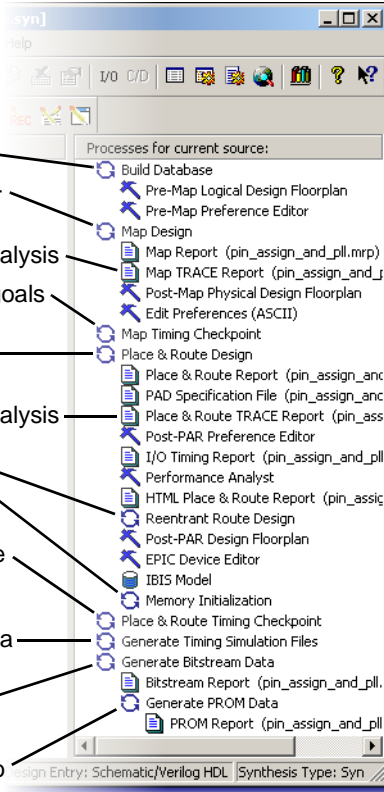
To set constraints, enter them in the sheet or through the **Pin Attribute** and **Device** menus.

# Implementing the Design

Select the device , then double-click a process . Start at the top and work down. The list of processes varies with the device and other factors.

For more information about a process, select it and press **F1**.

## FPGA Processes



Synthesize design — Build Database

Map to architecture-specific blocks — Pre-Map Logical Design Floorplan  
Pre-Map Preference Editor

Run static timing analysis — Map Design

Check map timing goals — Map Report (pin\_assign\_and\_pll.mrp)  
Map TRACE Report (pin\_assign\_and\_pll.mrp)  
Post-Map Physical Design Floorplan

Place blocks and route signals — Edit Preferences (ASCII)  
Map Timing Checkpoint

Run static timing analysis — Place & Route Design

Refine routing — Place & Route Report (pin\_assign\_and\_pll.mrp)  
PAD Specification File (pin\_assign\_and\_pll.mrp)  
Place & Route TRACE Report (pin\_assign\_and\_pll.mrp)

Generate memory initialization file — Post-PAR Preference Editor

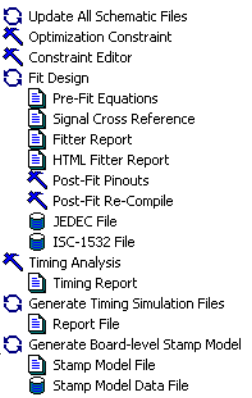
Check place & route timing goals — I/O Timing Report (pin\_assign\_and\_pll.mrp)  
Performance Analyst

Generate timing data for simulators — HTML Place & Route Report (pin\_assign\_and\_pll.mrp)  
Reentrant Route Design

Generate device programming file — Post-PAR Design Floorplan  
EPIC Device Editor

Convert bitstream to PROM format — IBIS Model  
Memory Initialization  
Place & Route Timing Checkpoint  
Generate Timing Simulation Files  
Generate Bitstream Data  
Bitstream Report (pin\_assign\_and\_pll.mrp)  
Generate PROM Data  
PROM Report (pin\_assign\_and\_pll.mrp)

## CPLD/SPLD Processes



Synthesize design — Update All Schematic Files  
Optimization Constraint  
Constraint Editor

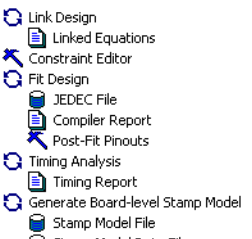
Place blocks and route signals — Fit Design  
Pre-Fit Equations  
Signal Cross Reference  
Fitter Report  
HTML Fitter Report  
Post-Fit Pinouts  
Post-Fit Re-Compile

Run static timing analysis — JEDEC File  
ISC-1532 File  
Timing Analysis

Generate timing data for simulators — Timing Report  
Generate Timing Simulation Files  
Report File

Generate timing data for board-level design — Generate Board-level Stamp Model  
Stamp Model File  
Stamp Model Data File

## Digital Interconnect Processes



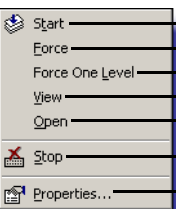
Combine modules — Link Design  
Linked Equations  
Constraint Editor

Place blocks and route signals — Fit Design  
JEDEC File  
Compiler Report  
Post-Fit Pinouts

Run static timing analysis — Timing Analysis  
Timing Report

Generate timing data for board-level design — Generate Board-level Stamp Model  
Stamp Model File  
Stamp Model Data File

For a menu of options, right-click the process.



Start — Start the process (will not run if up to date)

Force — Run all steps even if up to date

Force One Level — Run last step even if up to date

View — Open the tool, report, or file, creating it if necessary

Open — Open the report or file

Stop — Stop the process

Properties... — Set process properties

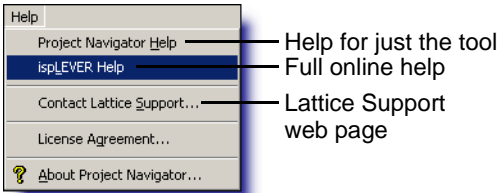
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# Getting More Information

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## Refer to the Online Help

- ◆ Select **Help** > **ispLEVER Help**.



- ◆ Select an item in a window or dialog box and press **F1**.
- ◆ Click **Help** in a dialog box.


Take the tutorials. In the online help, select **Tutorials and Examples**.

Refer to the reference manuals. In the online help, select **Software Manuals > Software User Manuals**.

Refer to the synthesis tool and simulator tool manuals. In the online help, select **Software Manuals > Third-Party Manuals**.


## Refer to the Web Site

**Lattice Semiconductor**  
[www.latticesemi.com](http://www.latticesemi.com)

**What's New at Lattice**  
[www.latticesemi.com/search/new\\_updated.cfm](http://www.latticesemi.com/search/new_updated.cfm)  
or click 

**Frequently Asked Questions**  
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