Lattice®
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ispLSI Macro Library Reference Manual

Version 8.2

Technical Support Line: 1-800-LATTICE or (408) 826-6002
IDE-ISPML-RM 8.2.1

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August 2000

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Preface

Overview

This Preface contains information on the following topics:

- Purpose and Scope
- Documentation Conventions
- Quick Reference Macro Table
- Programmable Macro Reference

Purpose and Scope

The *ispLSI Macro Library Reference Manual* documents the features, capabilities, and use of the library macros provided with the pLSI and ispLSI Development System from Lattice Semiconductor Corporation (LSC). This reference manual provides the following information about each macro:

Function The purpose and use of the macro.

Availability 1000, 2000, 3000, 5000, or 8000 devices.

Symbol The representation of a macro within a schematic.

Type Macro types are as follows:

Logic
These are the building blocks of macros.

Primitive
AND, NAND, OR, NOR, and XOR gates, and the FD11 and FD12 D-type flip-flops are logic primitives.

Soft
A soft macro is a predefined netlist of a particular logic function.

Hard
A hard macro is a netlist that is pre-mapped to the ispLSI architecture for optimal resource utilization or performance.

Logic Resources The number of product terms (PTs), Generic Logic Blocks (GLBs), GLB outputs, and approximate GLB levels a macro requires.

Macro Port Definition The format of the equation you enter that represents the macro and the port order.

Truth Table The table that shows the relationships between all the possible inputs and outputs for the macro.

Schematic A diagram of the logic within the macro is provided for the more complex macros.

Documentation Conventions

The following sections describe the conventions used for signal names, truth tables, pin labeling, and logic resources. A quick reference table is also included which gives a brief description of each macro and its availability.

Signal Names

A0..A_{n-1},B0..B_{n-1}	inputs
Z0..Z_{n-1}	outputs
ZN0	output of inverted gate
XI0	external input pin
XO0	external output pin
OE	Output Enable
XB0	external bidirectional pin
CLK	Clock line
D0..D_{n-1}	input to D flip-flop/latch; input to T flip-flop; load inputs for counters and shift registers
Q0..Q_{n-1}	output of flip-flop or latch
Q0'..Q_{n-1}'	previous output of flip-flop or latch
TE	Test Enable input for scan flip-flops
TI0..TI_{n-1}	Test Inputs for scan flip-flops and latches
G	Gate for latch
TG	Test Gate for scan latch
LD	parallel Load for shift registers and counters
CD	Clear Direct (asynchronous)
PS	Preset Synchronous
CS	Clear Synchronous
PD	Preset Direct (only on latches)
J0,K0	inputs to JK flip-flop
S0,S1,R0,R1	inputs to SR latch
S0..S_{n-1}	select lines – multiplexors/demultiplexors, decoders/priority encoders
EN	Enable for multiplexors and counters
CI	Carry In for adders
CO	Carry Out for adders
BI	Borrow In for subtractors
BO	Borrow Out for subtractors
EQ	A equals B output for comparators
GT	A greater than B output for comparators
LT	A Less Than B output for comparators
EQI	Cascade input of EQ from previous stage for mag comparators
GTI	Cascade input of GT from previous stage for mag comparators
LTI	Cascade input of LT from previous stage for mag comparators

CAI	shift registers: serial input; counters: CAscade In
CAIR	shift right serial input
CAIL	shift left serial input
RL	shift Right/shift Left control for SRRL shift registers
CAO	CAscade Out for counters
DNUP	count Down/count UP control for up-down counters

Truth Tables

x	don’t care
X	X (unknown) state
Z	high impedance state
d	any pattern of 1s and 0s on an input or set of inputs
$\overline{d}$	the inverse of d
↑	rising clock edge
↓	falling clock edge
-	appears in output column if a bidirectional pin acts as an input pin

For macros such as the MUX2 and the MUX2E, which are identical except for the enable feature on the MUX2E, table cells in gray represent the additional truth table row and column that apply only to the macro with the enable. For example, the truth table for the MUX2 and MUX2E appears as follows:

Input		**Output**
EN	**S0**	**Z0**
1	0	A0
1	1	A1
0	x	0

By disregarding the gray cells in the truth table shown above, you can see the truth table for the MUX2.

Input	**Output**
S0	**Z0**
0	A0
1	A1

Some truth tables show input and output information for several macros that perform the same function but handle a different number of bits. For example, LD11 and LD14 have one-bit and four-bit D latches, respectively. In these truth tables, you see **0~$_{n-1}$**, which indicates that the column represents bits 0 through n-1, where n is the number of bits in the macro of interest. The truth table for LD11 and LD14 looks like:

Input		**Output**
D0~D$_{n-1}$	**G**	**Q0~Q$_{n-1}$**
d	1	d
x	0	Q0~Q$_{n-1}$

The truth table for LD11 alone would look like this:

Input		Output
D0	**G**	**Q0**
d	1	d
x	0	Q0

Module Macro Truth Tables

*............. These inputs, once set, are fixed and can only be connected to VCC/GND.

‡............. Refer to the User Programmable Features table.

†............. Refer to the section on Control Blocks for functionality.

**............ ADI and ADO are required to share I/O pins so they must be connected to bidirectional pins.

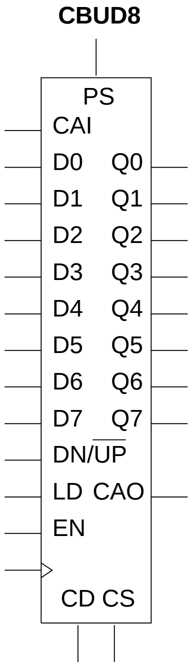
§............. Data-in can only be external input signals. No logic can be connected.

§§........... Data-out can only be external output signals. No logic can be connected.

Pin Labeling

Two formats for describing groups of pins–logic diagrams and equation entry lines–are included in this manual. Both of these formats are shown in the following example:

Logic Symbol



Macro Port Definition

```
CBUD8([Q0..Q7],CAO,[D0..D7],CAI,CLK,PS,LD,EN,DNUP,CD,CS);
```

Both of these examples refer to pins Q0 through Q7. The expressions [Q0..Q7] and Q0, Q1, Q2, Q3, Q4, Q5, Q6, Q7 are equivalent.

Macro Port Definition shows the pin order of the macros.

Logic Resources

The logic resources of each macro are described as follows:

Product Terms (PTs) The number of gates in the AND array of the GLBs used by the macro. Add one product term if you use the Product Term Clock option with the macro or if the macro has an asynchronous clear (CD). If “/out” follows the number of product terms, it means the “number of product terms per output.”

Generic Logic Blocks(GLB) The number of GLBs that the macro uses.

GLB Outputs (Outputs) The number of GLB outputs the macro uses, including outputs internal to the macro. A GLB output is also called an Output Logic Macrocell (OLMC).

GLB Levels (Levels) The number of levels of GLBs (not gates) used.

For example, this is the logic resource summary for MUX24 and MUX24E:

Macro	PT	GLBs	Outputs	Levels
MUX24	4/out	.5	2	1
MUX24E	4/out	.5	2	1

A dash (-) indicates that the amount of the resource the macro uses depends on how the macro is used or how the partitioner in ispEXPERT Compiler arranges the macro in the device.

Logic resources for most of the logic primitive macros are not listed. These macros are rarely used by themselves, and when used with other macros, they are placed in space left over by other macros.

Logic resource information is approximate because the partitioner may use different resources for a given macro depending on the rest of the design.

Using the NOMIN Attribute

Calling some macros and specifying the NOMIN attribute for a specific pin results in error 5319 being issued to indicate a problem fitting the logic. The following table lists the macros and the pin that cannot be assigned the NOMIN attribute.

Macro	Parameter
F3ADD_2	P012
ADDF8A_2	P012
ADDF8A_5	P345
ADDF16A_2	P012
ADDF16A_4	P345
ADDF16A_6	P678
ADDF16A_8	P911
ADDF16A_10	P1214
ADDH8A_4	P345
ADDH16A_4	P345
ADDH16A_6	P678
ADDH16A_8	P911
ADDH16A_10	P1214
CMP8	EQ
MULT44_6	P345
F3SUB_2	P012
SUBF8A_2	P012
SUBF8A_5	P345
SUBF16A_2	P012
SUBF16A_4	P345
SUBF16A_6	P678
SUBF16A_8	P911
SUBF16A_10	P1214
SUBH8A_4	P345
SUBH16A_4	P345
SUBH16A_6	P678
SUBH16A_8	P911
SUBH16A_10	P1214

Quick Reference Macro Table

The following table lists the macros available from LSC for use with the ispLSI 1000, 2000, 3000, 5000, and 8000 device families.

Macro	Description	1000	2000	3000	5000	8000
ADDF1	1-bit full adder	X	X	X	X	X
ADDF2	2-bit full adder	X	X	X	X	X
F3ADD	3-bit full adder with propagate-generate	X	X	X	X	X
ADDF4	4-bit full adder	X	X	X	X	X
ADDF8	8-bit full adder	X	X	X	X	X
ADDF8A	8-bit full adder with propagate-generate submacros	X	X	X	X	X
ADDF16A	16-bit full adder with propagate-generate submacros	X	X	X	X	X
ADDH1	1-bit half adder	X	X	X	X	X
ADDH2	2-bit half adder	X	X	X	X	X
ADDH3	3-bit half adder	X	X	X	X	X
ADDH4	4-bit half adder	X	X	X	X	X
ADDH8	8-bit half adder	X	X	X	X	X
ADDH8A	8-bit half adder built with propagate-generate submacros	X	X	X	X	X
ADDH16A	16-bit half adder built with propagate-generate submacros	X	X	X	X	X
AND2 through AND18	2 to 18-input AND gates	X	X	X	X	X
BI11	1-bit bidirect pin	X	X	X	X	X
BI14	Four BI11s with common Output Enable	X	X	X	X	X
BI18	Eight BI11s with common Output Enable	X	X	X	X	X

Macro	Description	1000	2000	3000	5000	8000
BI21	1-bit bidirect pin with inverted output	X	X	X	X	X
BI24	Four BI21s with common Output Enable	X	X	X	X	X
BI28	Eight BI21s with common Output Enable	X	X	X	X	X
BI31	1-bit bidirect pin with active low Output Enable	X	X	X	X	X
BI34	Four BI31s with common Output Enable	X	X	X	X	X
BI38	Eight BI31s with common Output Enable	X	X	X	X	X
BI41	1-bit bidirect pin with inverted output and active low Output Enable	X	X	X	X	X
BI44	Four BI41s with common Output Enable	X	X	X	X	X
BI48	Eight BI41s with common Output Enable	X	X	X	X	X
BIID11	1-bit bidirect pin with registered input	X	X	X		X
BIID14	Four BIID11s with common clock and Output Enable	X	X	X		X
BIID18	Eight BIID11s with common clock and Output Enable	X	X	X		X
BIID21	1-bit bidirect pin with registered input and inverted output	X	X	X		X
BIID24	Four BIID21s with common clock and Output Enable	X	X	X		X
BIID28	Eight BIID21s with common clock and Output Enable	X	X	X		X
BIID31	1-bit bidirect pin with registered input and active low enable	X	X	X		X

Macro	**Description**	**1000**	**2000**	**3000**	**5000**	**8000**
BIID34	Four BIID31s with common clock and Output Enable	X	X	X		X
BIID38	Eight BIID31s with common clock and Output Enable	X	X	X		X
BIID41	1-bit bidirect pin with registered input, inverted output, and active low enable	X	X	X		X
BIID44	Four BIID41s with common clock and Output Enable	X	X	X		X
BIID48	Eight BIID41s with common clock and Output Enable	X	X	X		X
BIID51	1-bit bidirect pin with registered input and inverted clock	X	X	X		X
BIID54	Four BIID51s with common clock and Output Enable	X	X	X		X
BIID58	Eight BIID51s with common clock and Output Enable	X	X	X		X
BIID61	1-bit bidirect pin with registered input, inverted output, and inverted clock	X	X	X		X
BIID64	Four BIID61s with common clock and Output Enable	X	X	X		X
BIID68	Eight BIID61s with common clock and Output Enable	X	X	X		X
BIID71	1-bit bidirect pin with registered input, active low enable, and inverted clock	X	X	X		X
BIID74	Four BIID71s with common clock and Output Enable	X	X	X		X
BIID78	Eight BIID71s with common clock and Output Enable	X	X	X		X
BIID81	1-bit bidirect pin with registered input, inverted output, active low enable, and inverted clock	X	X	X		X

Macro	Description	1000	2000	3000	5000	8000
BIID84	Four BIID81s with common clock and Output Enable	X	X	X		X
BIID88	Eight BIID81s with common clock and Output Enable	X	X	X		X
BIIL11	1-bit bidirect pin with latched input	X	X	X		X
BIIL14	Four BIIL11s with common G and Output Enable	X	X	X		X
BIIL18	Eight BIIL11s with common G and Output Enable	X	X	X		X
BIIL21	1-bit bidirect pin with latched input and inverted output	X	X	X		X
BIIL24	Four BIIL21s with common G and Output Enable	X	X	X		X
BIIL28	Eight BIIL21s with common G and Output Enable	X	X	X		X
BIIL31	1-bit bidirect pin with latched input and active low enable	X	X	X		X
BIIL34	Four BIIL31s with common G and Output Enable	X	X	X		X
BIIL38	Eight BIIL31s with common G and Output Enable	X	X	X		X
BIIL41	1-bit bidirect pin with latched input, inverted output, and active low enable	X	X	X		X
BIIL44	Four BIIL41s with common G and Output Enable	X	X	X		X
BIIL48	Eight BIIL41s with common G and Output Enable	X	X	X		X
BIIL51	1-bit bidirect pin with latched input, and inverted G	X	X	X		X
BIIL54	Four BIIL51s with common G and Output Enable	X	X	X		X
BIIL58	Eight BIIL51s with common G and Output Enable	X	X	X		X

Macro	Description	1000	2000	3000	5000	8000
BIIL61	1-bit bidirect pin with latched input, inverted output, and inverted G	X	X	X		X
BIIL64	Four BIIL61s with common G and Output Enable	X	X	X		X
BIIL68	Eight BIIL61s with common G and Output Enable	X	X	X		X
BIIL71	1-bit bidirect pin with latched input, active low enable, and inverted G	X	X	X		X
BIIL74	Four BIIL71s with common G and Output Enable	X	X	X		X
BIIL78	Eight BIIL71s with common G and Output Enable	X	X	X		X
BIIL81	1-bit bidirect pin with latched input, inverted output, active low enable, and inverted G	X	X	X		X
BIIL84	Four BIIL81s with common G and Output Enable	X	X	X		X
BIIL88	Eight BIIL81s with common G and Output Enable	X	X	X		X
BIN27	Binary-7-segment decoder with enable	X	X	X	X	X
BUF	Single input buffer	X	X	X	X	X
CBD11	1-bit down counter with async clear, CAI, and CAO	X	X	X	X	X
CBD12	2-bit down counter with async clear, CAI, and CAO	X	X	X	X	X
CBD14	4-bit down counter with async clear, CAI, and CAO	X	X	X	X	X
CBD18	8-bit down counter with async clear, CAI, and CAO	X	X	X	X	X
CBD21	1-bit down counter with async clear, enable, CAI, and CAO	X	X	X	X	X

Macro	**Description**	**1000**	**2000**	**3000**	**5000**	**8000**
CBD22	2-bit down counter with async clear, enable, CAI, and CAO	X	X	X	X	X
CBD24	4-bit down counter with async clear, enable, CAI, and CAO	X	X	X	X	X
CBD28	8-bit down counter with async clear, enable, CAI, and CAO	X	X	X	X	X
CBD31	1-bit down counter with async clear, enable, parallel data load, sync preset, CAI, and CAO	X	X	X	X	X
CBD32	2-bit down counter with async clear, enable, parallel data load, sync preset, CAI, and CAO	X	X	X	X	X
CBD34	4-bit down counter with async clear, enable, parallel data load, sync preset, CAI, and CAO	X	X	X	X	X
CBD38	8-bit down counter with async clear, enable, parallel data load, sync preset, CAI, and CAO	X	X	X	X	X
CBD41	1-bit down counter with sync clear, enable, parallel data load, sync preset, CAI, and CAO	X	X	X	X	X
CBD42	2-bit down counter with sync clear, enable, parallel data load, sync preset, CAI, and CAO	X	X	X	X	X
CBD44	4-bit down counter with sync clear, enable, parallel data load, sync preset, CAI, and CAO	X	X	X	X	X

Macro	Description	1000	2000	3000	5000	8000
CBD48	8-bit down counter with sync clear, enable, parallel data load, sync preset, CAI, and CAO	X	X	X	X	X
CBD516	16-bit down counter with async clear and enable	X	X	X	X	X
CBD616	16-bit down counter with async clear, CAO, and enable	X	X	X	X	X
CBU11	1-bit up counter with async clear, CAI, and CAO	X	X	X	X	X
CBU12	2-bit up counter with async clear, CAI, and CAO	X	X	X	X	X
CBU14	4-bit up counter with async clear, CAI, and CAO	X	X	X	X	X
CBU18	8-bit up counter with async clear, CAI, and CAO	X	X	X	X	X
CBU21	1-bit up counter with async clear, enable, CAI, and CAO	X	X	X	X	X
CBU22	2-bit up counter with async clear, enable, CAI, and CAO	X	X	X	X	X
CBU24	4-bit up counter with async clear, enable, CAI, and CAO	X	X	X	X	X
CBU28	8-bit up counter with async clear, enable, CAI, and CAO	X	X	X	X	X
CBU31	1-bit up counter with async clear, enable, parallel data load, sync preset, CAI, and CAO	X	X	X	X	X
CBU32	2-bit up counter with async clear, enable, parallel data load, sync preset, CAI, and CAO	X	X	X	X	X
CBU34	4-bit up counter with async clear, enable, parallel data load, sync preset, CAI, and CAO	X	X	X	X	X

Macro	Description	1000	2000	3000	5000	8000
CBU38	8-bit up counter with async clear, enable, parallel data load, sync preset, CAI, and CAO	X	X	X	X	X
CBU41	1-bit up counter with sync clear, enable, parallel data load, sync preset, CAI, and CAO	X	X	X	X	X
CBU42	2-bit up counter with sync clear, enable, parallel data load, sync preset, CAI, and CAO	X	X	X	X	X
CBU44	4-bit up counter with sync clear, enable, parallel data load, sync preset, CAI, and CAO	X	X	X	X	X
CBU48	8-bit up counter with sync clear, enable, parallel data load, sync preset, CAI, and CAO	X	X	X	X	X
CBU516	16-bit up counter with async clear and enable	X	X	X	X	X
CBU616	16-bit up counter with async clear, enable, and CAO	X	X	X	X	X
CBU716	16-bit up counter with async clear, enable, parallel data load and carry out	X	X	X	X	X
CBUD1	1-bit up/down counter with async clear, sync clear, enable, parallel data load, sync preset, CAI, and CAO	X	X	X	X	X
CBUD2	2-bit up/down counter with async clear, sync clear, enable, parallel data load, sync preset, CAI, and CAO	X	X	X	X	X
CBUD4	4-bit up/down counter with async clear, sync clear, enable, parallel data load, sync preset, CAI, and CAO	X	X	X	X	X

Macro	**Description**	**1000**	**2000**	**3000**	**5000**	**8000**
CBUD8	8-bit up/down counter with async clear, sync clear, enable, parallel data load, sync preset, CAI, and CAO	X	X	X	X	X
CDD14	4-bit decade down counter with async clear, enable, and parallel data load	X	X	X	X	X
CDD18	8-bit decade down counter with async clear, enable, and parallel data load	X	X	X	X	X
CDD24	4-bit decade down counter with sync clear, enable, and parallel data load	X	X	X	X	X
CDD28	8-bit decade down counter with sync clear, enable, and parallel data load	X	X	X	X	X
CDD34	4-bit decade down counter with async clear, enable, and parallel data load, CAI, and CAO	X	X	X	X	X
CDD38	8-bit decade down counter with async clear, enable, and parallel data load, CAI, and CAO	X	X	X	X	X
CDD44	4-bit decade down counter with sync clear, enable, parallel data load, CAI, and CAO	X	X	X	X	X
CDD48	8-bit decade down counter with sync clear, enable, parallel data load, CAI, and CAO	X	X	X	X	X
CDU14	4-bit decade up counter with async clear, enable, and parallel data load	X	X	X	X	X
CDU18	8-bit decade up counter with async clear, enable, and parallel data load	X	X	X	X	X

Macro	Description	1000	2000	3000	5000	8000
CDU24	4-bit decade up counter with sync clear, enable, and parallel data load	X	X	X	X	X
CDU28	8-bit decade up counter with sync clear, enable, and parallel data load	X	X	X	X	X
CDU34	4-bit decade up counter with async clear, enable, parallel data load, CAI, and CAO	X	X	X	X	X
CDU38	8-bit decade up counter with async clear, enable, parallel data load, CAI, and CAO	X	X	X	X	X
CDU44	4-bit decade up counter with sync clear, enable, parallel data load, CAI, and CAO	X	X	X	X	X
CDU48	4-bit decade up counter with sync clear, enable, parallel data load, CAI, and CAO	X	X	X	X	X
CDUD4	4-bit up/down decade counter with async clear, sync clear, enable, and parallel data load	X	X	X	X	X
CDUD8	8-bit up/down decade counter with async clear, sync clear, enable, and parallel data load	X	X	X	X	X
CDUD4c	4-bit up/down decade counter with async clear, sync clear, enable, and parallel data load, CAI, and CAO	X	X	X	X	X
CDUD8c	8-bit up/down decade counter with async clear, sync clear, enable, parallel data load, CAI, and CAO	X	X	X	X	X
CGD14	4-bit gray code down counter with async clear, sync preset, enable, and parallel data load	X	X	X	X	X

Macro	Description	1000	2000	3000	5000	8000
CGD24	4-bit gray code down counter with sync clear, sync preset, enable, and parallel data load	X	X	X	X	X
CGU14	4-bit gray code up counter with async clear, sync preset, enable, and parallel data load	X	X	X	X	X
CGU24	4-bit gray code up counter with sync clear, sync preset, enable, and parallel data load	X	X	X	X	X
CGUD4	4-bit gray code up/down counter with async clear, sync clear and preset, enable, and parallel data load	X	X	X	X	X
CMP2	2-bit equality comparator	X	X	X	X	X
CMP4	4-bit equality comparator	X	X	X	X	X
CMP8	8-bit equality comparator	X	X	X	X	X
DEC2	1-2 decoder	X	X	X	X	X
DEC2E	1-2 decoder with enable	X	X	X	X	X
DEC3	1-3 decoder	X	X	X	X	X
DEC3E	1-3 decoder with enable	X	X	X	X	X
DEC4	1-4 decoder	X	X	X	X	X
DEC4E	1-4 decoder with enable	X	X	X	X	X
DMUX2	1 of 2 output dmux	X	X	X	X	X
DMUX2E	1 of 2 output dmux with enable	X	X	X	X	X
DMUX4	1 of 4 output dmux	X	X	X	X	X
DMUX4E	1 of 4 output dmux with enable	X	X	X	X	X
DMUX22	Dual 1 of 2 output dmux with common select line	X	X	X	X	X

Macro	**Description**	**1000**	**2000**	**3000**	**5000**	**8000**
DMUX22E	Dual 1 of 2 output dmux with common select line and enable	X	X	X	X	X
DMUX24	Dual 1 of 4 output dmux with common select line	X	X	X	X	X
DMUX24E	Dual 1 of 4 output dmux with common select line and enable	X	X	X	X	X
DMUX42	Quad 1 of 2 output dmux with common select line	X	X	X	X	X
DMUX42E	Quad 1 of 2 output dmux with common select line and enable	X	X	X	X	X
DMUX44	Quad 1 of 4 output dmux with common select line	X	X	X	X	X
DMUX44E	Quad 1 of 4 output dmux with common select line and enable	X	X	X	X	X
DMUX82	Octal 1 of 2 output dmux with common select line	X	X	X	X	X
DMUX82E	Octal 1 of 2 output dmux with common select line and enable	X	X	X	X	X
F3SUB	3-bit full subtractor with propagate-generate	X	X	X	X	X
FD11	1-bit D flip-flop	X	X	X	X	X
FD14	4-bit D flip-flop	X	X	X	X	X
FD18	8-bit D flip-flop	X	X	X	X	X
FD21	1-bit D flip-flop with async clear	X	X	X	X	X
FD24	4-bit D flip-flop with async clear	X	X	X	X	X
FD28	8-bit D flip-flop with async clear	X	X	X	X	X
FD31	1-bit D flip-flop with sync preset	X	X	X	X	X

Macro	**Description**	**1000**	**2000**	**3000**	**5000**	**8000**
FD34	4-bit D flip-flop with sync preset	X	X	X	X	X
FD38	8-bit D flip-flop with sync preset	X	X	X	X	X
FD41	1-bit D flip-flop with async clear dominant over sync preset	X	X	X	X	X
FD44	4-bit D flip-flop with async clear dominant over sync preset	X	X	X	X	X
FD48	8-bit D flip-flop with async clear dominant over sync preset	X	X	X	X	X
FD51	1-bit D flip-flop with sync preset dominant over sync clear	X	X	X	X	X
FD54	4-bit D flip-flop with sync preset dominant over sync clear	X	X	X	X	X
FD58	8-bit D flip-flop with sync preset dominant over sync clear	X	X	X	X	X
FD61	1-bit flip-flop with scan	X	X	X	X	X
FD64	4-bit flip-flop with scan	X	X	X	X	X
FD68	8-bit flip-flop with scan	X	X	X	X	X
FD71	1-bit D flip-flop with scan and async clear	X	X	X	X	X
FD74	4-bit D flip-flop with scan and async clear	X	X	X	X	X
FD78	8-bit D flip-flop with scan and async clear	X	X	X	X	X
FD81	1-bit D flip-flop with scan and sync preset	X	X	X	X	X
FD84	4-bit D flip-flop with scan and sync preset	X	X	X	X	X

Macro	Description	1000	2000	3000	5000	8000
FD88	8-bit D flip-flop with scan and sync preset	X	X	X	X	X
FD91	1-bit D flip-flop with scan and async clear dominant over sync preset	X	X	X	X	X
FD94	4-bit D flip-flop with scan and async clear dominant over sync preset	X	X	X	X	X
FD98	8-bit D flip-flop with scan and async clear dominant over sync preset	X	X	X	X	X
FDA1	1-bit D flip-flop with scan and sync preset dominant over async clear	X	X	X	X	X
FDA4	4-bit D flip-flop with scan and sync preset dominant over async clear	X	X	X	X	X
FDA8	8-bit D flip-flop with scan and sync preset dominant over async clear	X	X	X	X	X
FJK11	JK flip-flop	X	X	X	X	X
FJK21	JK flip-flop with async clear	X	X	X	X	X
FJK31	JK flip-flop with scan	X	X	X	X	X
FJK41	JK flip-flop with scan and async clear	X	X	X	X	X
FJK51	JK flip-flop with async clear and sync preset	X	X	X	X	X
FT11	Toggle flip-flop with async clear	X	X	X	X	X
FT21	Toggle flip-flop with sync clear and preset, preset dominant	X	X	X	X	X
IB11	1-bit input pin	X	X	X	X	X
ID11	1-bit registered input pin	X	X	X		X
ID14	Four ID11s with common clock	X	X	X		X

Macro	**Description**	**1000**	**2000**	**3000**	**5000**	**8000**
ID18	Eight ID11s with common clock	X	X	X		X
ID21	1-bit registered input pin with inverted clock	X	X	X		X
ID24	Four ID21s with common clock	X	X	X		X
ID28	Eight ID21s with common clock	X	X	X		X
IL11	1-bit input pin with D latch on input	X	X	X		X
IL14	Four IL11s with common G	X	X	X		X
IL18	Eight IL11s with common G	X	X	X		X
IL21	1-bit input pin with D latch on input, inverted enable	X	X	X		X
IL24	Four IL21s with common G	X	X	X		X
IL28	Eight IL21s with common G	X	X	X		X
INV	Single input inverter	X	X	X	X	X
LD11	1-bit D latch	X	X	X	X	X
LD14	4-bit D latch	X	X	X	X	X
LD18	8-bit D latch	X	X	X	X	X
LD21	1-bit D latch with async clear	X	X	X	X	X
LD24	4-bit D latch with async clear	X	X	X	X	X
LD28	8-bit D latch with async clear	X	X	X	X	X
LD31	1-bit D latch with async preset	X	X	X	X	X
LD34	4-bit D latch with async preset	X	X	X	X	X
LD38	8-bit D latch with async preset	X	X	X	X	X
LD41	1-bit D latch with async clear dominant over async preset	X	X	X	X	X
LD44	4-bit D latch with async clear dominant over async preset	X	X	X	X	X

Macro	Description	1000	2000	3000	5000	8000
LD48	8-bit D latch with async clear dominant over async preset	X	X	X	X	X
LD51	1-bit D latch with async preset dominant over async clear	X	X	X	X	X
LD54	4-bit D latch with async preset dominant over async clear	X	X	X	X	X
LD58	8-bit D latch with async preset dominant over async clear	X	X	X	X	X
LD61	1-bit D latch with scan	X	X	X	X	X
LD64	4-bit D latch with scan	X	X	X	X	X
LD68	8-bit D latch with scan	X	X	X	X	X
LD71	1-bit D latch with scan and async clear	X	X	X	X	X
LD74	4-bit D latch with scan and async clear	X	X	X	X	X
LD78	8-bit D latch with scan and async clear	X	X	X	X	X
LD81	1-bit D latch with scan and async preset	X	X	X	X	X
LD84	4-bit D latch with scan and async preset	X	X	X	X	X
LD88	8-bit D latch with scan and async preset	X	X	X	X	X
LD91	1-bit D latch with scan and async clear dominant over async preset	X	X	X	X	X
LD94	4-bit D latch with scan and async clear dominant over async preset	X	X	X	X	X
LD98	8-bit D latch with scan and async clear dominant over async preset	X	X	X	X	X

Macro	Description	1000	2000	3000	5000	8000
LDA1	1-bit D latch with scan and async preset dominant over async clear	X	X	X	X	X
LDA4	4-bit D latch with scan and async preset dominant over async clear	X	X	X	X	X
LDA8	8-bit D latch with scan and async preset dominant over async clear	X	X	X	X	X
LSR1	Simple SR latch	X	X	X	X	X
LSR2	SR latch with OR on S and R inputs	X	X	X	X	X
LXOR2	XOR gate	X	X	X	X	X
MAG2	2-bit magnitude comparator	X	X	X	X	X
MAG4	4-bit magnitude comparator	X	X	X	X	X
MAG8	8-bit magnitude comparator	X	X	X	X	X
MULT24	2-bit by 4-bit multiplier	X	X	X	X	X
MULT44	4-bit by 4-bit multiplier	X	X	X	X	X
MUX2	1 of 2 input mux	X	X	X	X	X
MUX2E	1 of 2 input mux with enable	X	X	X	X	X
MUX4	1 of 4 input mux	X	X	X	X	X
MUX4E	1 of 4 input mux with enable	X	X	X	X	X
MUX8	1 of 8 input mux	X	X	X	X	X
MUX8E	1 of 8 input mux with enable	X	X	X	X	X
MUX16	1 of 16 input mux	X	X	X	X	X
MUX16E	1 of 16 input mux with enable	X	X	X	X	X
MUX22	Dual 1 of 2 input mux with common select line	X	X	X	X	X
MUX22E	Dual 1 of 2 input mux with common select line and enable	X	X	X	X	X

Macro	Description	1000	2000	3000	5000	8000
MUX24	Dual 1 of 4 input mux with common select line	X	X	X	X	X
MUX24E	Dual 1 of 4 input mux with common select line and enable	X	X	X	X	X
MUX42	Quad 1 of 2 input mux with common select line	X	X	X	X	X
MUX42E	Quad 1 of 2 input mux with common select line and enable	X	X	X	X	X
MUX44	Quad 1 of 4 input mux with common select line	X	X	X	X	X
MUX44A	Quad 1 of 4 input mux with common select line	X	X	X	X	X
MUX44AE	Quad 1 of 4 input mux with common select line and enable	X	X	X	X	X
MUX44E	Quad 1 of 4 input mux with common select line and enable	X	X	X	X	X
MUX82	Octal 1 of 2 input mux with common select line	X	X	X	X	X
MUX82E	Octal 1 of 2 input mux with common select line and enable	X	X	X	X	X
NAND2 through NAND12 & NAND16	2 through 12 and 16-input NAND gate	X	X	X	X	X
NOR2 through NOR12 & NOR16	2 though 12 and 16-input NOR gate	X	X	X	X	X
OB11	1-bit output pin	X	X	X	X	X
OB21	1-bit inverting output pin	X	X	X	X	X
OB24	Four OB21s	X	X	X	X	X
OB28	Eight OB21s	X	X	X	X	X

Macro	**Description**	**1000**	**2000**	**3000**	**5000**	**8000**
OR2 through OR12 & OR16	1 through 12 and 16-input OR gate	X	X	X	X	X
OT11	1-bit 3-state output pin	X	X	X	X	X
OT14	Four OT11s with common Output Enable	X	X	X	X	X
OT18	Eight OT11s with common Output Enable	X	X	X	X	X
OT21	1-bit inverting 3-state output pin	X	X	X	X	X
OT24	Four OT21s with common Output Enable	X	X	X	X	X
OT28	Eight OT21s with common Output Enable	X	X	X	X	X
OT31	1-bit 3-state output pin with active low enable	X	X	X	X	X
OT34	Four OT31s with common Output Enable	X	X	X	X	X
OT38	Eight OT31s with common Output Enable	X	X	X	X	X
OT41	1-bit inverting 3-state output pin with active low enable	X	X	X	X	X
OT44	Four OT41s with common Output Enable	X	X	X	X	X
OT48	Eight OT41s with common Output Enable	X	X	X	X	X
PG1	1-bit propagate-generate	X	X	X	X	X
PG2	2-bit propagate-generate	X	X	X	X	X
PG3	3-bit propagate-generate	X	X	X	X	X
PG4	4-bit propagate-generate	X	X	X	X	X
PREN8	7-line to 3-line priority encoder	X	X	X	X	X
PREN8E	7-line to 3-line priority encoder with enable	X	X	X	X	X

Macro	Description	1000	2000	3000	5000	8000
PREN10	9-line to 4-line priority encoder	X	X	X	X	X
PREN10E	9-line to 4-line priority encoder with enable	X	X	X	X	X
PREN16	15-line to 4-line priority encoder	X	X	X	X	X
PREN16E	15-line to 4-line priority encoder with enable	X	X	X	X	X
SRR11	1-bit right shift register with async reset	X	X	X	X	X
SRR14	4-bit right shift register with async reset	X	X	X	X	X
SRR18	8-bit right shift register with async reset	X	X	X	X	X
SRR21	1-bit right shift register with async reset and enable	X	X	X	X	X
SRR24	4-bit right shift register with async reset and enable	X	X	X	X	X
SRR28	8-bit right shift register with async reset and enable	X	X	X	X	X
SRR31	1-bit right shift register with async reset, enable, parallel data load, and sync preset	X	X	X	X	X
SRR34	4-bit right shift register with async reset, enable, parallel data load, and sync preset	X	X	X	X	X
SRR38	8-bit right shift register with async reset, enable, parallel data load, and sync preset	X	X	X	X	X
SRR41	1-bit right shift register with sync reset, enable, parallel data load, and sync preset	X	X	X	X	X
SRR44	4-bit right shift register with sync reset, enable, parallel data load, and sync preset	X	X	X	X	X

Macro	Description	1000	2000	3000	5000	8000
SRR48	8-bit right shift register with sync reset, enable, parallel data load, and sync preset	X	X	X	X	X
SRRL1	1-bit right/left shift register with async reset, enable, parallel data load, and sync preset	X	X	X	X	X
SRRL4	4-bit right/left shift register with async reset, enable, parallel data load, and sync preset	X	X	X	X	X
SRRL8	8-bit right/left shift register with async reset, enable, parallel data load, and sync preset	X	X	X	X	X
SUBF1	1-bit full subtractor	X	X	X	X	X
SUBF2	2-bit full subtractor	X	X	X	X	X
SUBF4	4-bit full subtractor	X	X	X	X	X
SUBF8	8-bit full subtractor	X	X	X	X	X
SUBF8A	8-bit full subtractor with propagate-generate	X	X	X	X	X
SUBF16A	16-bit full subtractor with propagate-generate	X	X	X	X	X
SUBH1	1-bit half subtractor	X	X	X	X	X
SUBH2	2-bit half subtractor	X	X	X	X	X
SUBH3	3-bit half subtractor	X	X	X	X	X
SUBH4	4-bit half subtractor	X	X	X	X	X
SUBH8	8-bit half subtractor	X	X	X	X	X
SUBH8A	8-bit half subtractor built with propagate-generate submacro	X	X	X	X	X
SUBH16A	16-bit half subtractor built with propagate-generate submacro	X	X	X	X	X
XNOR2	Input XNOR gate	X	X	X	X	X

Macro	**Description**	**1000**	**2000**	**3000**	**5000**	**8000**
XNOR3	Input XNOR gate	X	X	X	X	X
XNOR4	Input XNOR gate	X	X	X	X	X
XNOR7	Input XNOR gate	X	X	X	X	X
XNOR8	Input XNOR gate	X	X	X	X	X
XNOR9	Input XNOR gate	X	X	X	X	X
XOR2	Input XOR gate	X	X	X	X	X
XOR3	Input XOR gate	X	X	X	X	X
XOR4	Input XOR gate	X	X	X	X	X
XOR8	Input XOR gate	X	X	X	X	X
XOR9	Input XOR gate	X	X	X	X	X

* CAO is a 2-level output (1 logic level and 1 CO delay).

** ADDF8: CO is a 3-level output.

*** SUBF8: BO is a 3-level output.

Arithmetic Functions

This chapter contains information on the following macros:

- Adders
- Comparators
- Multipliers
- Propagate-Generate
- Subtractors

Adders

ADDF1, ADDF2, F3ADD, ADDF4, ADDF8, ADDF8A, and ADDF16A

Function:

ADDF1:	1-bit full adder.
ADDF2:	2-bit full adder.
F3ADD:	3-bit full adder with propagate-generate.
ADDF4:	4-bit full adder.
ADDF8:	8-bit full adder.
ADDF8A:	8-bit full adder built with propagate-generate submacros.
ADDF16A:	16-bit full adder built with propagate-generate submacros.

Availability:

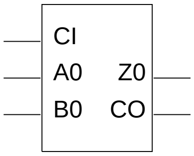
ADDF1, ADDF2, F3ADD, ADDF4, ADDF8, ADDF8A, and ADDF16A can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Additional symbols and schematics appear on the following pages.

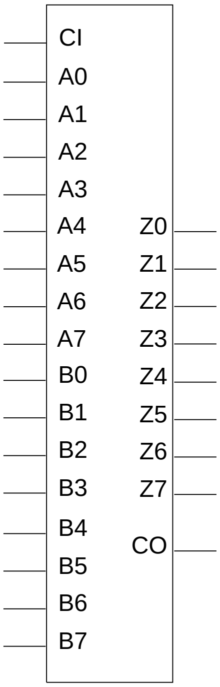
Type:

Soft:	ADDF1, ADDF2, F3ADD, ADDF8A, ADDF16A
Hard:	ADDF4, ADDF8

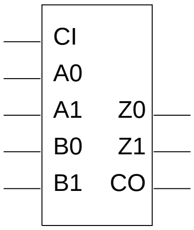
ADDF1



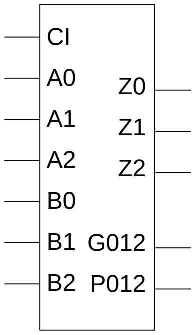
ADDF8



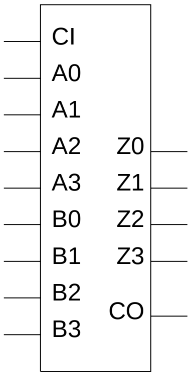
ADDF2



F3ADD



ADDF4

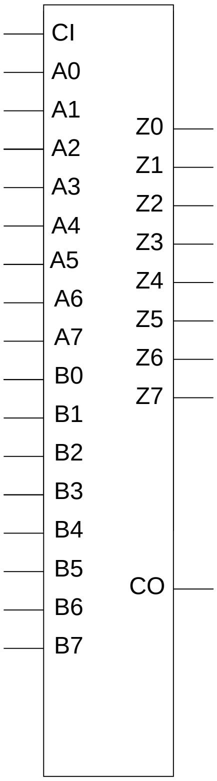


Logic Resources:

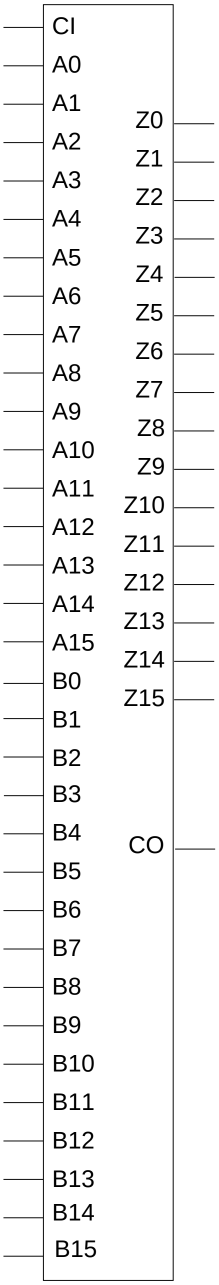
Macro	PT	GLB	Output	Level
ADDF4	****	2	6	2
ADDF8	*****	9	27	3

****	Z0: 4 PT	Z1: 7 PT	Z2: 4 PT
	Z3: 7 PT	CO: 7 PT	TCO: 7 PT
*****	Z0: 2 PT	Z1: 3 PT	Z2: 4 PT
	Z3: 5 PT	Z4: 6 PT	Z5: 7 PT
	Z6: 7 PT	Z7: 7 PT	CO: 6 PT
	CA: 3 PT	CB: 3 PT	CC: 7 PT
	G0-G6: 1 PT	P0-P7: 2 PT	

ADDF8A



ADDF16A



Macro Port Definition:

```
ADDF1 (Z0,CAO,A0,B0,CI);
ADDF2 (Z0,Z1,CO,A0,A1,B0,B1,CI);
F3ADD ([Z0..Z2],G012,P012,A0,A1,A2,B0,B1,B2,CI);
  F3ADD_1 (Z0,Z1,G012,A0,A1,A2,B0,B1,B2,CI);
  F3ADD_2 (Z2,P012,A0,A1,A2,B0,B1,B2,CI);
ADDF4 ([Z0..Z3],CO,[A0..A3],[B0..B3],CI);
  ADDF4_1 (Z0,Z1,TCO,A0,A1,B0,B1,CI);
  ADDF4_2 (Z2,Z3,CO,A2,A3,B2,B3,TCO);
ADDF8 ([Z0..Z7],CO,[A0..A7],[B0..B7],CI);
  ADDF8_1 (CO,[P0..P7],[G0..G3],CC,CI);
  ADDF8_2 (Z7,[P0..P7],[G0..G3],A3,B3,CI,CA);
  ADDF8_3 (Z6,[P0..P6],G0,G1,A0,A2,B0,B2,CI,CB);
  ADDF8_4 (Z5,[P0..P6],G0,G1,G3,A2,A4,A6,B2,B4,B6,CI);
  ADDF8_5 (Z2,Z4,[P0..P4],[G0..G2],G4,A1,A3,A4,B1,B3,B4,CI);
  ADDF8_6 (Z3,[P0..P3],G1,G2,G5,G6,A0,A1,A5,A6,B0,B1,B5,B6,CI);
  ADDF8_7 (Z0,P7,G2,CC,P0,P5,P6,G4,G5,G6,A2,A7,B2,B7,CI);
  ADDF8_8 (Z1,CA,CB,P5,P0,P1,P4,P6,[G3..G6],A0,A5,B0,B5,CI);
ADDF8A ([Z0..Z7],CO,[A0..A7],[B0..B7],CI);
  ADDF8A_1 (Z0,Z1,G012,A0,A1,A2,B0,B1,B2,CI);
  ADDF8A_2 (Z2,P012,A0,A1,A2,B0,B1,B2,CI);
  ADDF8A_3 (C2,CCI,CI,P012,P345,G012,G345);
  ADDF8A_4 (Z3,Z4,G345,A3,A4,A5,B3,B4,B5,C2);
  ADDF8A_5 (Z5,P345,A3,A4,A5,B3,B4,B5,C2);
  ADDF8A_6 (CO,Z6,Z7,A6,A7,B6,B7,CCI);
ADDF16A ([Z0..Z15],CO,[A0..A15],[B0..B15],CI);
  ADDF16A_1 (Z0,Z1,G012,A0,A1,A2,B0,B1,B2,CI);
  ADDF16A_2 (Z2,P012,A0,A1,A2,B0,B1,B2,CI);
  ADDF16A_3 (Z3,Z4,G345,A3,A4,A5,B3,B4,B5,C2);
  ADDF16A_4 (Z5,P345,A3,A4,A5,B3,B4,B5,C2);
  ADDF16A_5 (Z6,Z7,G678,A6,A7,A8,B6,B7,B8,C5);
  ADDF16A_6 (Z8,P678,A6,A7,A8,B6,B7,B8,C5);
  ADDF16A_7 (Z9,Z10,G911,A9,A10,A11,B9,B10,B11,C8);
  ADDF16A_8 (Z11,P911,A9,A10,A11,B9,B10,B11,C8);
  ADDF16A_9 (Z12,Z13,G1214,A12,A13,A14,B12,B13,B14,C11);
  ADDF16A_10 (Z14,P1214,A12,A13,A14,B12,B13,B14,C11);
  ADDF16A_11 (Z15,CO,C2,CI,P012,G012,A15,B15,C14);
  ADDF16A_12 (C5,C8,C11,C14,C2,P345,G345,P678,G678,
              P911,G911,P1214,G1214);
```

Truth Table:

The truth table below applies to ADDF1, ADDF2, ADDF4, ADDF8, ADDF8A, and ADDF16A. The value of CO depends on the sum of A+B and n.

Input			Output	
A_{n-1}~A0	B_{n-1}~B0	CI	Z_{n-1}~Z0	CO
data	data	0	A+B	*
data	data	1	A+B+1	**

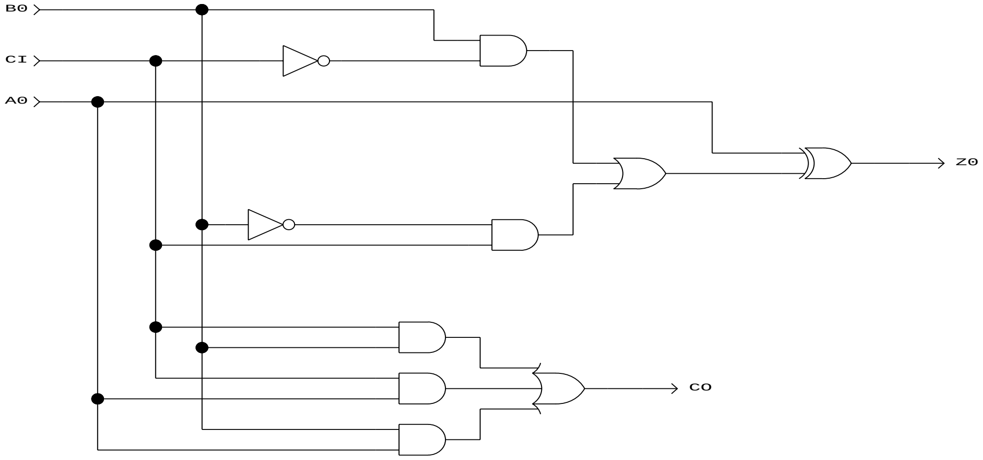
* If A+B<2^n, CO = 0. If A+B$\geq 2^n$, CO = 1.
** If A+B+1<2^n, CO = 0. If A+B+1$\geq 2^n$, CO = 1.

The truth table for F3ADD is shown below.

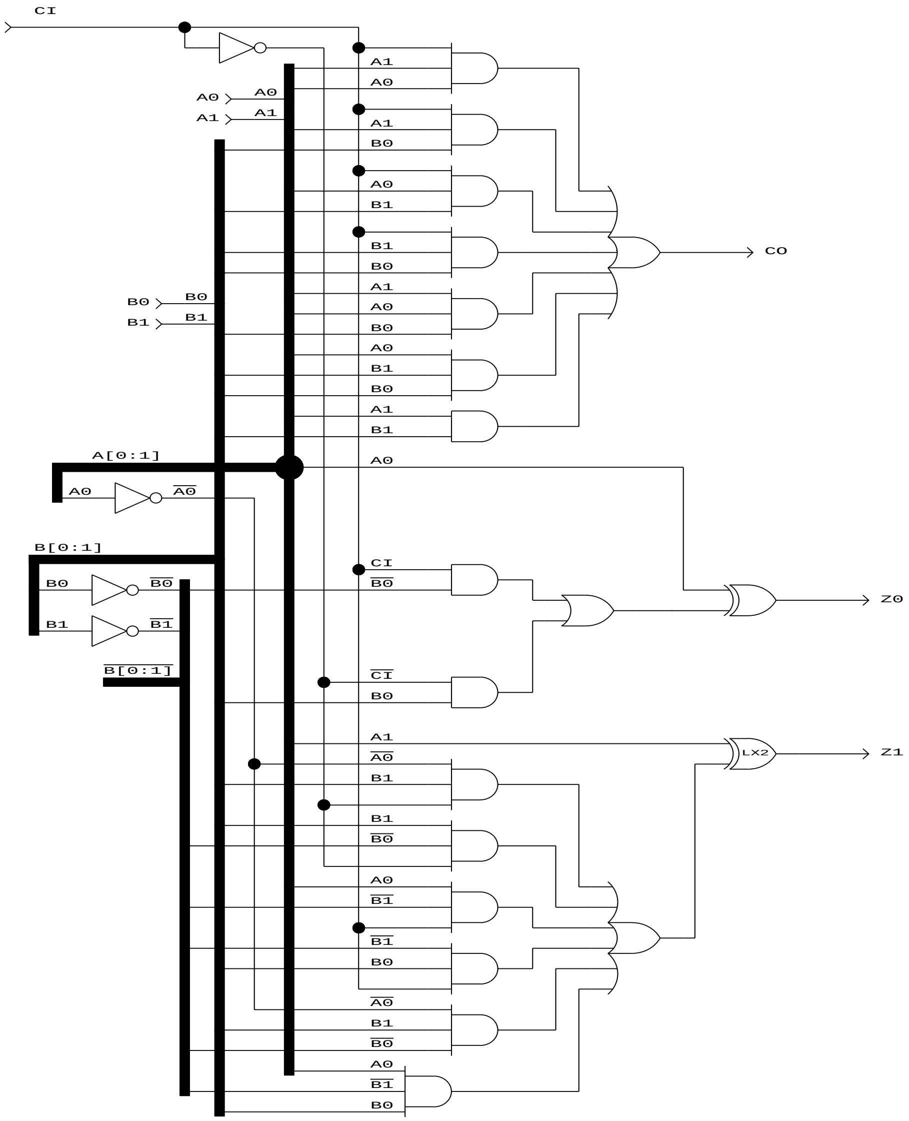
Input			Output		
A_2~A0	B_2~B0	CI	Z_2~Z0	G012	P012
data	data	0	A+B	*	***
data	data	1	A+B+1	**	***

* If A+B<2^n, G012 = 0. If A+B$\geq 2^n$, G012 = 1.
** If A+B+1<2^n, G012 = 0. If A+B+1$\geq 2^n$, G012 = 1.
*** P012 = (A0+B0) (A1+B1) (A2+B2).

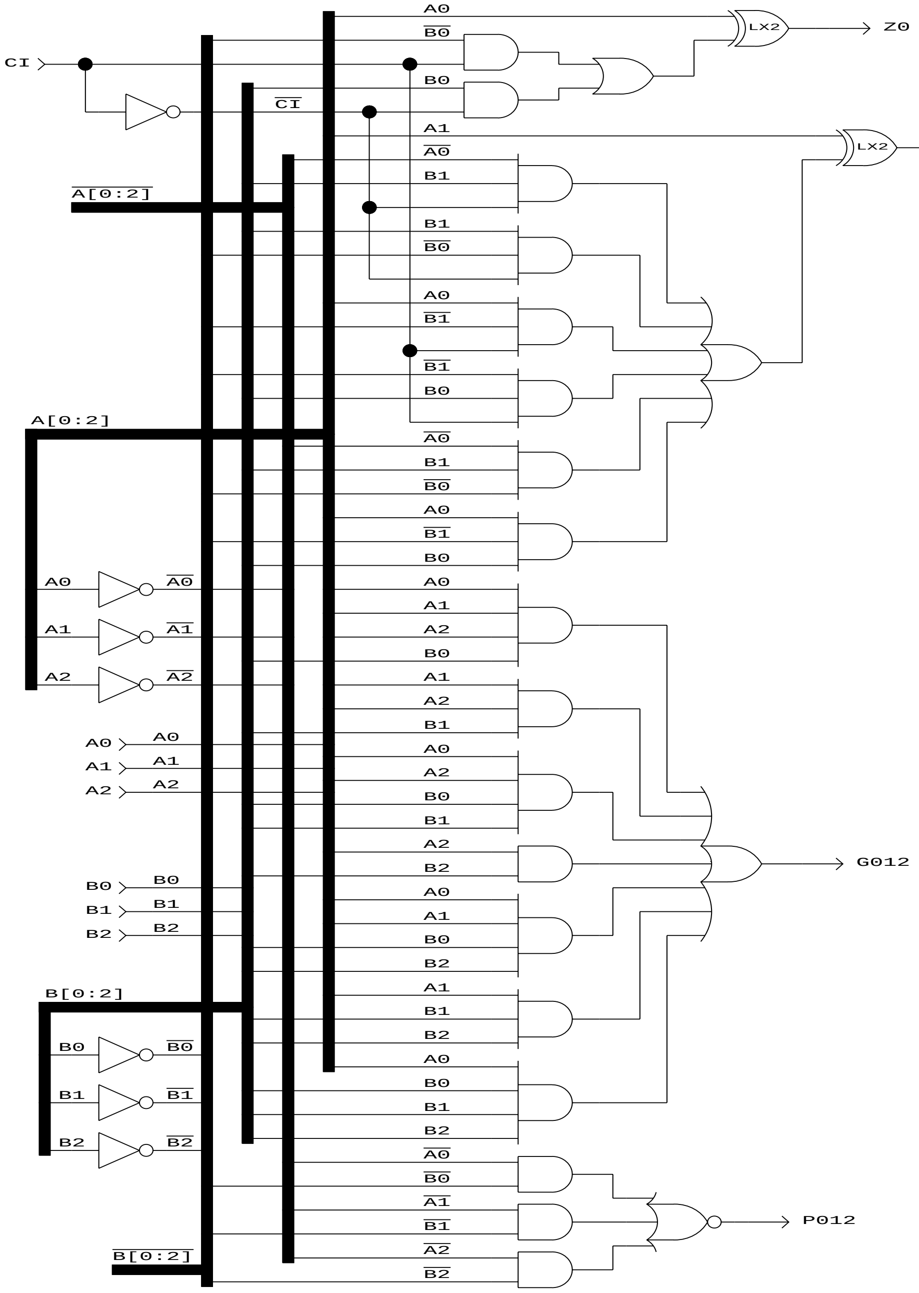
ADDF1



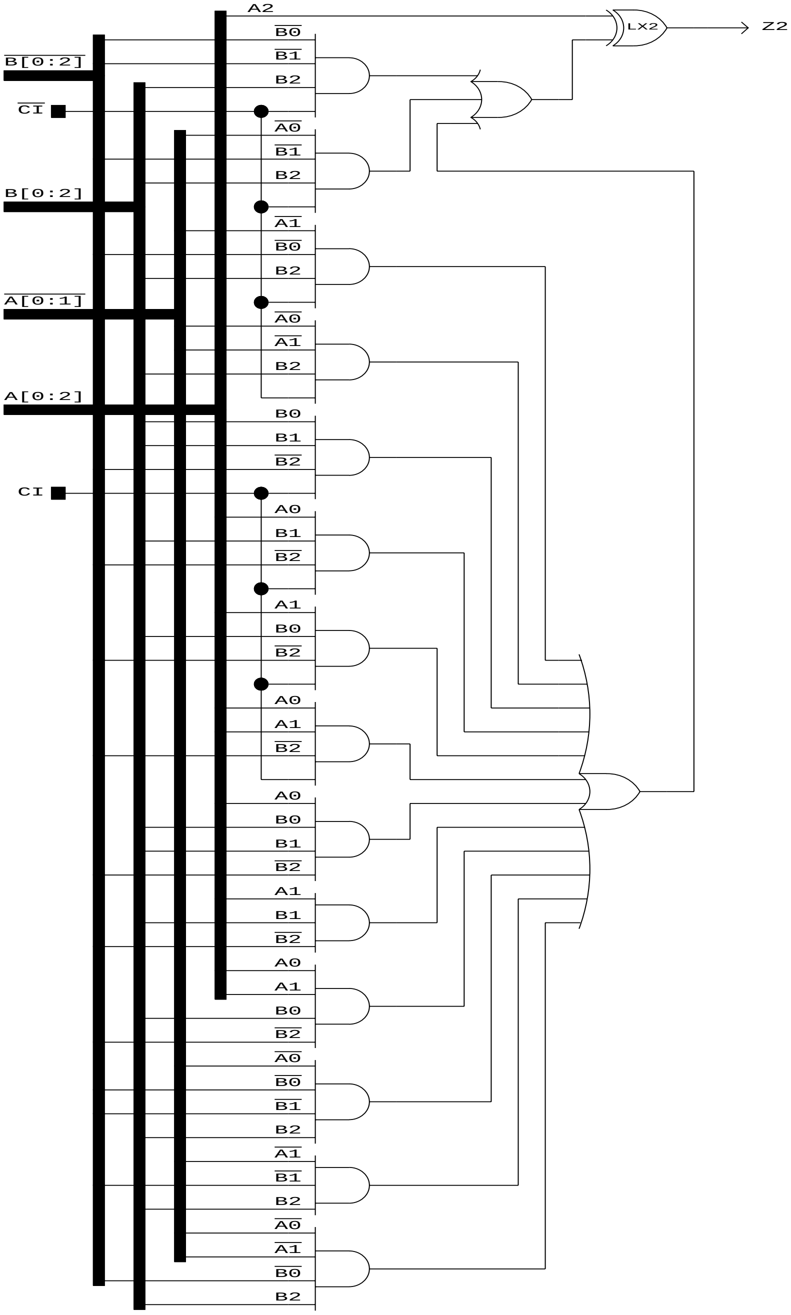
ADDF2


CI
A0
A0
A1
A1
A1
A0
A1
B0
A0
B1
B1
B0
A1
A0
B0
A0
B1
B0
A1
B1
CO
B0
B0
B1
B1
A[0:1]
A0
A0
$\overline{A0}$
B[0:1]
B0
$\overline{B0}$
B1
$\overline{B1}$
$\overline{B[0:1]}$
CI
$\overline{B0}$
Z0
$\overline{CI}$
B0
A1
$\overline{A0}$
LX2
Z1
B1
B1
$\overline{B0}$
A0
$\overline{B1}$
$\overline{B1}$
B0
$\overline{A0}$
B1
$\overline{B0}$
A0
$\overline{B1}$
B0

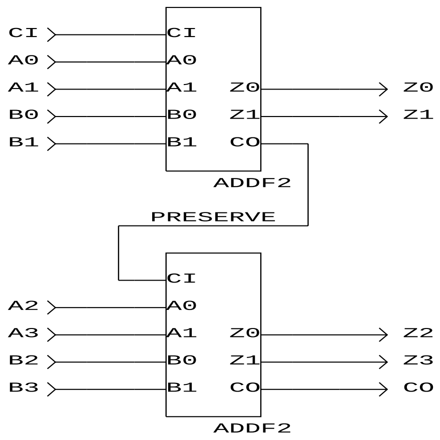
F3ADD.1


A0
$\overline{B0}$
CI
B0
$\overline{CI}$
LX2
Z0
A1
$\overline{A0}$
B1
LX2
Z1
$\overline{A[0:2]}$
B1
$\overline{B0}$
A0
$\overline{B1}$
$\overline{B1}$
B0
A[0:2]
$\overline{A0}$
B1
$\overline{B0}$
A0
$\overline{B1}$
B0
A0
$\overline{A0}$
A0
A1
$\overline{A1}$
A1
A2
A2
$\overline{A2}$
B0
A1
A2
B1
A0
A0
A0
A1
A1
A2
A2
A2
B0
B1
A2
B2
G012
B0
B0
A0
B1
B1
A1
B2
B2
B0
B2
B[0:2]
A1
B0
$\overline{B0}$
B1
B2
B1
$\overline{B1}$
A0
B0
B2
$\overline{B2}$
B1
B2
$\overline{A0}$
$\overline{B0}$
$\overline{A1}$
P012
$\overline{B1}$
$\overline{A2}$
$\overline{B[0:2]}$
$\overline{B2}$

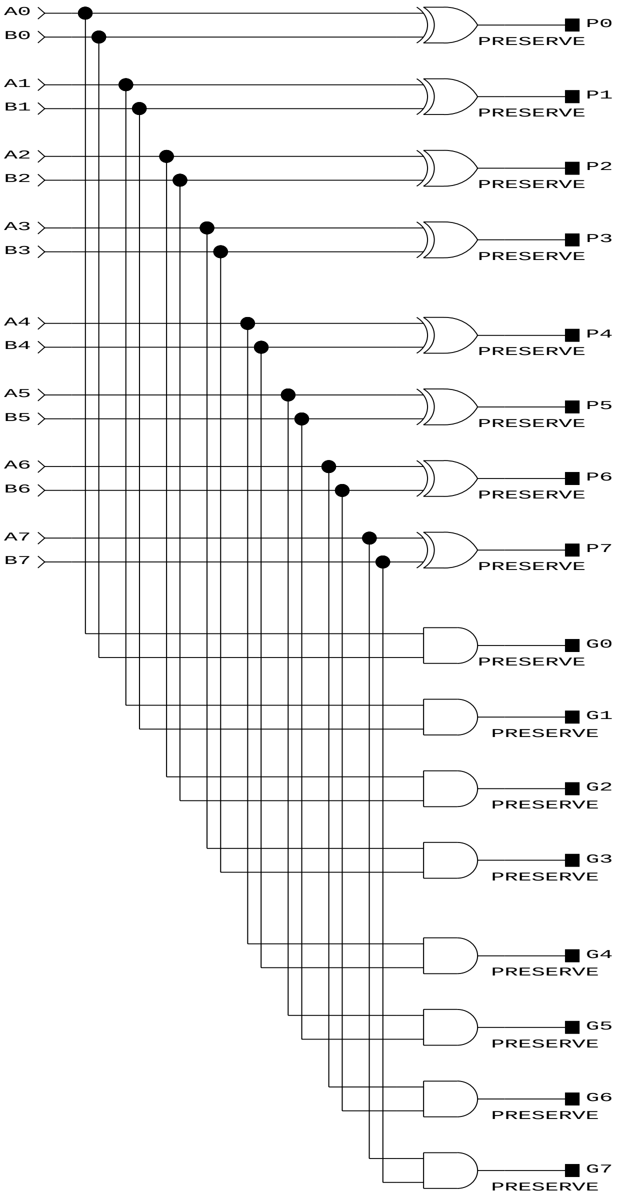
F3ADD.2


$\overline{B[0:2]}$
$\overline{CI}$
B[0:2]
$\overline{A[0:1]}$
A[0:2]
CI
A2
$\overline{B0}$
$\overline{B1}$
B2
$\overline{A0}$
$\overline{B1}$
B2
$\overline{A1}$
$\overline{B0}$
B2
$\overline{A0}$
$\overline{A1}$
B2
B0
B1
$\overline{B2}$
A0
B1
$\overline{B2}$
A1
B0
$\overline{B2}$
A0
A1
$\overline{B2}$
A0
B0
B1
$\overline{B2}$
A1
B1
$\overline{B2}$
A0
A1
B0
$\overline{B2}$
$\overline{A0}$
$\overline{B0}$
$\overline{B1}$
B2
$\overline{A1}$
$\overline{B1}$
B2
$\overline{A0}$
$\overline{A1}$
$\overline{B0}$
B2
LX2
Z2

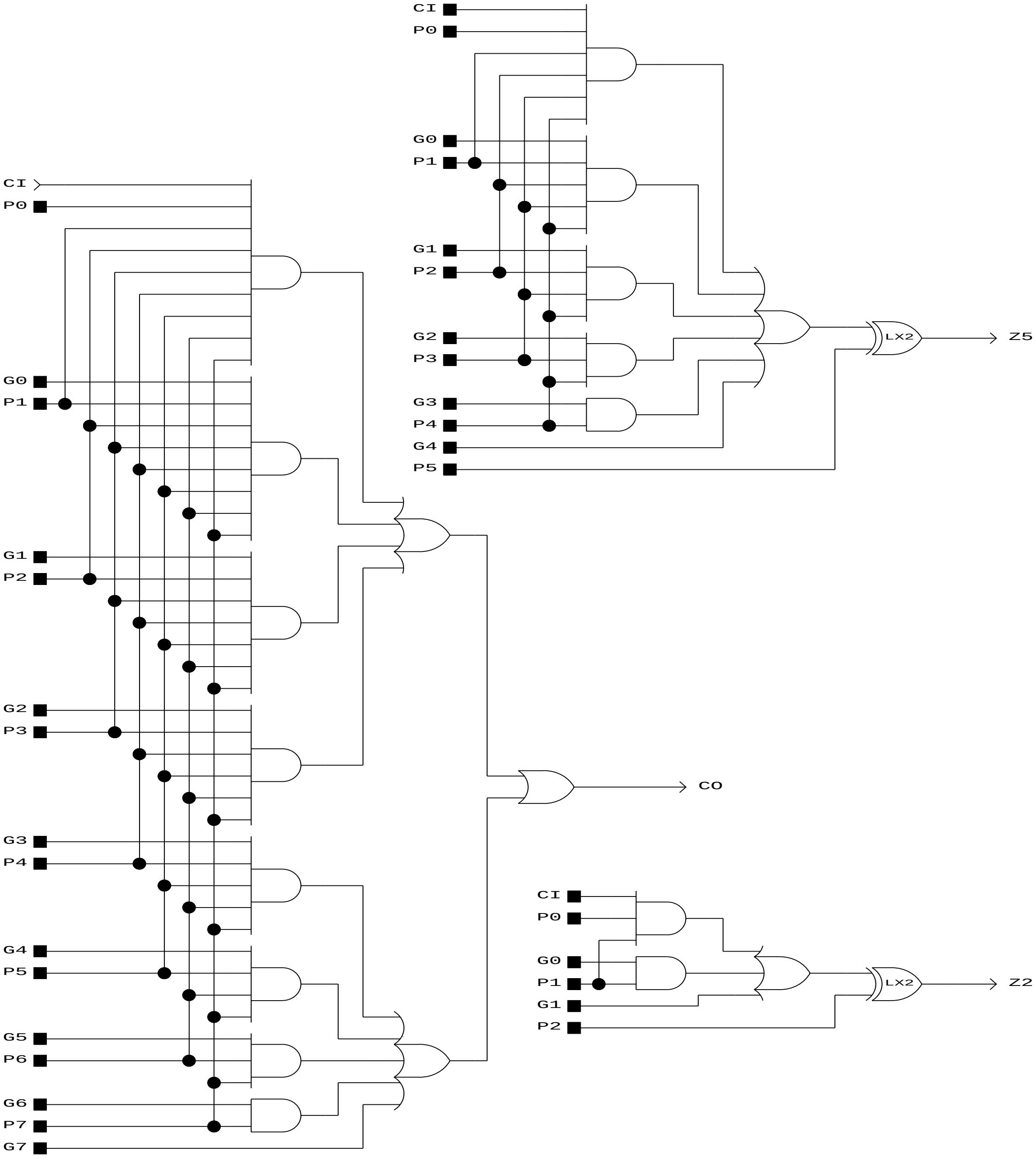
ADDF4


CI
A0
A1
B0
B1
CI
A0
A1
B0
B1
Z0
Z1
CO
Z0
Z1
ADDF2
PRESERVE
A2
A3
B2
B3
CI
A0
A1
B0
B1
Z0
Z1
CO
Z2
Z3
CO
ADDF2

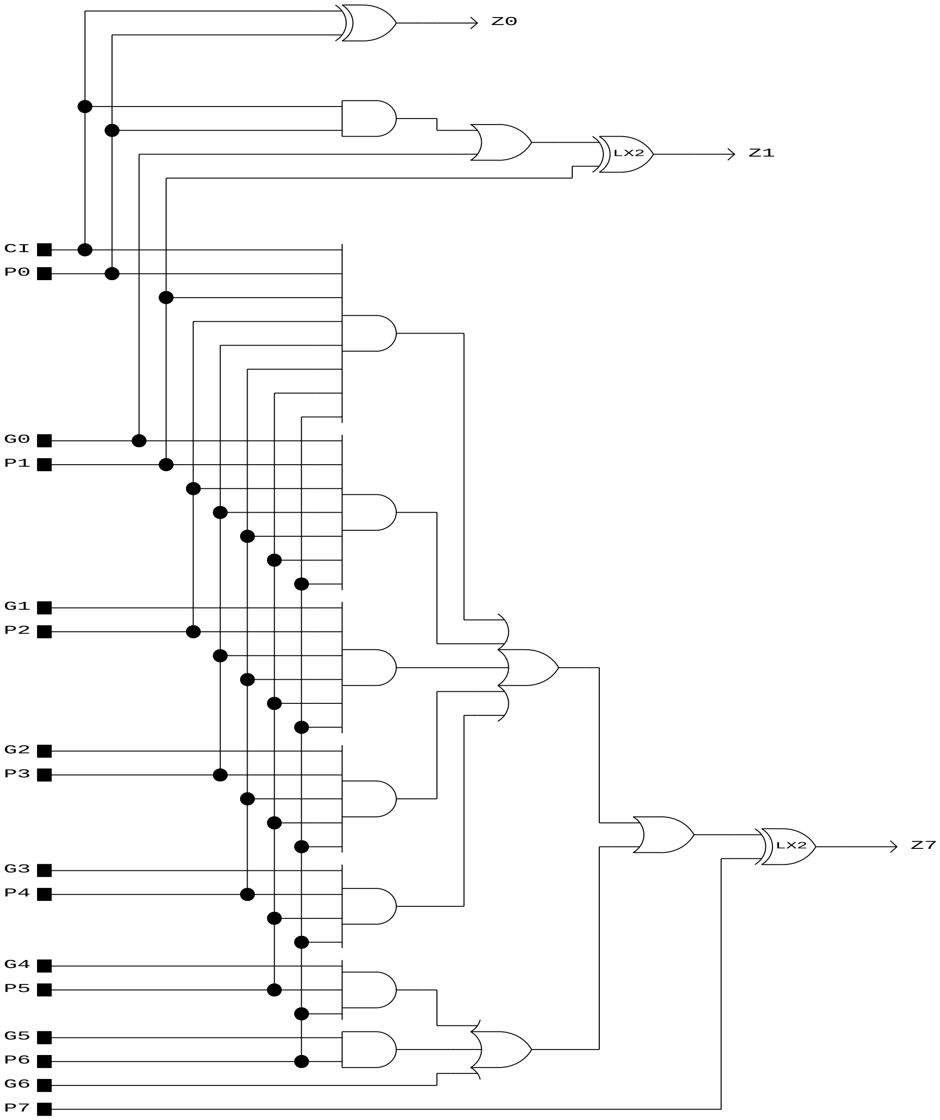
ADDF8.1


A0
B0
A1
B1
A2
B2
A3
B3
A4
B4
A5
B5
A6
B6
A7
B7
P0
P1
P2
P3
P4
P5
P6
P7
G0
G1
G2
G3
G4
G5
G6
G7
PRESERVE

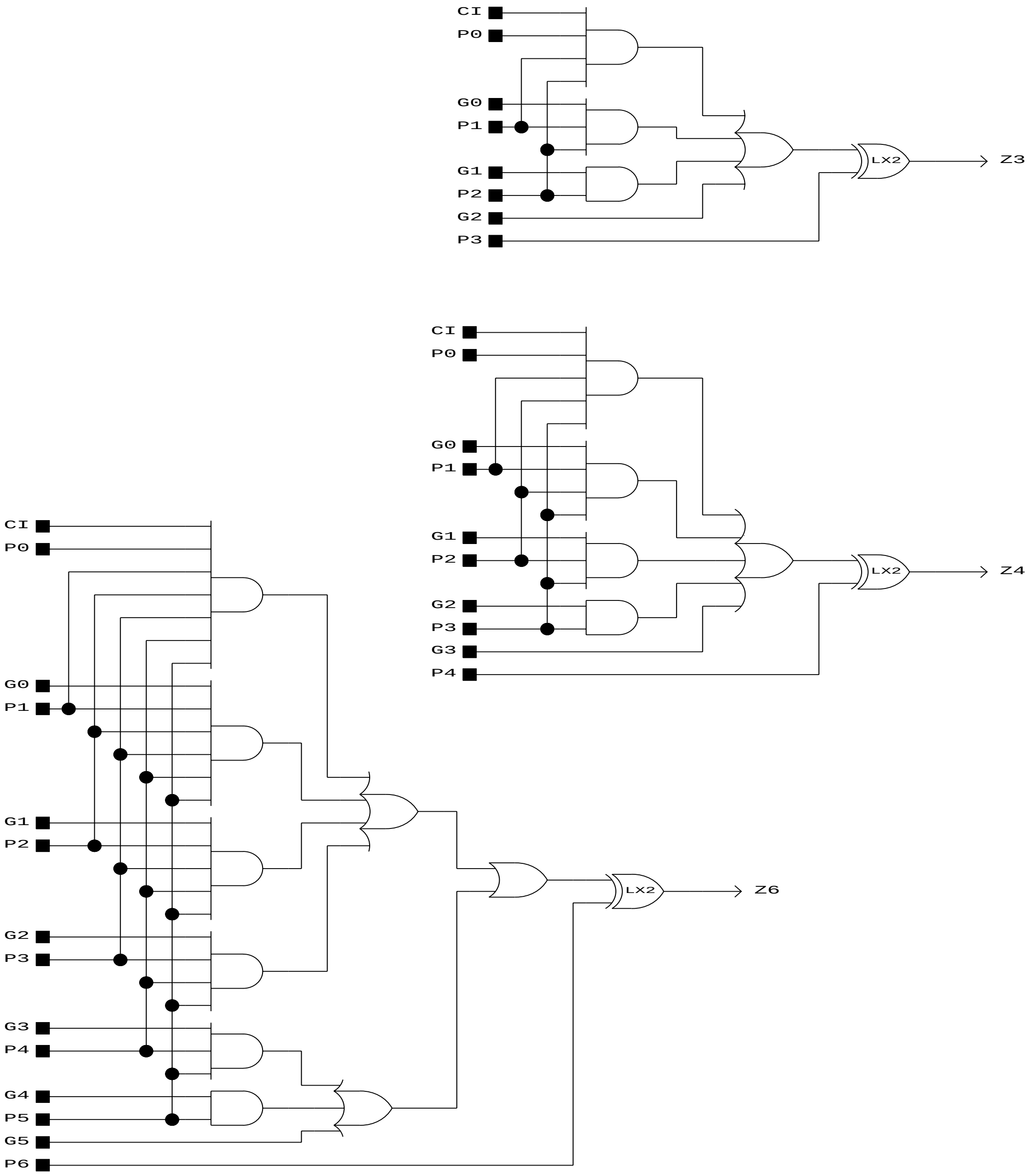
ADDF8.2


CI
P0
G0
P1
G1
P2
G2
P3
G3
P4
G4
P5
LX2
Z5
CI
P0
G0
P1
G1
P2
G2
P3
G3
P4
G4
P5
G5
P6
G6
P7
G7
CO
CI
P0
G0
P1
G1
P2
LX2
Z2

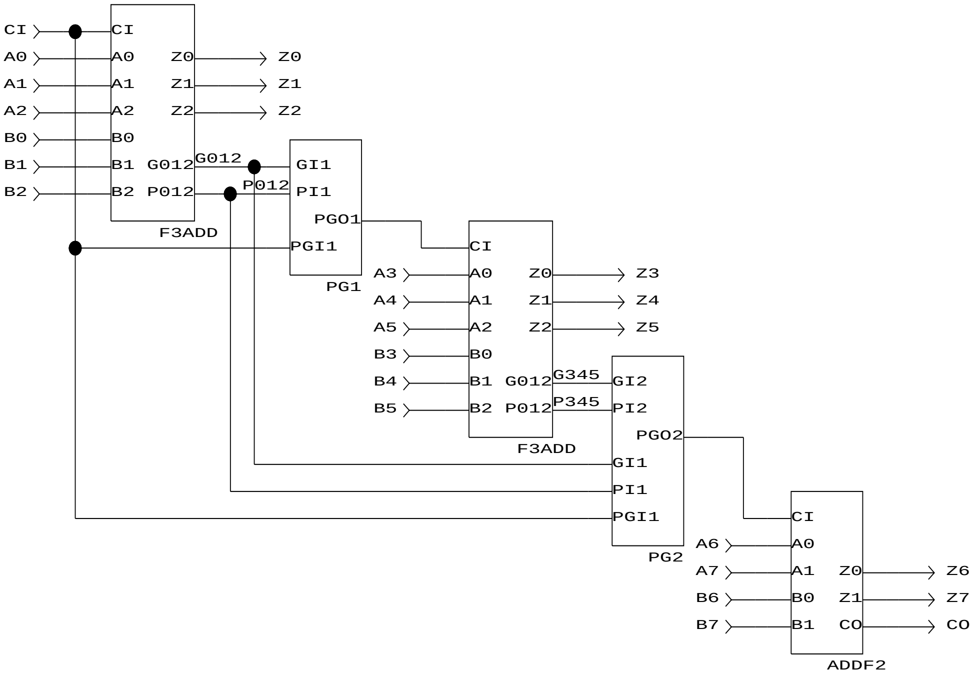
ADDF8.3



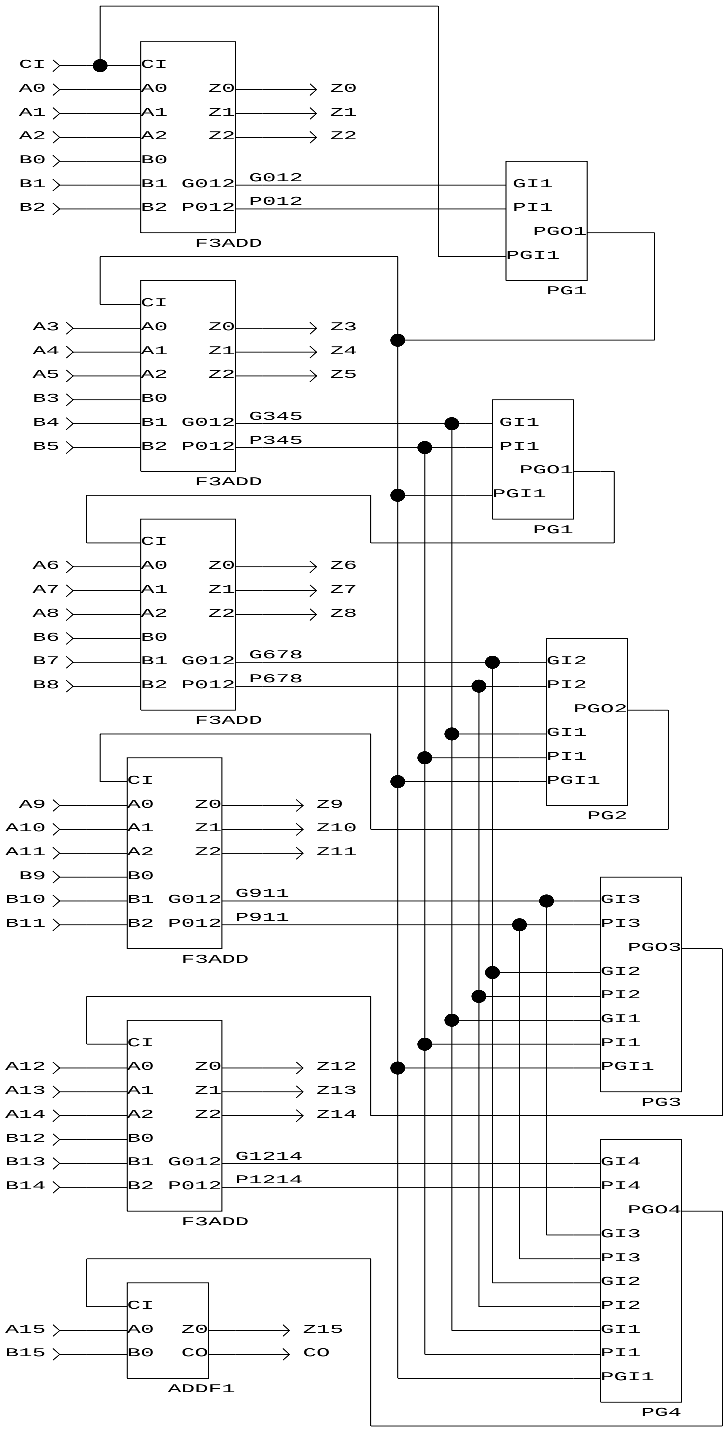
ADDF8.4


CI
P0
G0
P1
G1
P2
G2
P3
LX2
Z3
CI
P0
G0
P1
G1
P2
G2
P3
G3
P4
LX2
Z4
CI
P0
G0
P1
G1
P2
G2
P3
G3
P4
G4
P5
G5
P6
LX2
Z6

ADDF8A


CI
A0
A1
A2
B0
B1
B2
CI
A0
A1
A2
B0
B1
B2
Z0
Z1
Z2
G012
P012
F3ADD
Z0
Z1
Z2
G012
P012
GI1
PI1
PGO1
PGI1
PG1
A3
A4
A5
B3
B4
B5
CI
A0
A1
A2
B0
B1
B2
Z0
Z1
Z2
G012
P012
F3ADD
Z3
Z4
Z5
G345
P345
GI2
PI2
PGO2
GI1
PI1
PGI1
PG2
A6
A7
B6
B7
CI
A0
A1
B0
B1
Z0
Z1
CO
ADDF2
Z6
Z7
CO

ADDF16 A


CI
A0
A1
A2
B0
B1
B2
CI
A0
A1
A2
B0
B1
B2
Z0
Z1
Z2
G012
P012
Z0
Z1
Z2
G012
P012
F3ADD
GI1
PI1
PGO1
PGI1
PG1
A3
A4
A5
B3
B4
B5
CI
A0
A1
A2
B0
B1
B2
Z0
Z1
Z2
G012
P012
Z3
Z4
Z5
G345
P345
F3ADD
GI1
PI1
PGO1
PGI1
PG1
A6
A7
A8
B6
B7
B8
CI
A0
A1
A2
B0
B1
B2
Z0
Z1
Z2
G012
P012
Z6
Z7
Z8
G678
P678
F3ADD
GI2
PI2
PGO2
GI1
PI1
PGI1
PG2
A9
A10
A11
B9
B10
B11
CI
A0
A1
A2
B0
B1
B2
Z0
Z1
Z2
G012
P012
Z9
Z10
Z11
G911
P911
F3ADD
GI3
PI3
PGO3
GI2
PI2
GI1
PI1
PGI1
PG3
A12
A13
A14
B12
B13
B14
CI
A0
A1
A2
B0
B1
B2
Z0
Z1
Z2
G012
P012
Z12
Z13
Z14
G1214
P1214
F3ADD
GI4
PI4
PGO4
GI3
PI3
GI2
PI2
GI1
PI1
PGI1
PG4
A15
B15
CI
A0
B0
Z0
CO
Z15
CO
ADDF1

ADDH1, ADDH2, ADDH3, ADDH4, ADDH8, ADDH8A, and ADDH16A

Function:

ADDH1:	1-bit half adder.
ADDH2:	2-bit half adder.
ADDH3:	3-bit half adder.
ADDH4:	4-bit half adder.
ADDH8:	8-bit half adder.
ADDH8A:	8-bit half adder built with propagate-generate submacros.
ADDH16A:	16-bit half adder built with propagate-generate submacros.

Availability:

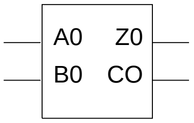
ADDH1, ADDH2, ADDH3, ADDH4, ADDH8, ADDH8A, and ADDH16A can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Additional symbols and schematics appear on the following pages.

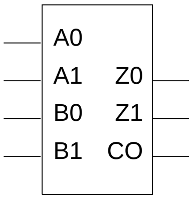
Type:

Soft:	ADDH1, ADDH2, ADDH3, ADDH8A, ADDH16A
Hard:	ADDH4, ADDH8

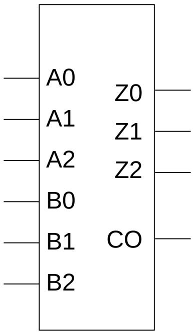
ADDH1



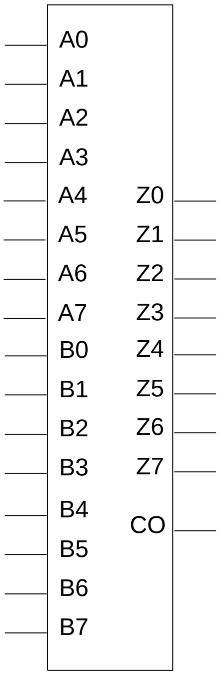
ADDH2



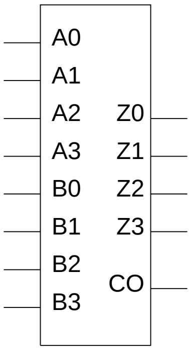
ADDH3



ADDH8



ADDH4

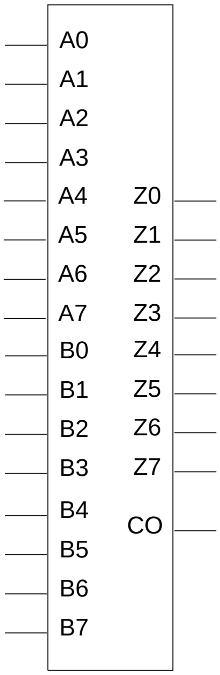


Logic Resources:

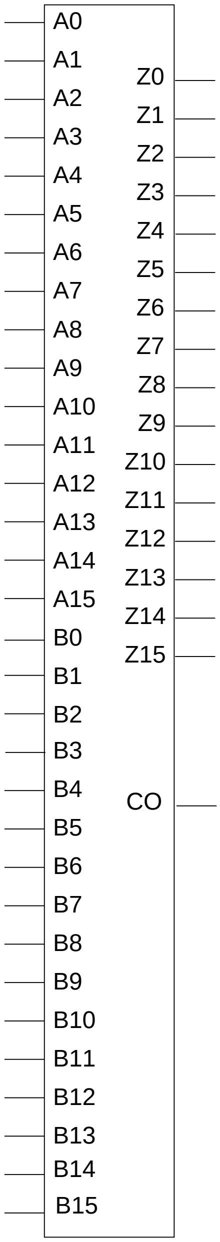
Macro	PT	GLB	Output	Level
ADDH4	****	2	6	2
ADDH8	*****	6	22	3

****	Z0: 2 PT	Z1: 6 PT
	Z2: 4 PT	Z3: 7 PT
	CO: 7 PT	TCO: 3 PT
*****	Z0: 2 PT	Z1: 2 PT
	Z2: 3 PT	Z3: 4 PT
	Z4: 5 PT	Z5: 9 PT
	Z6: 11 PT	Z7: 8 PT
	CO: 7 PT	CC: 3 PT
	G1-G5: 1 PT	P1-P7: 2 PT

ADDH8A



ADDH16A



Truth Table:

The value of CO depends on the sum of A+B and n.

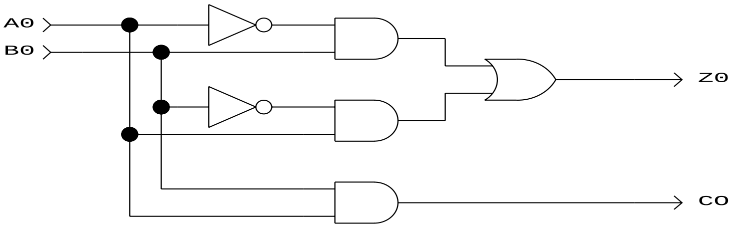
Input		Output	
A$_{n-1}$~A0	**B$_{n-1}$~B0**	**Z$_{n-1}$~Z0**	**CO**
data	data	A+B	*

* If A+B<2^n, CO = 0. If A+B≥2^n, CO = 1.

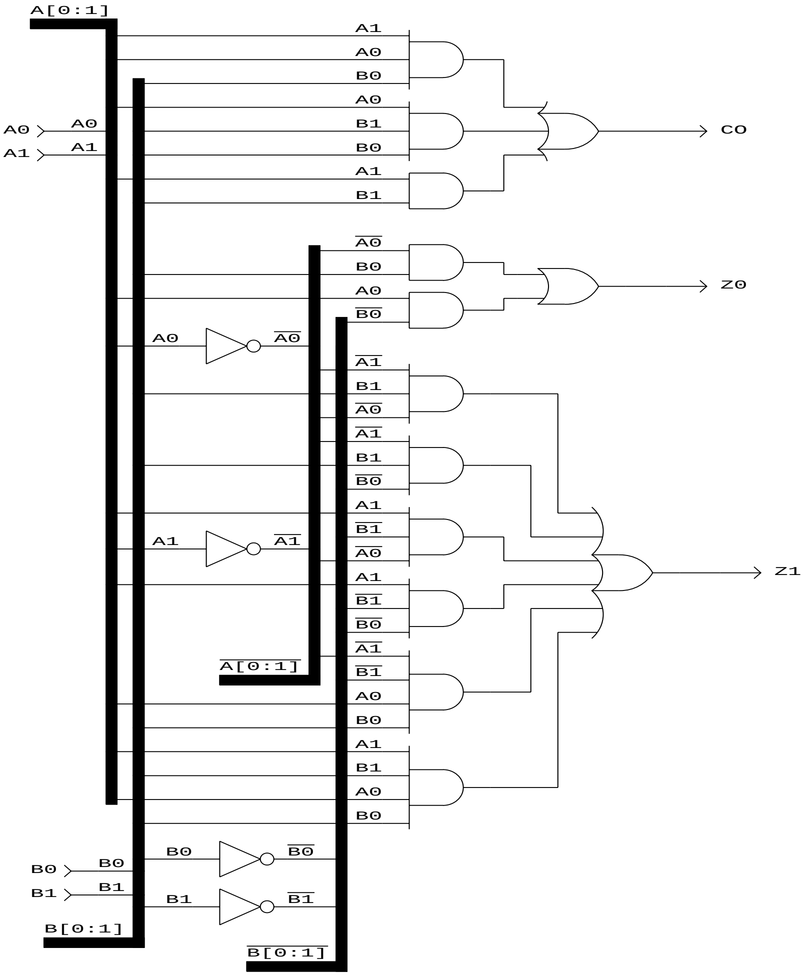
Macro Port Definition:

```
ADDH1 (Z0,CO,A0,B0);
ADDH2 (Z0,Z1,CO,A0,A1,B0,B1);
ADDH3 ([Z0..Z2],CO,A0,A1,A2,B0,B1,B2);
  ADDH3_1 (Z0,A0,B0);
  ADDH3_2 (Z1,Z2,CO,A0,A1,A2,B0,B1,B2);
ADDH4 ([Z0..Z3],CO,[A0..A3],[B0..B3]);
  ADDH4_1 (Z0,Z1,TCO,A0,A1,B0,B1);
  ADDH4_2 (Z2,Z3,CO,A2,A3,B2,B3,TCO);
ADDH8 ([Z0..Z7],CO,[A0..A7],[B0..B7]);
  ADDH8_1 (CO,Z1,Z3,[P1..P7],[G1..G5],A0,B0,CC);
  ADDH8_2 (Z0,Z2,Z4,Z7,[P1..P7],[G1..G5],A0,A6,B0,B6);
  ADDH8_3 (Z6,G5,G4,P4,[P1..P3],P5,P6,[G1..G3],A0,A4,A5,B0,B4,B5);
  ADDH8_4 (Z5,G3,P3,G1,P1,P2,P4,P5,G2,G4,A0,A1,A3,B0,B1,B3);
  ADDH8_5 (G2,P2,P1,A1,A2,B1,B2);
  ADDH8_6 (P7,P6,P5,CC,[A5..A7],[B5..B7]);
ADDH8A ([Z0..Z7],CO,[A0..A7],[B0..B7]);
  ADDH8A_1 (Z0,A0,B0,C2,CCI,P345,G345);
  ADDH8A_2 (Z1,Z2,C2,A0,A1,A2,B0,B1,B2);
  ADDH8A_3 (Z3,Z4,G345,A3,A4,A5,B3,B4,B5,C2);
  ADDH8A_4 (Z5,P345,A3,A4,A5,B3,B4,B5,C2);
  ADDH8A_5 (Z6,Z7,CO,A6,A7,B6,B7,CCI);
ADDH16A ([Z0..Z15],CO,[A0..A15],[B0..B15]);
  ADDH16A_1 (Z0,Z15,CO,A0,A15,B0,B15,C14);
  ADDH16A_2 (Z1,Z2,C2,A0,A1,A2,B0,B1,B2);
  ADDH16A_3 (Z3,Z4,G345,A3,A4,A5,B3,B4,B5,C2);
  ADDH16A_4 (Z5,P345,A3,A4,A5,B3,B4,B5,C2);
  ADDH16A_5 (Z6,Z7,G678,A6,A7,A8,B6,B7,B8,C5);
  ADDH16A_6 (Z8,P678,A6,A7,A8,B6,B7,B8,C5);
  ADDH16A_7 (Z9,Z10,G911,A9,A10,A11,B9,B10,B11,C8);
  ADDH16A_8 (Z11,P911,A9,A10,A11,B9,B10,B11,C8);
  ADDH16A_9 (Z12,Z13,G1214,A12,A13,A14,B12,B13,B14,C11);
  ADDH16A_10 (Z14,P1214,A12,A13,A14,B12,B13,B14,C11);
  ADDH16A_11 (C5,C8,C11,C14,C2,P345,G345,P678,G678,P911,G911,
              P1214,G1214);
```

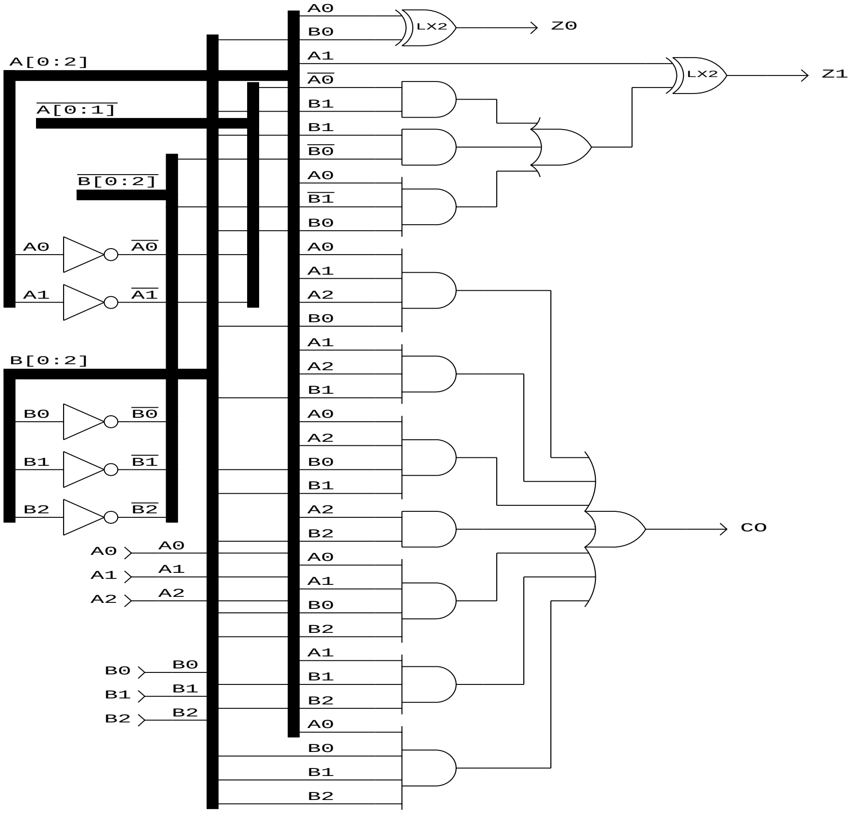
ADDH1



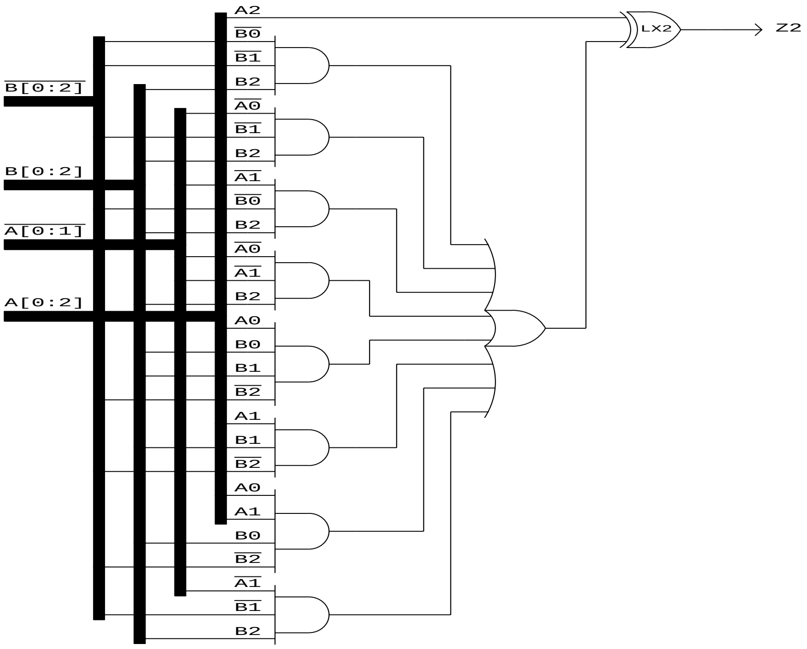
ADDH2


A[0:1]
A1
A0
B0
A0
B1
B0
A1
B1
A0
A1
A0
A1
CO
$\overline{A0}$
B0
A0
$\overline{B0}$
Z0
A0
$\overline{A0}$
$\overline{A1}$
B1
$\overline{A0}$
$\overline{A1}$
B1
$\overline{B0}$
A1
$\overline{B1}$
$\overline{A0}$
A1
$\overline{A1}$
A1
$\overline{B1}$
$\overline{B0}$
Z1
$\overline{A[0:1]}$
$\overline{A1}$
$\overline{B1}$
A0
B0
A1
B1
A0
B0
B0
B0
$\overline{B0}$
B1
B1
B1
$\overline{B1}$
B[0:1]
$\overline{B[0:1]}$

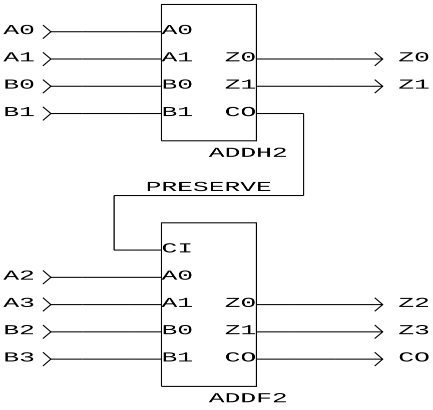
ADDH3.1


A0
B0
LX2
Z0
A1
LX2
Z1
A[0:2]
$\overline{A0}$
B1
$\overline{A[0:1]}$
B1
$\overline{B0}$
$\overline{B[0:2]}$
A0
$\overline{B1}$
B0
A0
$\overline{A0}$
A0
A1
A1
$\overline{A1}$
A2
B0
A1
B[0:2]
A2
B1
B0
$\overline{B0}$
A0
A2
B0
B1
$\overline{B1}$
B1
B2
$\overline{B2}$
A2
B2
C0
A0
A0
A0
A1
A1
A1
A2
A2
B0
B2
A1
B0
B0
B1
B1
B1
B2
B2
B2
A0
B0
B1
B2

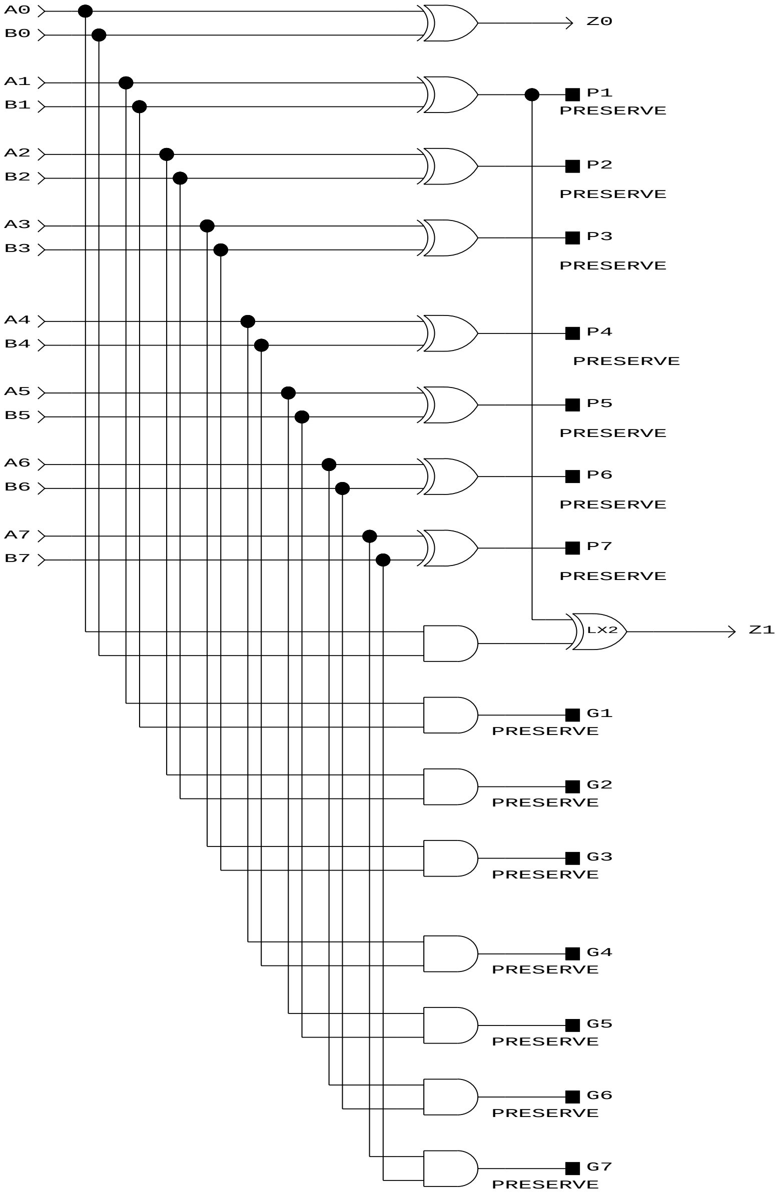
ADDH3.2


$\overline{B[0:2]}$
B[0:2]
$\overline{A[0:1]}$
A[0:2]
A2
$\overline{B0}$
$\overline{B1}$
B2
$\overline{A0}$
$\overline{B1}$
B2
$\overline{A1}$
$\overline{B0}$
B2
$\overline{A0}$
$\overline{A1}$
B2
A0
B0
B1
$\overline{B2}$
A1
B1
$\overline{B2}$
A0
A1
B0
$\overline{B2}$
$\overline{A1}$
$\overline{B1}$
B2
LX2
Z2

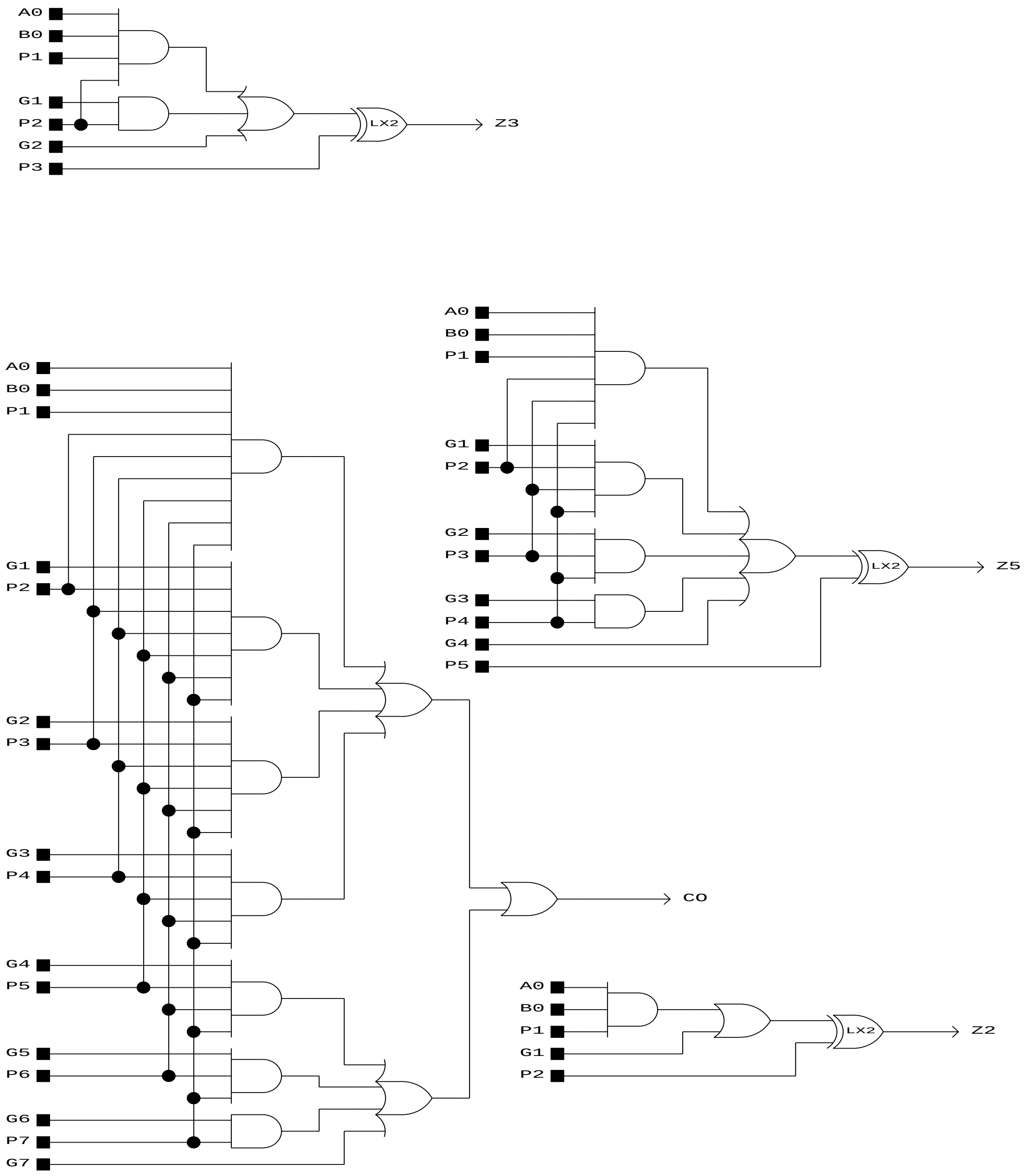
ADDH4


A0
A1
B0
B1
A0
A1
B0
B1
Z0
Z1
CO
Z0
Z1
ADDH2
PRESERVE
CI
A2
A3
B2
B3
A0
A1
B0
B1
Z0
Z1
CO
Z2
Z3
CO
ADDF2

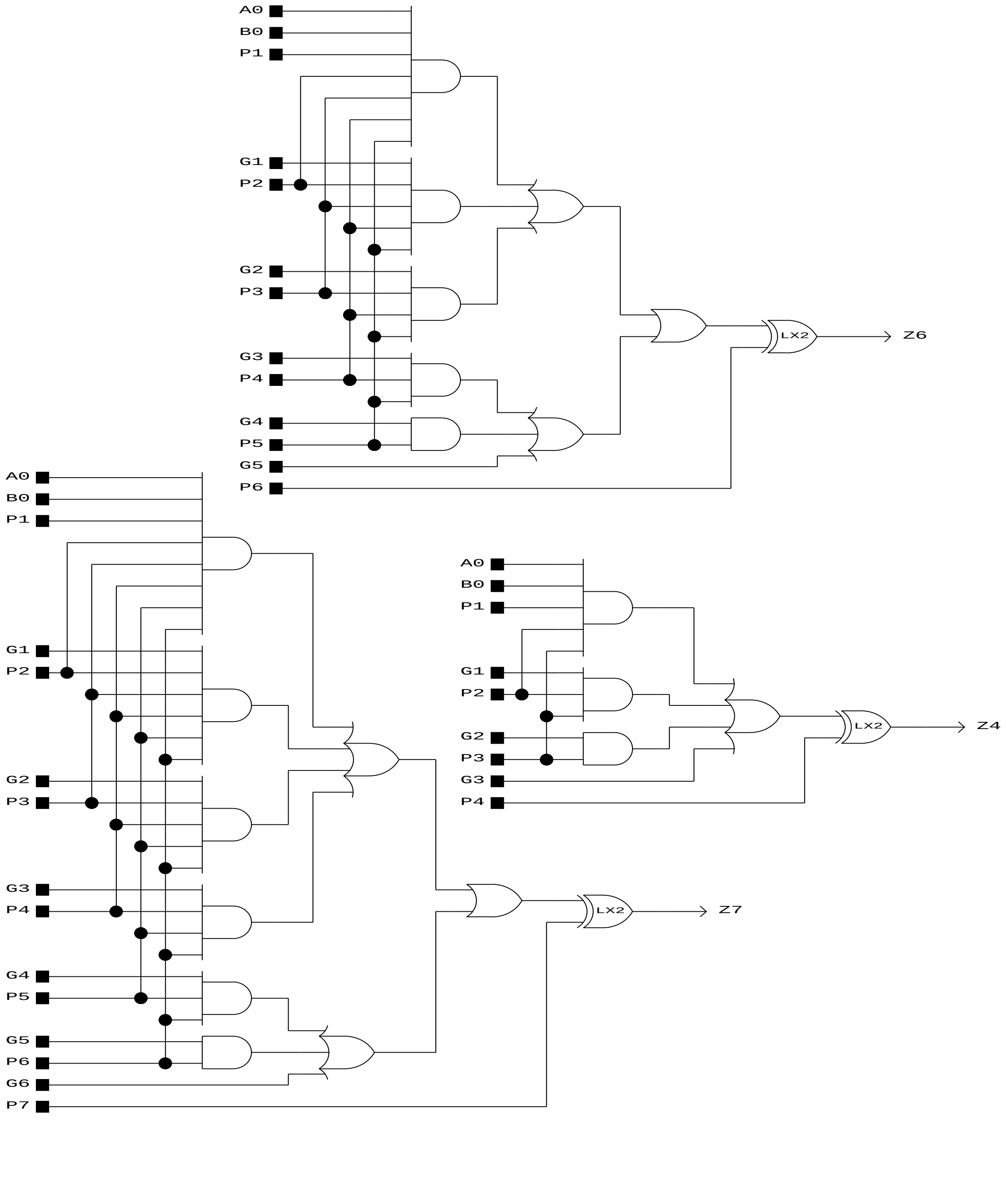
ADDH8.1


A0
B0
A1
B1
A2
B2
A3
B3
A4
B4
A5
B5
A6
B6
A7
B7
Z0
P1
PRESERVE
P2
PRESERVE
P3
PRESERVE
P4
PRESERVE
P5
PRESERVE
P6
PRESERVE
P7
PRESERVE
LX2
Z1
G1
PRESERVE
G2
PRESERVE
G3
PRESERVE
G4
PRESERVE
G5
PRESERVE
G6
PRESERVE
G7
PRESERVE

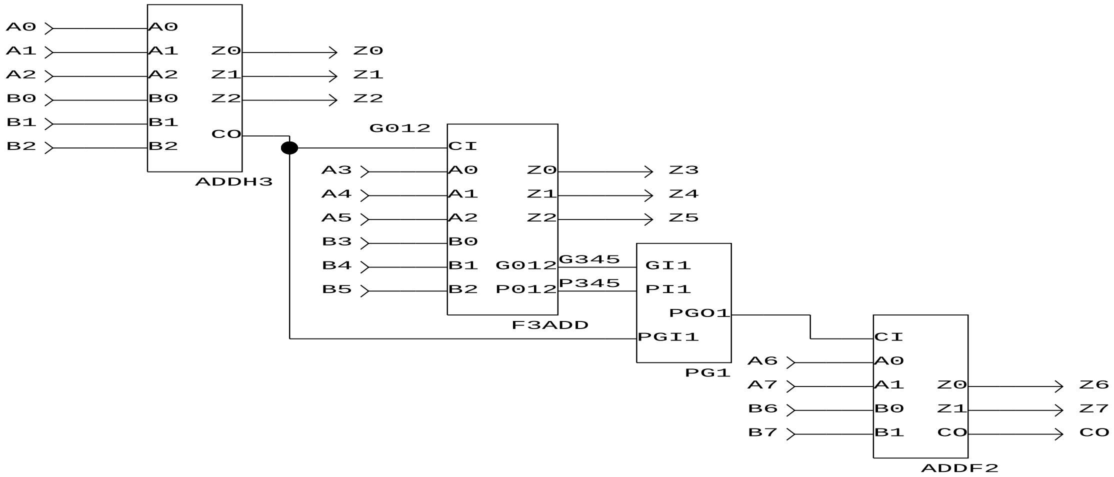
ADDH8.2


A0
B0
P1
G1
P2
G2
P3
LX2
Z3
A0
B0
P1
G1
P2
G2
P3
G3
P4
G4
P5
LX2
Z5
A0
B0
P1
G1
P2
G2
P3
G3
P4
G4
P5
G5
P6
G6
P7
G7
CO
A0
B0
P1
G1
P2
LX2
Z2

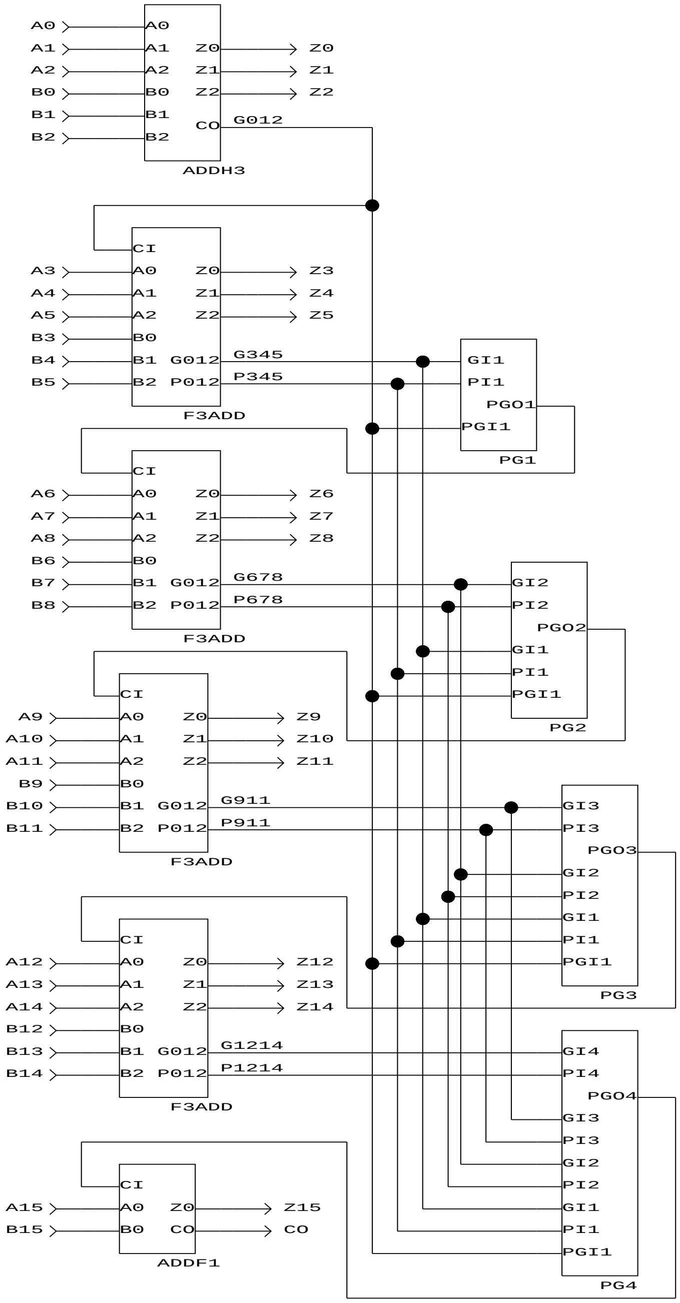
ADDH8.3


A0
B0
P1
G1
P2
G2
P3
G3
P4
G4
P5
G5
P6
LX2
Z6
A0
B0
P1
G1
P2
G2
P3
G3
P4
LX2
Z4
A0
B0
P1
G1
P2
G2
P3
G3
P4
G4
P5
G5
P6
G6
P7
LX2
Z7

ADDH8A

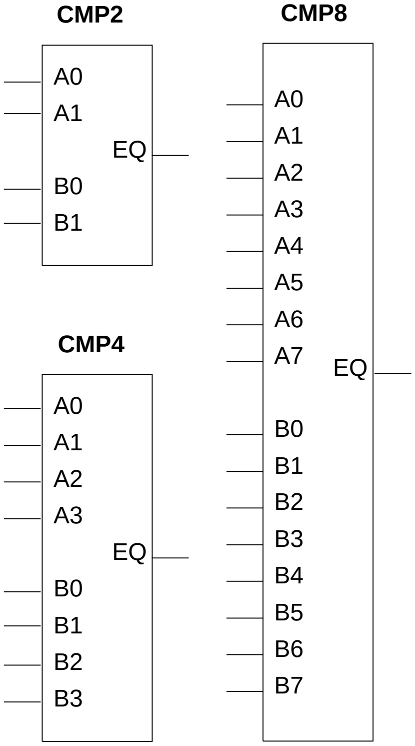

A0
A1
A2
B0
B1
B2
A0
A1
A2
B0
B1
B2
Z0
Z1
Z2
CO
Z0
Z1
Z2
ADDH3
G012
CI
A3
A4
A5
B3
B4
B5
A0
A1
A2
B0
B1
B2
Z0
Z1
Z2
G012
P012
Z3
Z4
Z5
F3ADD
G345
P345
GI1
PI1
PGO1
PGI1
PG1
CI
A6
A7
B6
B7
A0
A1
B0
B1
Z0
Z1
CO
Z6
Z7
CO
ADDF2

ADDH16A


A0
A1
A2
B0
B1
B2
A0
A1
A2
B0
B1
B2
Z0
Z1
Z2
CO
Z0
Z1
Z2
G012
ADDH3
CI
A3
A4
A5
B3
B4
B5
A0
A1
A2
B0
B1
B2
Z0
Z1
Z2
G012
P012
Z3
Z4
Z5
G345
P345
F3ADD
GI1
PI1
PGO1
PGI1
PG1
CI
A6
A7
A8
B6
B7
B8
A0
A1
A2
B0
B1
B2
Z0
Z1
Z2
G012
P012
Z6
Z7
Z8
G678
P678
F3ADD
GI2
PI2
PGO2
GI1
PI1
PGI1
PG2
CI
A9
A10
A11
B9
B10
B11
A0
A1
A2
B0
B1
B2
Z0
Z1
Z2
G012
P012
Z9
Z10
Z11
G911
P911
F3ADD
GI3
PI3
PGO3
GI2
PI2
GI1
PI1
PGI1
PG3
CI
A12
A13
A14
B12
B13
B14
A0
A1
A2
B0
B1
B2
Z0
Z1
Z2
G012
P012
Z12
Z13
Z14
G1214
P1214
F3ADD
GI4
PI4
PGO4
GI3
PI3
GI2
PI2
GI1
PI1
PGI1
PG4
CI
A15
B15
A0
B0
Z0
CO
Z15
CO
ADDF1

Comparators

CMP2, CMP4, and CMP8



Function:

CMP2:	2-bit equality comparator.
CMP4:	4-bit equality comparator.
CMP8:	8-bit equality comparator.

Availability:

CMP2, CMP4, and CMP8 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Soft

Macro Port Definition:

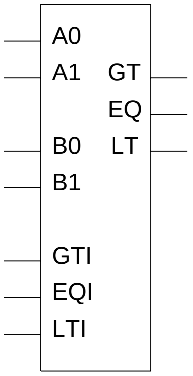
```
CMP2 (EQ,A0,A1,B0,B1);
CMP4 (EQ,[A0..A3],[B0..B3]);
CMP8 (EQ,[A0..A7],[B0..B7]);
```

Truth Table:

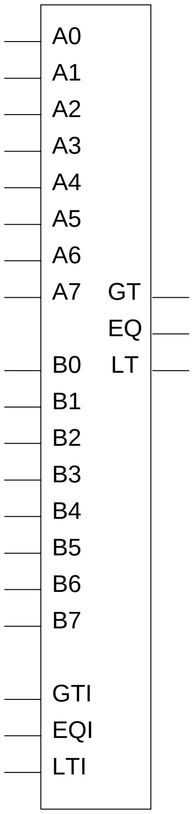
Input	Output
A0~A_{n-1}, B0~B_{n-1}	**EQ**
A0=B0,... A_{n-1}=B_{n-1}	1
All other values	0

MAG2, MAG4, and MAG8

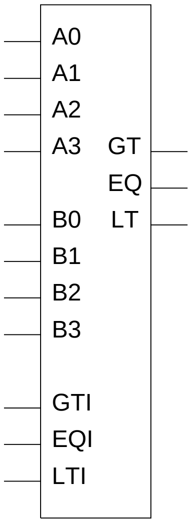
MAG2



MAG8



MAG4



Function:

MAG2: 2-bit magnitude comparator.
MAG4: 4-bit magnitude comparator.
MAG8: 8-bit magnitude comparator.

Availability:

MAG2, MAG4, and MAG8 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type:

Soft: MAG2
Hard: MAG4 and MAG8

Logic Resources:

Macro	PT	GLB	Output	Level
MAG4	16/out	3	3	1
MAG8	16/out	6	6	2

Macro Port Definition:

```
MAG2 (GT,EQ,LT,A0,A1,B0,B1,GTI,EQI,LTI);
MAG4 (GT,EQ,LT,[A0..A3],[B0..B3],GTI,EQI,LTI);
  MAG4_1 (EQ,[A0..A3],[B0..B3],GTI,EQI,LTI);
  MAG4_2 (GT,[A0..A3],[B0..B3],GTI,EQI,LTI);
  MAG4_3 (LT,[A0..A3],[B0..B3],GTI,EQI,LTI);
MAG8 (GT,EQ,LT,[A0..A7],[B0..B7],GTI,EQI,LTI);
  MAG8_1 (TEQ,[A4..A7],[B4..B7],GTI,EQI,LTI);
  MAG8_2 (TGT,[A4..A7],[B4..B7],GTI,EQI,LTI);
  MAG8_3 (TLT,[A4..A7],[B4..B7],GTI,EQI,LTI);
  MAG8_4 (EQ,[A0..A3],[B0..B3],TGT,TEQ,TLT);
  MAG8_5 (GT,[A0..A3],[B0..B3],TGT,TEQ,TLT);
  MAG8_6 (LT,[A0..A3],[B0..B3],TGT,TEQ,TLT);
```

Truth Table:

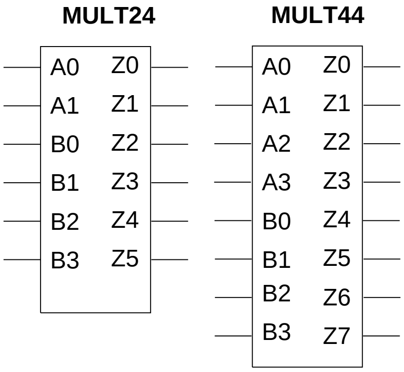
The truth table is the same for all MAGs.

Input					Output		
LTI	**ETI**	**GTI**	**A**	**B**	**LT**	**EQ**	**GT**
0	0	0	x	x	0	0	0
0	0	1	x	x	0	0	1
0	1	0	A<B		1	0	0
0	1	0	A=B		0	1	0
0	1	0	A>B		0	0	1
0	1	1	x	x	0	0	0
1	0	0	x	x	1	0	0
1	0	1	x	x	0	0	0
1	1	0	x	x	0	0	0
1	1	1	x	x	0	0	0

x = don’t care.

Multipliers

MULT24 and MULT44



Function:

MULT24:	2-bit by 4-bit multiplier.
MULT44:	4-bit by 4-bit multiplier.

Availability:

MULT24 and MULT44 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Schematics appear on the following pages.

Type: Soft

Macro Port Definition:

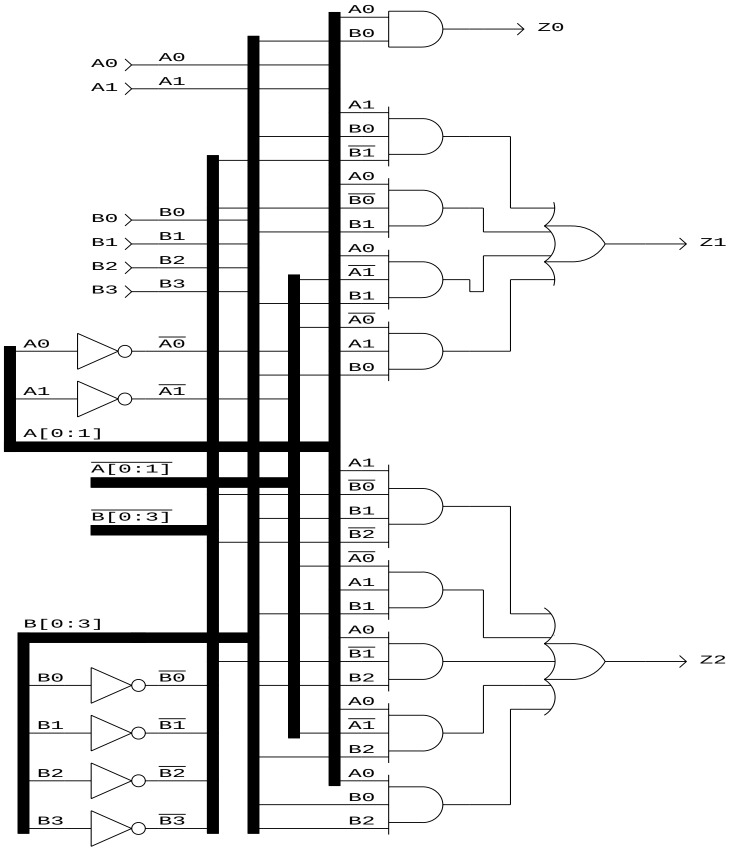
```
MULT24 (Z0,Z1,Z2,Z3,Z4,Z5,A0,A1,B0,B1,B2,B3);
  MULT24_1 (Z0,Z1,Z2,Z3,A0,A1,B0,B1,B2,B3);
  MULT24_2 (Z4,Z5,A0,A1,B0,B1,B2,B3);
MULT44 ([Z0..Z7],[A0..A3],[B0..B3]);
  MULT44_1 (L0,L1,L2,L3,A0,A1,B0,B1,B2,B3);
  MULT44_2 (H0,H1,H2,H3,A2,A3,B0,B1,B2,B3);
  MULT44_3 (L4,L5,H4,H5,A0,A1,A2,A3,B0,B1,B2,B3);
  MULT44_4 (Z0,Z1,Z2,G012,L0,L1,L2,H0);
  MULT44_5 (Z3,Z4,G345,L3,L4,L5,H1,H2,H3,G012);
  MULT44_6 (Z5,P345,L3,L4,L5,H1,H2,H3,G012);
  MULT44_7 (Z6,Z7,G345,P345,G012,H4,H5,C5);
```

Truth Table:

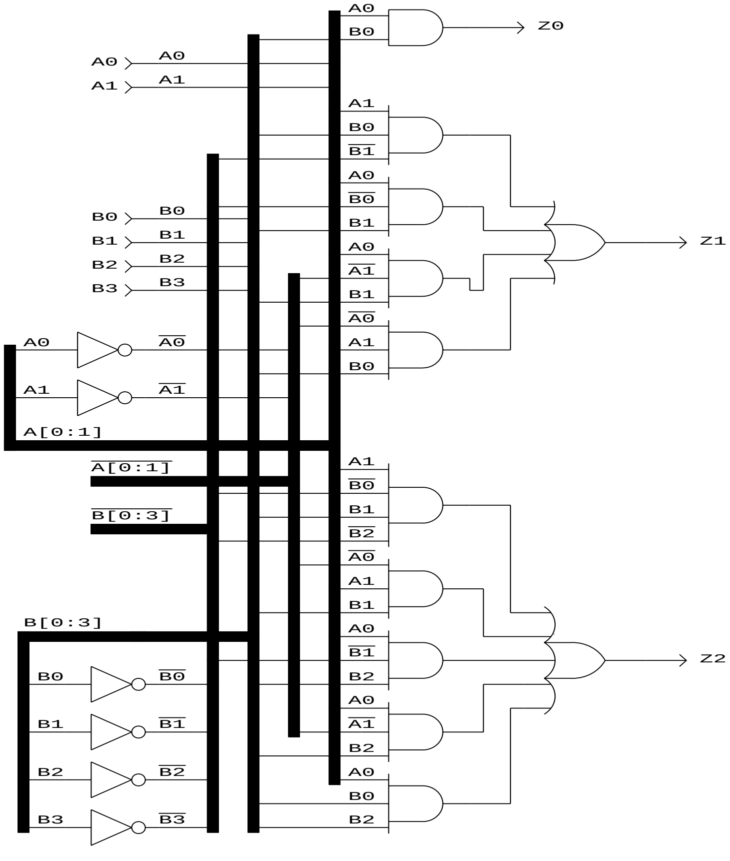
Input		Output
A_{n-1}~A0	**B_{n-1}~B0**	**Z_{n-1}~Z0**
data	data	A*B

* = multiply.

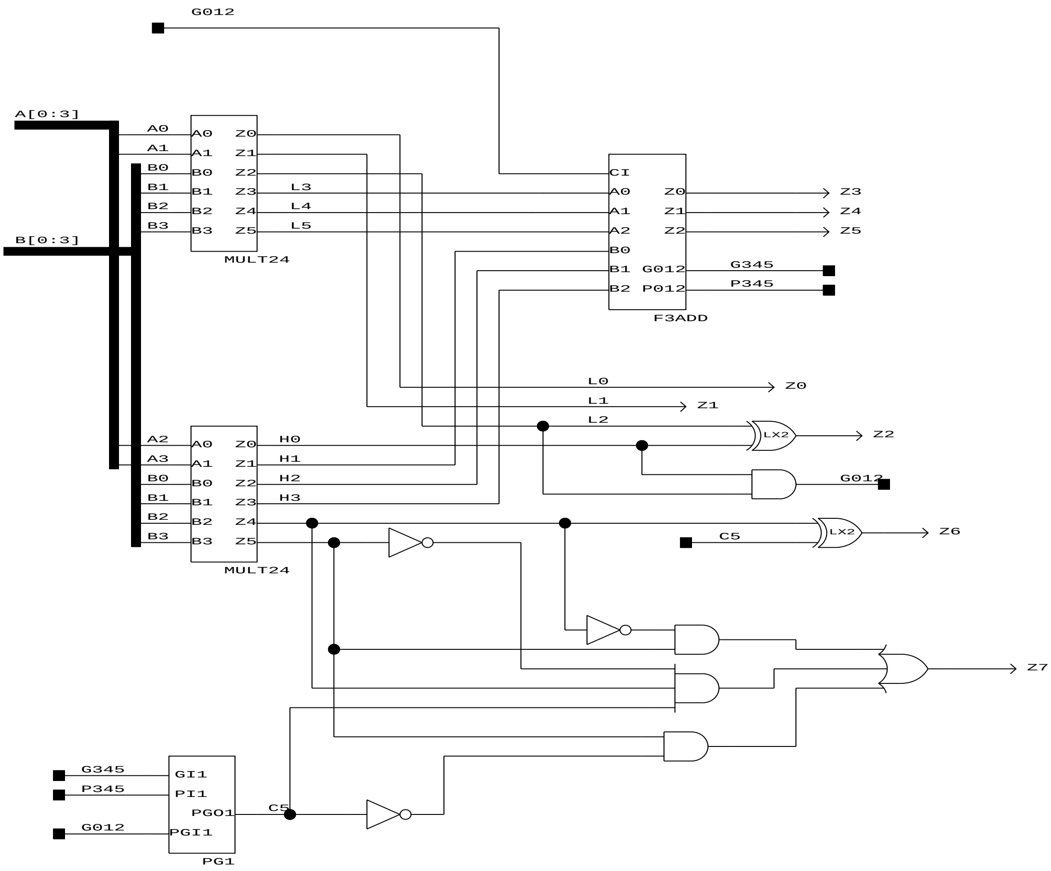
MULT24.1


A0
B0
Z0
A0
A1
A0
A1
A1
B0
$\overline{B1}$
A0
$\overline{B0}$
B1
B0
B1
B2
B3
B0
B1
B2
B3
Z1
A0
$\overline{A1}$
B1
$\overline{A0}$
A1
B0
A0
$\overline{A0}$
A1
$\overline{A1}$
A[0:1]
$\overline{A[0:1]}$
$\overline{B[0:3]}$
A1
$\overline{B0}$
B1
$\overline{B2}$
$\overline{A0}$
A1
B1
A0
$\overline{B1}$
B2
Z2
A0
$\overline{A1}$
B2
A0
B0
B2
B[0:3]
B0
$\overline{B0}$
B1
$\overline{B1}$
B2
$\overline{B2}$
B3
$\overline{B3}$

MULT24.2

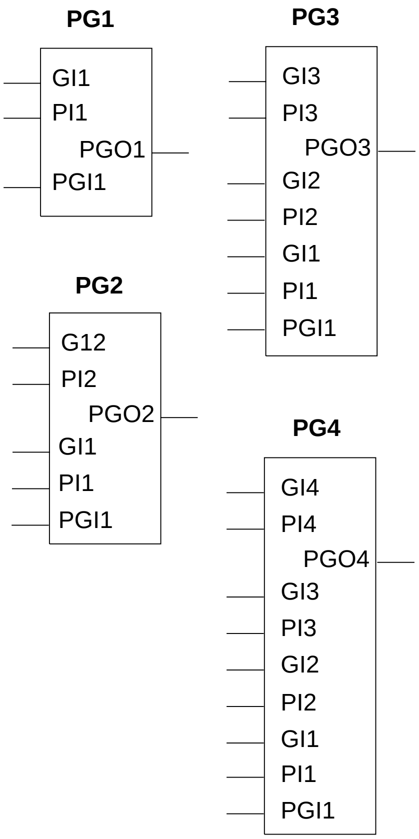

A0
B0
Z0
A0
A1
A0
A1
A1
B0
$\overline{B1}$
A0
$\overline{B0}$
B1
B0
B1
B2
B3
B0
B1
B2
B3
A0
$\overline{A1}$
B1
Z1
$\overline{A0}$
A1
B0
A0
$\overline{A0}$
A1
$\overline{A1}$
A[0:1]
A1
$\overline{A[0:1]}$
$\overline{B0}$
B1
$\overline{B[0:3]}$
$\overline{B2}$
$\overline{A0}$
A1
B1
B[0:3]
A0
$\overline{B1}$
Z2
B0
$\overline{B0}$
B2
A0
B1
$\overline{B1}$
$\overline{A1}$
B2
B2
$\overline{B2}$
A0
B0
B3
$\overline{B3}$
B2

MULT44


G012
A[0:3]
B[0:3]
A0
A1
B0
B1
B2
B3
A0 Z0
A1 Z1
B0 Z2
B1 Z3
B2 Z4
B3 Z5
L3
L4
L5
MULT24
CI
A0 Z0
A1 Z1
A2 Z2
B0
B1 G012
B2 P012
F3ADD
Z3
Z4
Z5
G345
P345
L0
L1
L2
Z0
Z1
LX2
Z2
A2
A3
B0
B1
B2
B3
A0 Z0
A1 Z1
B0 Z2
B1 Z3
B2 Z4
B3 Z5
H0
H1
H2
H3
MULT24
G012
C5
LX2
Z6
Z7
G345
P345
G012
GI1
PI1
PGO1
PGI1
PG1
C5

Propagate-Generate

PG1, PG2, PG3, and PG4



Function:

PG1:	Propagate-Generate Bit 1.
PG2:	Propagate-Generate Bit 2.
PG3:	Propagate-Generate Bit 3.
PG4:	Propagate-Generate Bit 4.

Availability:

PG1, PG2, PG3, and PG4 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Schematics appear on the following pages.

Type: Soft

Macro Port Definition:

```
PG1 (PGO1,PGI1,PI1,GI1);
PG2 (PGO2,PGI1,PI1,GI1,PI2,GI2);
PG3 (PGO3,PGI1,PI1,GI1,PI2,GI2,PI3,GI3);
PG4 (PGO4,PGI1,PI1,GI1,PI2,GI2,PI3,GI3,PI4,GI4);
```

Truth Table for PG1:

Input			Output
PGI1	**PI1**	**GI1**	**PGO1**
x	x	1	1
1	1	x	1

x = don’t care.

Truth Table for PG2:

Input					Output
PGI1	**PI1**	**PI2**	**GI1**	**G12**	**PGO2**
x	x	x	x	1	1
x	x	1	1	x	1
1	1	1	x	x	1

x = don’t care.

Truth Table for PG3:

Input							Output
PGI1	**PI1**	**PI2**	**PI3**	**GI1**	**GI2**	**GI3**	**PGO3**
x	x	x	x	x	x	1	1
x	x	x	1	x	1	x	1
x	x	1	1	1	x	x	1
1	1	1	1	x	x	x	1

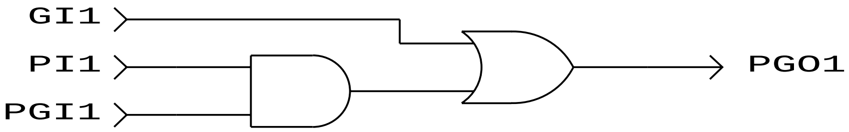
x = don’t care.

Truth Table for PG4:

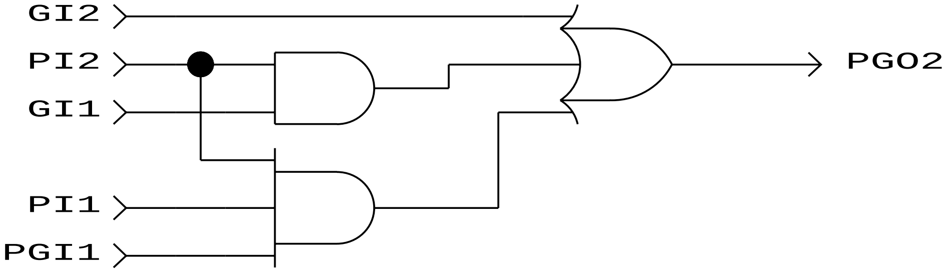
Input									Output
PGI1	**PI1**	**PI2**	**PI3**	**PI4**	**GI1**	**GI2**	**GI3**	**GI4**	**PGO4**
x	x	x	x	x	x	x	x	1	1
x	x	x	x	1	x	x	1	x	1
x	x	x	1	1	x	1	x	x	1
x	x	1	1	1	1	x	x	x	1
1	1	1	1	1	x	x	x	x	1

x = don’t care.

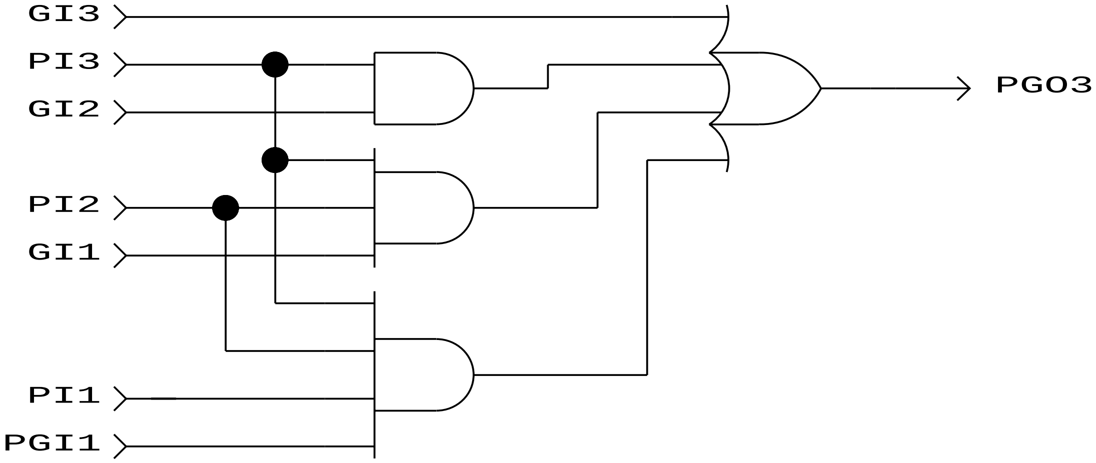
PG1



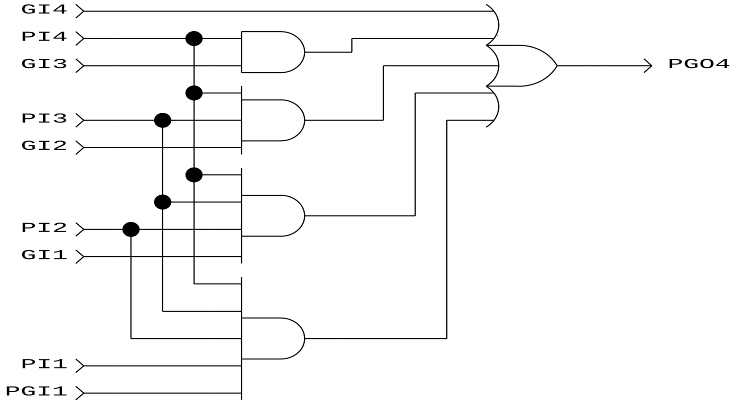
PG2



PG3



PG4



Subtractors

SUBF1, SUBF2, F3SUB, SUBF4, SUBF8, SUBF8A, and SUBF16A

Function:

SUBF1:	1-bit full subtractor.
SUBF2:	2-bit full subtractor.
F3SUB:	3-bit full subtractor with propagate-generate.
SUBF4:	4-bit full subtractor.
SUBF8:	8-bit full subtractor.
SUBF8A:	8-bit full subtractor built with propagate-generate submacros.
SUBF16A:	16-bit full subtractor built with propagate-generate submacros.

Availability:

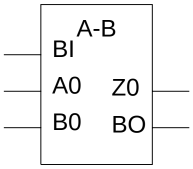
SUBF1, SUBF2, F3SUB, SUBF4, SUBF8, SUBF8A, and SUBF16A can be used with 1000, 2000, 3000, 5000, and 8000 devices.

An additional symbol and schematics appear on the following pages.

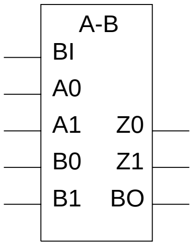
Type:

Soft:	SUBF1, SUBF2, F3SUB, SUBF8A, SUBF16A
Hard:	SUBF4, SUBF8

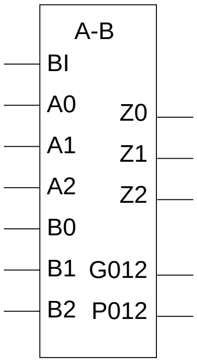
SUBF1



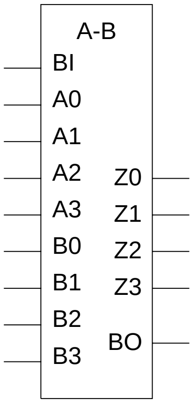
SUBF2



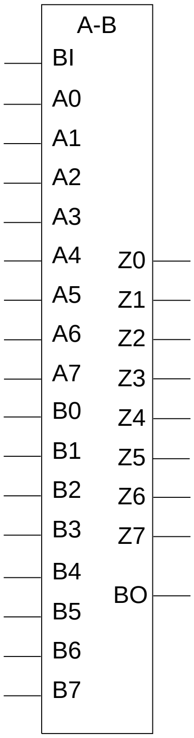
F3SUB



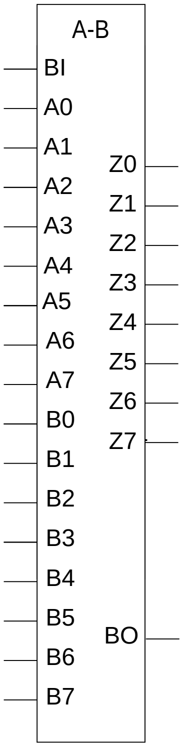
SUBF4



SUBF8



SUBF8A



Logic Resources:

Macro	PT	GLB	Output	Level
SUBF4	****	2	6	2
SUBF8	*****	8	27	3

****	Z0: 4 PT	Z1: 7 PT	Z2: 4 PT
	Z3: 7 PT	BO: 7 PT	TBO: 7 PT
*****	Z0: 2 PT	Z1: 3 PT	Z2: 4 PT
	Z3: 5 PT	Z4: 6 PT	Z5: 7 PT
	Z6: 6 PT	Z7: 7 PT	BO: 6 PT
	BA: 3 PT	BB: 7 PT	BC: 3 PT
	G0-G6: 1 PT	P0-P7: 2 PT	

Truth Table:

The truth table below applies to SUBF1, SUBF2, SUBF4, SUBF8, SUBF8A, and SUBF16A. The value of BO depends on the difference of A–B.

Input			Output	
A_{n-1}~A0	B_{n-1}~B0	BI	Z_{n-1}~Z0	BO
data	data	0	A–B	*
data	data	1	A–B–1	**

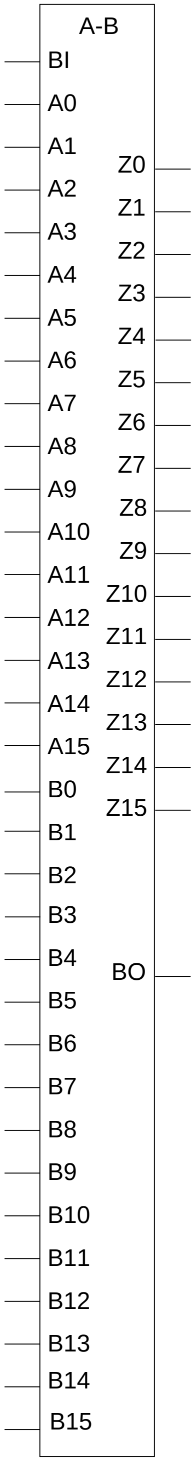
* If B≤A, BO = 0. If B>A, BO = 1.
** If B<A, BO = 0. If B≥A, BO = 1.

The truth table for F3SUB is shown below.

Input			Output		
A_2~A0	B_2~B0	BI	Z_2~Z0	G012	P012
data	data	0	A-B	*	***
data	data	1	A-B-1	**	***

* If B≤A, G012 = 0. If B>A, G012 = 1.
** If B≤A, G012 = 0. If B>A, G012 = 1.
*** P012 = ($\overline{A0}$ + B0) ($\overline{A1}$ + B1) ($\overline{A2}$ + B2) where $\overline{A0}$ = inverted A0.

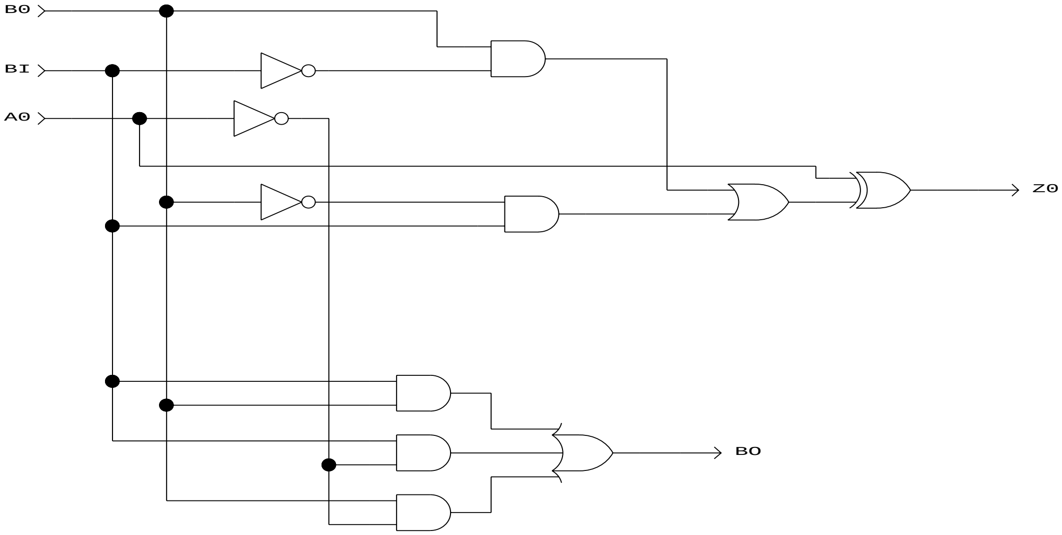
SUBF16A



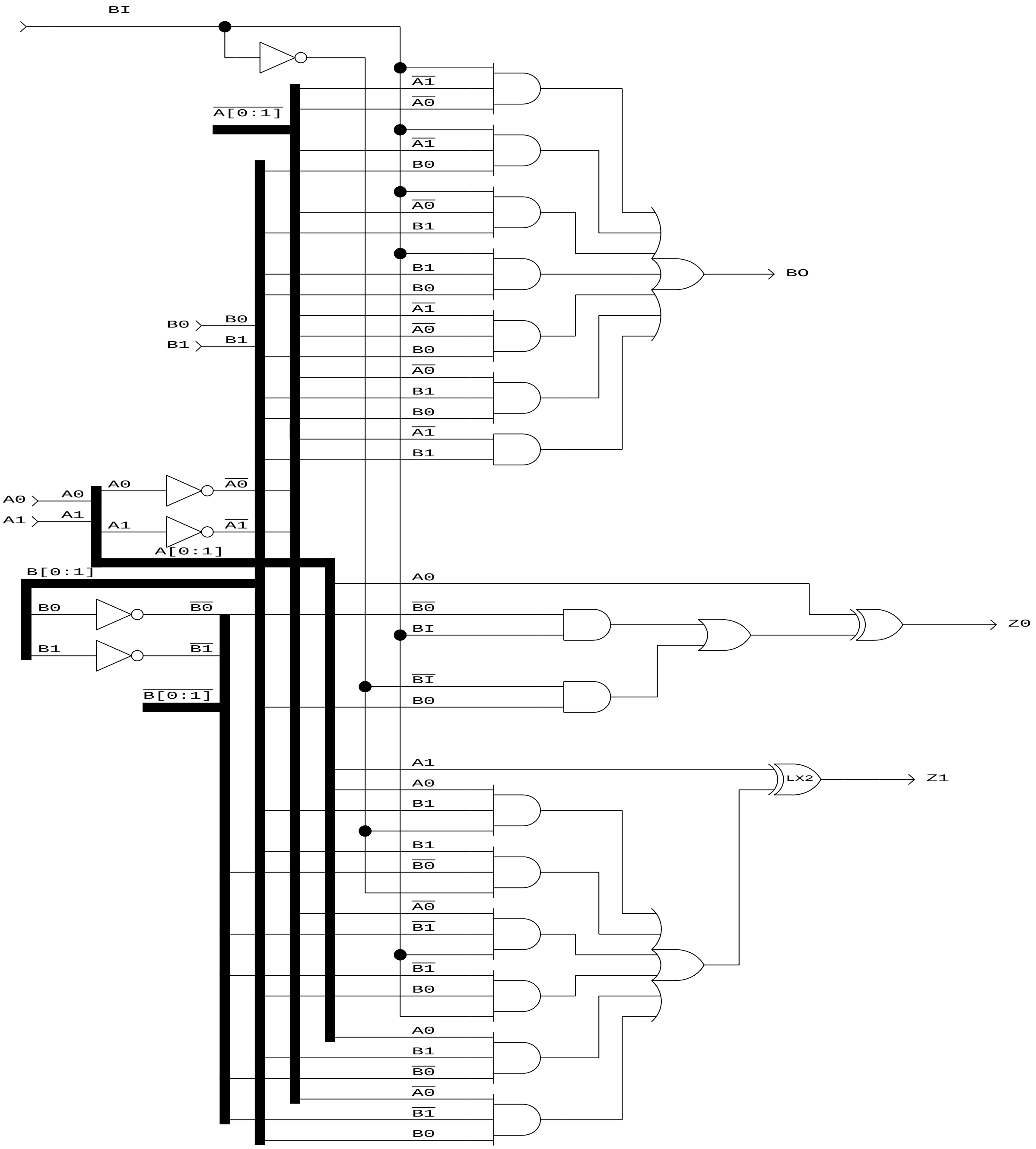
Macro Port Definition:

```
SUBF1 (Z0,BO,A0,B0,BI);
SUBF2 (Z0,Z1,BO,A0,A1,B0,B1,BI);
F3SUB ([Z0..Z2],G012,P012,[A0..A2],[B0..B2],BI);
  F3SUB_1 (Z0,Z1,G012,[A02..A2],[B0..B2],BI);
  F3SUB_2 (Z2,P012,[A0..A2][B0..B2],BI);
SUBF4 ([Z0..Z3],BO,[A0..A3],[B0..B3],BI);
  SUBF4_1 (Z0,Z1,TBO,A0,A1,B0,B1,BI);
  SUBF4_2 (Z2,Z3,BO,A2,A3,B2,B3,TBO);
SUBF8 ([Z0..Z7],BO,[A0..A7],[B0..B7],BI);
  SUBF8_1 (BO,[P0..P7],[G0..G3],BB,BI);
  SUBF8_2 (Z7,[P0..P7][G0..G3],A3,B3,BI,BA);
  SUBF8_3 (Z6,[P0..P6],G0,G1,A0,A2,B0,B2,BI,BC);
  SUBF8_4 (Z5,[P0..P6],G0,G1,G3,A2,A4,A6,B2,B4,B6,BI);
  SUBF8_5 (Z2,Z4,[P0..P4],[G0..G2],G4,A1,A3,A4,B1,B3,B4,BI);
  SUBF8_6 (Z3,[P0..P3],G1,G2,G5,G6,A0,A1,A5,A6,B0,B1,B5,B6,BI);
  SUBF8_7 (Z0,P7,G2,BB,P0,P5,P6,G4,G5,G6,A2,A7,B2,B7,BI);
  SUBF8_8 (Z1,BA,BC,P5,P0,P1,P4,P6,[G3..G6],A0,A5,B0,B5,BI);
SUBF8A ([Z0..Z7],BO,[A0..A7],[B0..B7],BI);
  SUBF8A_1 (Z0,Z1,G012,[A0..A2],[B0..B2],BI);
  SUBF8A_2 (Z2,P012,[A0..A2],[B0..B2],BI);
  SUBF8A_3 (BB2,BBI,BI,P012,P345,G012,G345);
  SUBF8A_4 (Z3,Z4,G345,A3,A4,A5,B3,B4,B5,BB2);
  SUBF8A_5 (Z5,P345,[A3..A5],[B3..B5],BB2);
  SUBF8A_6 (BO,Z6,Z7,A6,A7,B6,B7,BBI);
SUBF16A ([Z0..Z15],BO,[A0..A15],[B0..B15],BI);
  SUBF16A_1 (Z0,Z1,G012,A0,A1,A2,B0,B1,B2,BI);
  SUBF16A_2 (Z2,P012,A0,A1,A2,B0,B1,B2,BI);
  SUBF16A_3 (Z3,Z4,G345,A3,A4,A5,B3,B4,B5,BB2);
  SUBF16A_4 (Z5,P345,A3,A4,A5,B3,B4,B5,BB2);
  SUBF16A_5 (Z6,Z7,G678,A6,A7,A8,B6,B7,B8,BB5);
  SUBF16A_6 (Z8,P678,A6,A7,A8,B6,B7,B8,BB5);
  SUBF16A_7 (Z9,Z10,G911,A9,A10,A11,B9,B10,B11,BB8);
  SUBF16A_8 (Z11,P911,A9,A10,A11,B9,B10,B11,BB8);
  SUBF16A_9 (Z12,Z13,G1214,A12,A13,A14,B12,B13,B14,BB11);
  SUBF16A_10 (Z14,P1214,A12,A13,A14,B12,B13,B14,BB11);
  SUBF16A_11 (Z15,BO,BB2,BI,P012,G012,A15,B15,BB14);
  SUBF16A_12 (BB5,BB8,BB11,BB14,BB2,P345,G345,P678,G678,
              P911,G911,P1214,G1214);
```

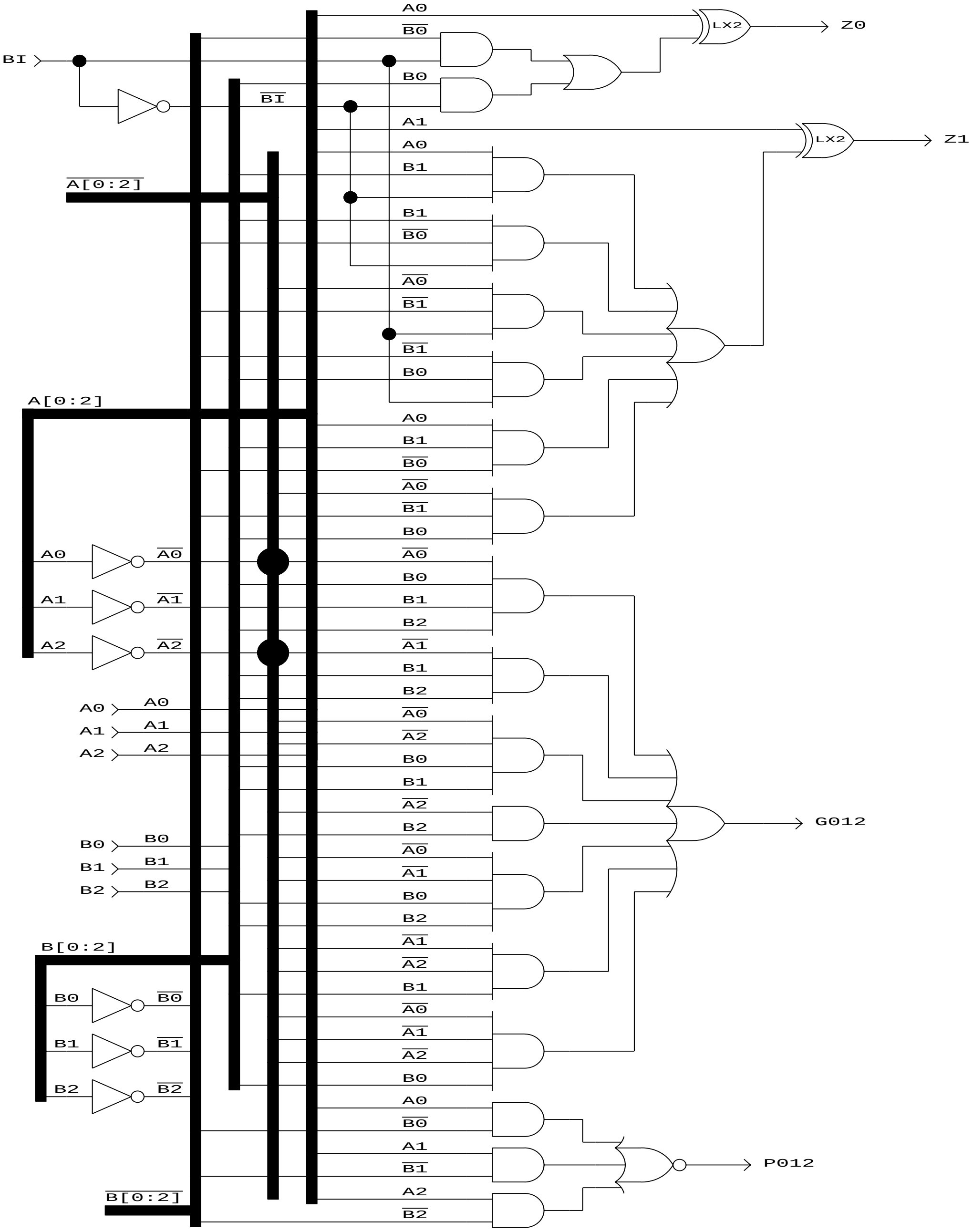
SUBF1



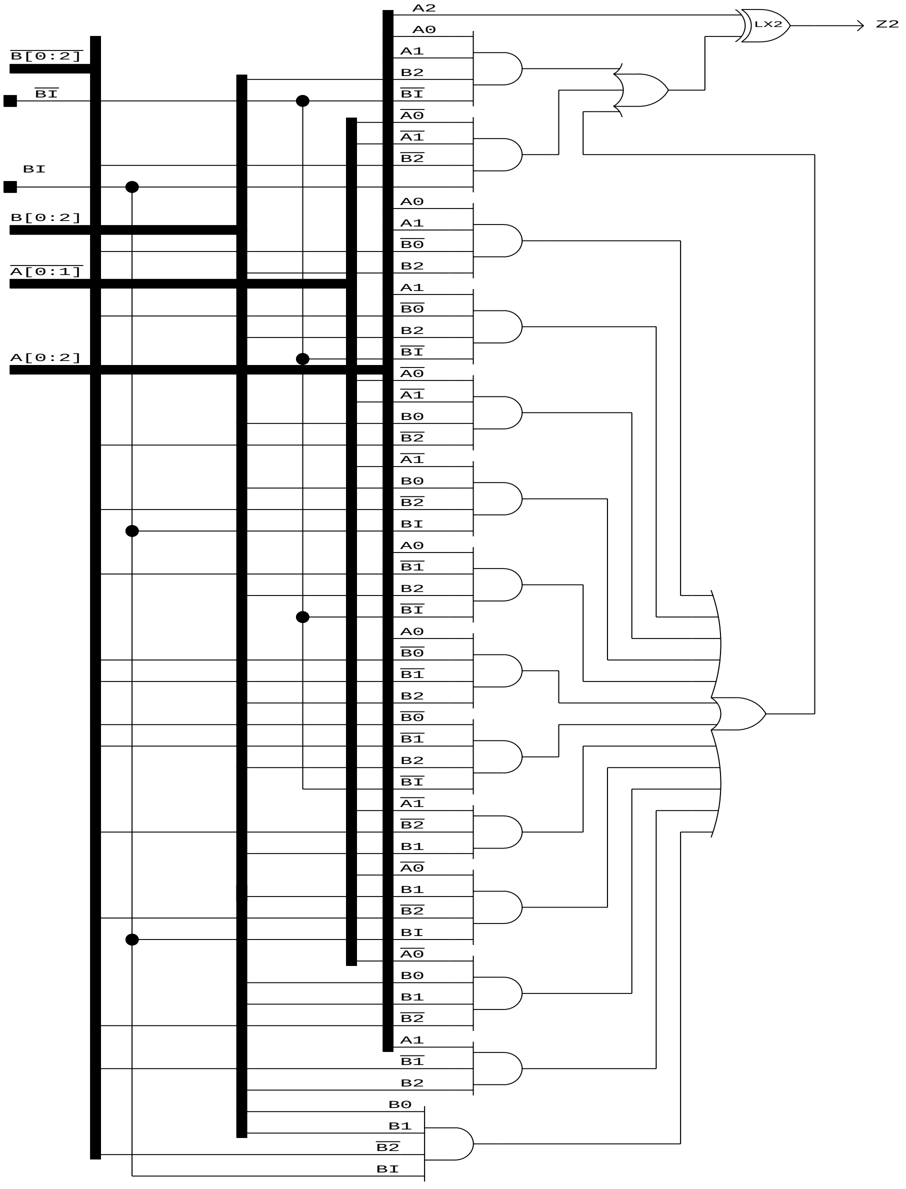
SUBF2


BI
$\overline{A1}$
$\overline{A0}$
$\overline{A[0:1]}$
$\overline{A1}$
B0
$\overline{A0}$
B1
B1
B0
BO
$\overline{A1}$
$\overline{A0}$
B0
$\overline{A0}$
B1
B0
$\overline{A1}$
B1
B0
B1
B0
B1
A0
A1
A0
A1
A0
$\overline{A0}$
A1
$\overline{A1}$
A[0:1]
B[0:1]
A0
B0
$\overline{B0}$
$\overline{B0}$
BI
Z0
B1
$\overline{B1}$
$\overline{BI}$
B0
$\overline{B[0:1]}$
A1
LX2
Z1
A0
B1
B1
$\overline{B0}$
$\overline{A0}$
$\overline{B1}$
$\overline{B1}$
B0
A0
B1
$\overline{B0}$
$\overline{A0}$
$\overline{B1}$
B0

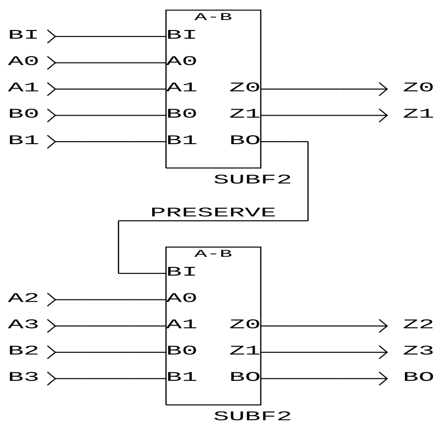
F3SUB.1


A0
LX2
Z0
$\overline{B0}$
BI
B0
$\overline{BI}$
A1
LX2
Z1
A0
B1
$\overline{A[0:2]}$
B1
$\overline{B0}$
$\overline{A0}$
$\overline{B1}$
$\overline{B1}$
B0
A[0:2]
A0
B1
$\overline{B0}$
$\overline{A0}$
$\overline{B1}$
B0
A0
$\overline{A0}$
$\overline{A0}$
B0
A1
$\overline{A1}$
B1
B2
A2
$\overline{A2}$
$\overline{A1}$
B1
B2
A0
A0
$\overline{A0}$
A1
A1
$\overline{A2}$
A2
A2
B0
B1
$\overline{A2}$
B2
G012
B0
B0
$\overline{A0}$
B1
B1
$\overline{A1}$
B2
B2
B0
B2
B[0:2]
$\overline{A1}$
$\overline{A2}$
B0
$\overline{B0}$
B1
$\overline{A0}$
B1
$\overline{B1}$
$\overline{A1}$
$\overline{A2}$
B2
$\overline{B2}$
B0
A0
$\overline{B0}$
A1
$\overline{B1}$
P012
A2
$\overline{B[0:2]}$
$\overline{B2}$

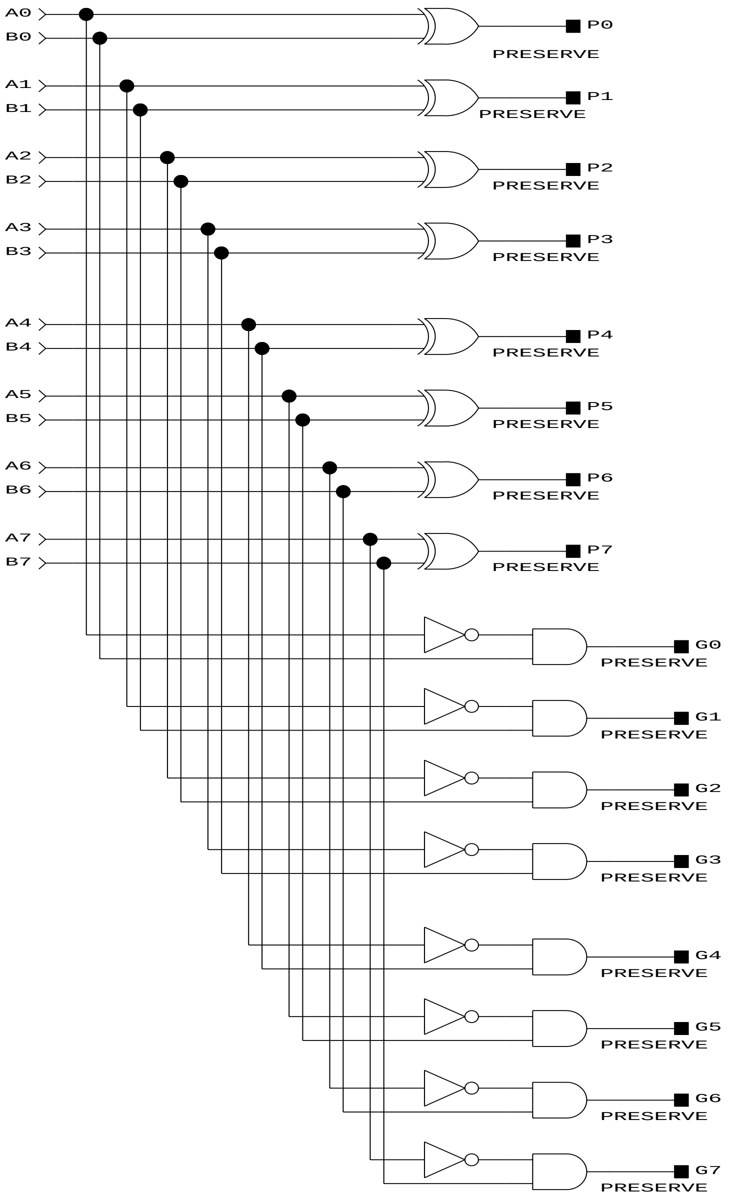
F3SUB. 2


$\overline{B[0:2]}$
$\overline{BI}$
BI
B[0:2]
$\overline{A[0:1]}$
A[0:2]
A2
A0
A1
B2
$\overline{BI}$
$\overline{A0}$
$\overline{A1}$
$\overline{B2}$
A0
A1
$\overline{B0}$
B2
A1
$\overline{B0}$
B2
$\overline{BI}$
$\overline{A0}$
$\overline{A1}$
B0
$\overline{B2}$
$\overline{A1}$
B0
$\overline{B2}$
BI
A0
$\overline{B1}$
B2
$\overline{BI}$
A0
$\overline{B0}$
$\overline{B1}$
B2
$\overline{B0}$
$\overline{B1}$
B2
$\overline{BI}$
$\overline{A1}$
$\overline{B2}$
B1
$\overline{A0}$
B1
$\overline{B2}$
BI
$\overline{A0}$
B0
B1
$\overline{B2}$
A1
$\overline{B1}$
B2
B0
B1
$\overline{B2}$
BI
LX2
Z2

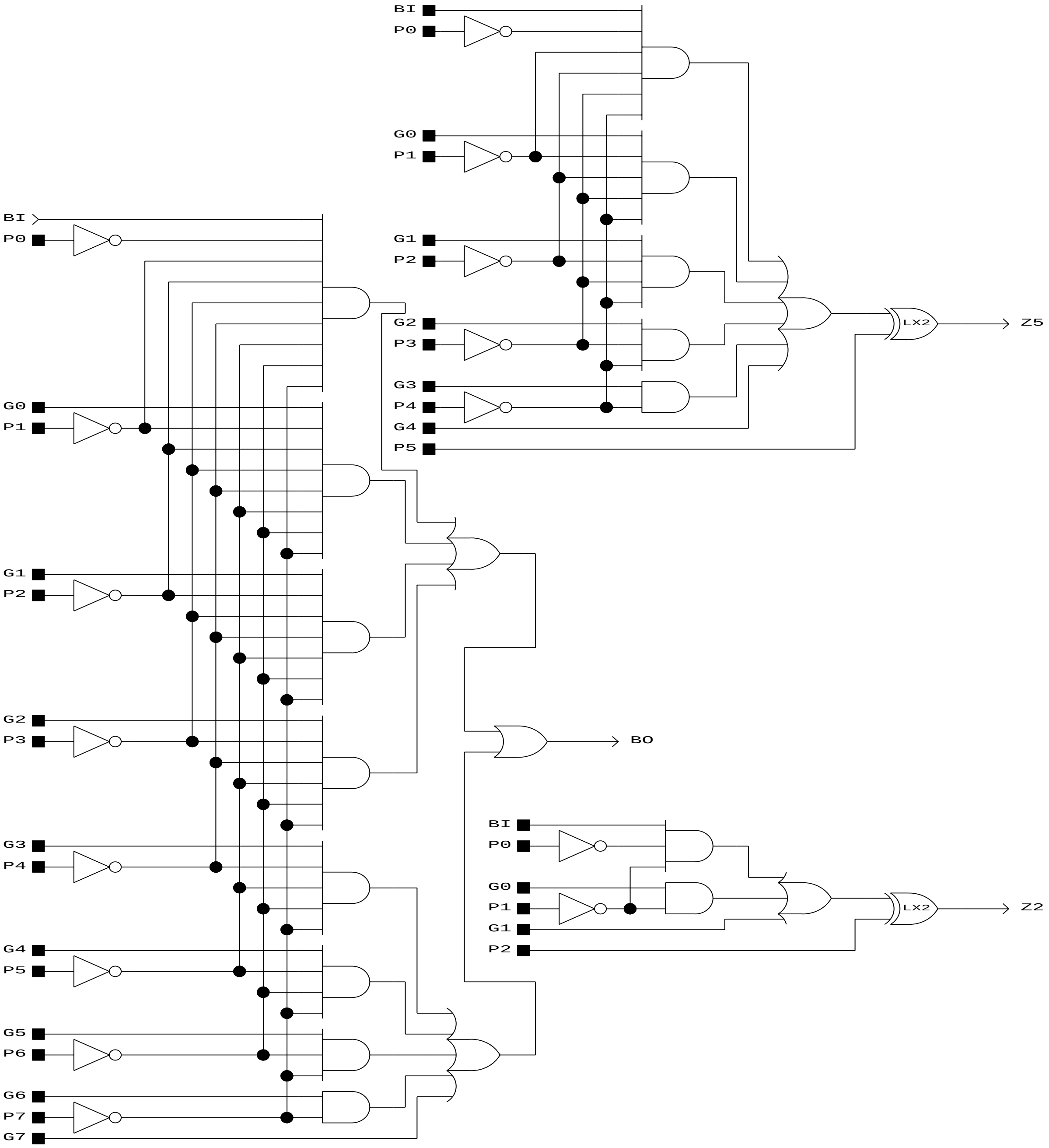
SUBF4


A-B
BI
A0
A1
B0
B1
Z0
Z1
BO
SUBF2
PRESERVE
A-B
BI
A0
A1
B0
B1
Z0
Z1
BO
SUBF2
BI
A0
A1
B0
B1
Z0
Z1
A2
A3
B2
B3
Z2
Z3
BO

SUBF8.1


A0
B0
A1
B1
A2
B2
A3
B3
A4
B4
A5
B5
A6
B6
A7
B7
P0
PRESERVE
P1
PRESERVE
P2
PRESERVE
P3
PRESERVE
P4
PRESERVE
P5
PRESERVE
P6
PRESERVE
P7
PRESERVE
G0
PRESERVE
G1
PRESERVE
G2
PRESERVE
G3
PRESERVE
G4
PRESERVE
G5
PRESERVE
G6
PRESERVE
G7
PRESERVE

SUBF8.2


BI
P0
G0
P1
G1
P2
G2
P3
G3
P4
G4
P5
LX2
Z5
BI
P0
G0
P1
G1
P2
G2
P3
G3
P4
G4
P5
G5
P6
G6
P7
G7
BO
BI
P0
G0
P1
G1
P2
LX2
Z2

SUBH1, SUBH2, SUBH3, SUBH4, SUBH8, SUBH8A, and SUBH16A

Function:

SUBH1:	1-bit half subtractor.
SUBH2:	2-bit half subtractor.
SUBH3:	3-bit half subtractor.
SUBH4:	4-bit half subtractor.
SUBH8:	8-bit half subtractor.
SUBH8A:	8-bit half subtractor built with propagate-generate submacros.
SUBH16A:	16-bit half subtractor built with propagate-generate submacros.

Availability:

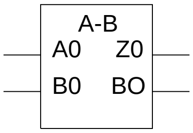
SUBH1, SUBH2, SUBH3, SUBH4, SUBH8, SUBH8A, and SUBH16A can be used with 1000, 2000, 3000, 5000, and 8000 devices.

An additional symbol and schematics appear on the following pages.

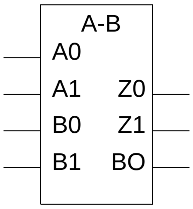
Type:

Soft:	SUBH1, SUBH2, SUBH3, SUBH8A, SUBH16A
Hard:	SUBH4, SUBH8

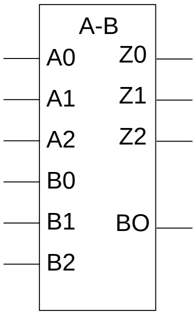
SUBH1



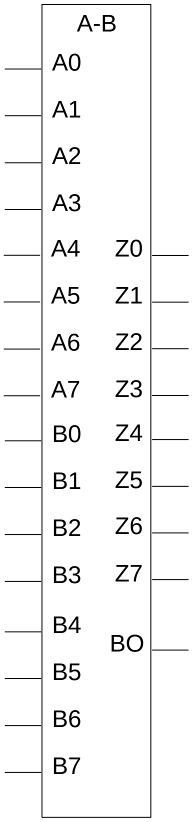
SUBH2



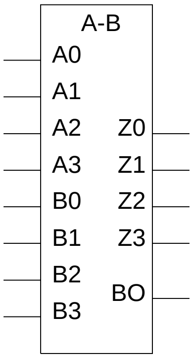
SUBH3



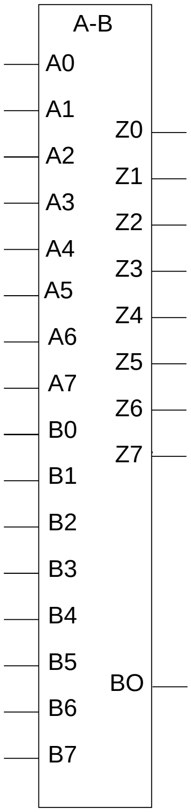
SUBH8



SUBH4



SUBH8A



Logic Resources:

Macro	PT	GLB	Output	Level
SUBH4	****	2	6	2
SUBH8	*****	6	22	3

****	Z0: 2 PT	Z1: 6 PT	Z2: 4 PT
	Z3: 7 PT	BO: 7 PT	TBO: 3 PT
*****	Z0: 2 PT	Z1: 2 PT	Z2: 3 PT
	Z3: 4 PT	Z4: 5 PT	Z5: 9 PT
	Z6: 11 PT	Z7: 8 PT	BO: 7 PT
	BB: 3 PT	G1-G5: 1 PT	P1-P7: 2 PT

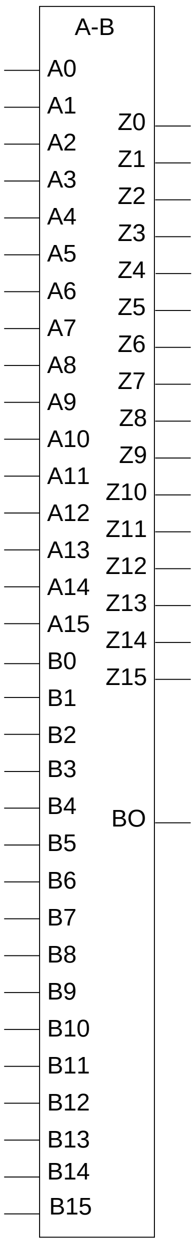
Truth Table:

The value of BO depends on the difference of A–B.

Input		**Output**	
A_{n-1}~A0	**B_{n-1}~B0**	**Z_{n-1}~Z0**	**BO**
data	data	A–B	*

* If B≤A, BO = 0. If B>A, BO = 1.

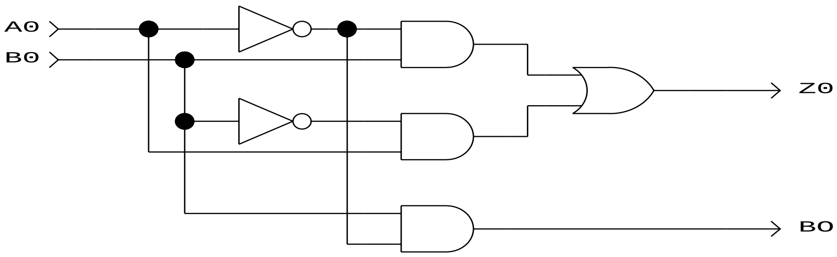
SUBH16A



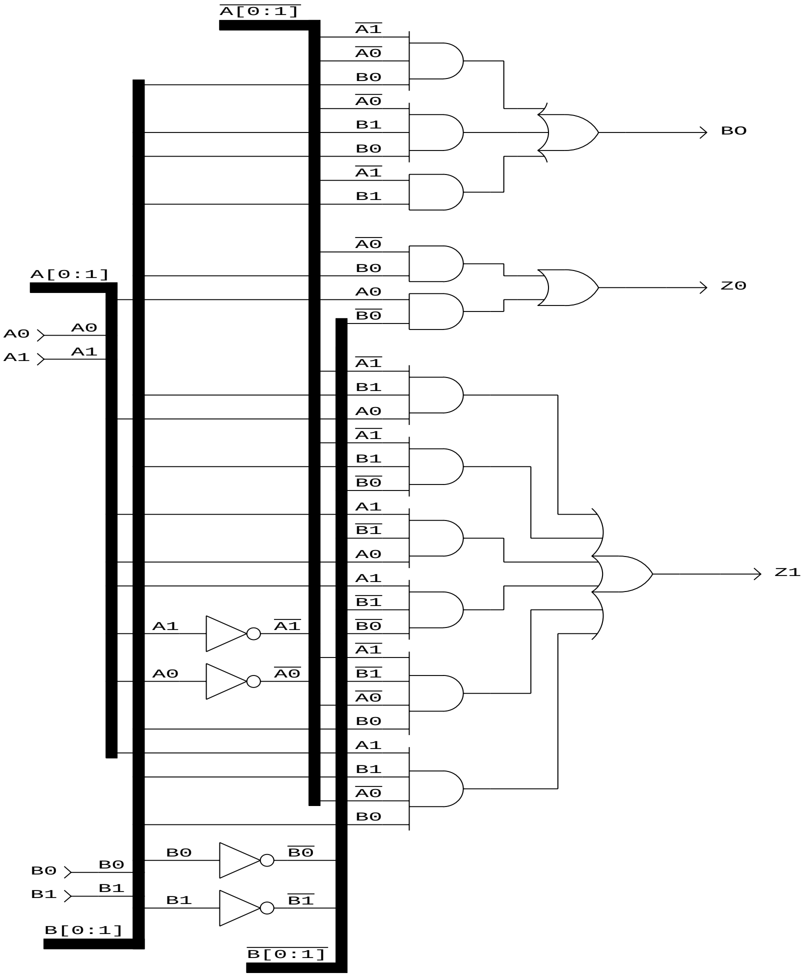
Macro Port Definition:

```
SUBH1 (Z0,BO,A0,B0);
SUBH2 (Z0,Z1,BO,A0,A1,B0,B1);
SUBH3 ([Z0..Z2],BO,[A0..A2],[B0..B2]);
  SUBH3_1 (Z0,A0,B0);
  SUBH3_2 (Z1,Z2,BO,A0,A1,A2,B0,B1,B2);
SUBH4  ([Z0..Z3],BO,[A0..A3],[B0..B3]);
  SUBH4_1 (Z0,Z1,TBO,A0,A1,B0,B1);
  SUBH4_2 (Z2,Z3,BO,A2,A3,B2,B3,TBO);
SUBH8 ([Z0..Z7],BO,[A0..A7],[B0..B7]);
  SUBH8_1 (BO,Z1,Z3,[P1..P7],[G1..G5],A0,B0,BB);
  SUBH8_2 (Z0,Z2,Z4,Z7,[P1..P7],[G1..G5],A0,A6,B0,B6);
  SUBH8_3 (Z6,[P1..P6],[G1..G5],A0,A4,A5,B0,B4,B5);
  SUBH8_4 (Z5,[P1..P5],[G1..G4],A0,A1,A3,B0,B1,B3);
  SUBH8_5 (G2,P2,P1,A1,A2,B1,B2);
  SUBH8_6 (BB,[P5..P7],[A5..A7],[B5..B7]);
SUBH8A ([Z0..Z7],BO,[A0..A7],[B0..B7]);
  SUBH8A_1 (Z0,A0,B0,BB2,BI,P345,G345);
  SUBH8A_2 (Z1,Z2,BB2,A0,A1,A2,B0,B1,B2);
  SUBH8A_3 (Z3,Z4,G345,A3,A4,A5,B3,B4,B5,BB2);
  SUBH8A_4 (Z5,P345,A3,A4,A5,B3,B4,B5,BB2);
  SUBH8A_5 (Z6,Z7,BO,A6,A7,B6,B7,BI);
SUBH16A ([Z0..Z15],BO,[A0..A15],[B0..B15]);
  SUBH16A_1  (Z0,Z15,BO,A0,A15,B0,B15,BB14);
  SUBH16A_2  (Z1,Z2,BB2,A0,A1,A2,B0,B1,B2);
  SUBH16A_3  (Z3,Z4,G345,A3,A4,A5,B3,B4,B5,BB2);
  SUBH16A_4  (Z5,P345,A3,A4,A5,B3,B4,B5,BB2);
  SUBH16A_5  (Z6,Z7,G678,A6,A7,A8,B6,B7,B8,BB5);
  SUBH16A_6  (Z8,P678,A6,A7,A8,B6,B7,B8,BB5);
  SUBH16A_7  (Z9,Z10,G911,A9,A10,A11,B9,B10,B11,BB8);
  SUBH16A_8  (Z11,P911,A9,A10,A11,B9,B10,B11,BB8);
  SUBH16A_9  (Z12,Z13,G1214,A12,A13,A14,B12,B13,B14,BB11);
  SUBH16A_10 (Z14,P1214,A12,A13,A14,B12,B13,B14,BB11);
  SUBH16A_11 (BB5,BB8,BB11,BB14,BB2,P345,G345,P678,G678,P911,
              G911,P1214,G1214);
```

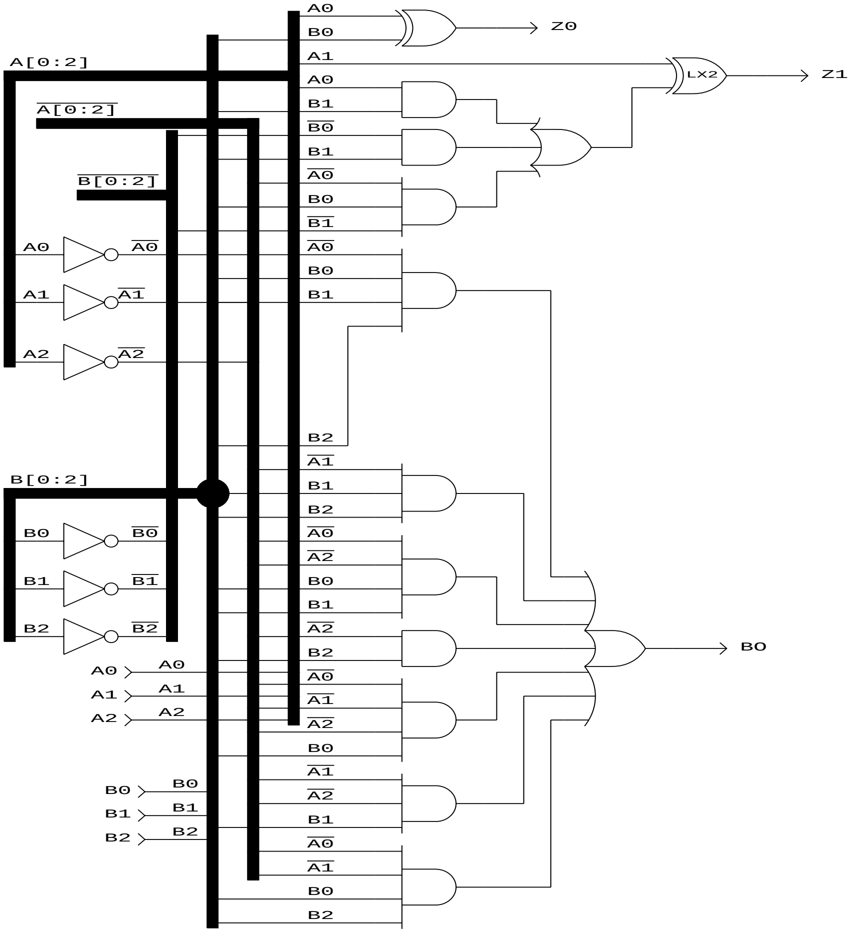
SUBH1



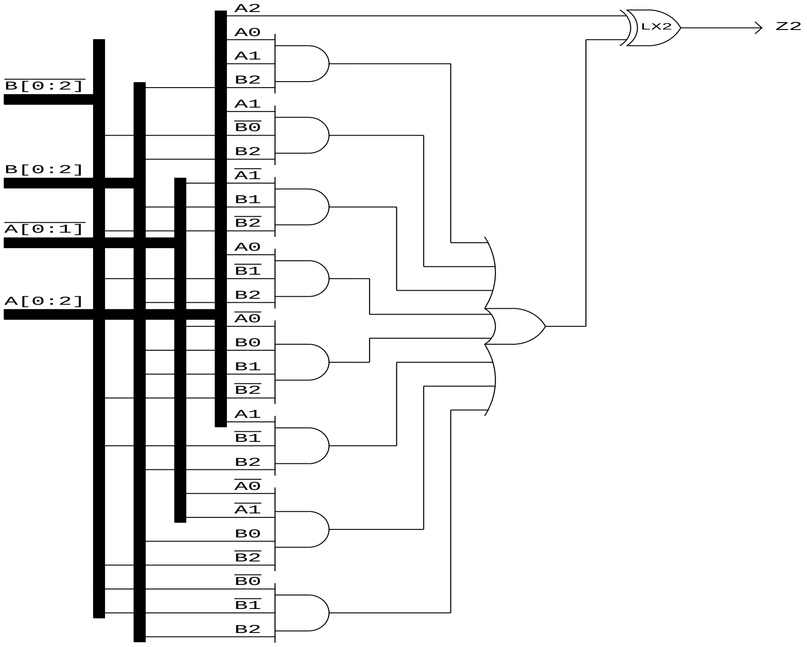
SUBH2


$\overline{A[0:1]}$
$\overline{A1}$
$\overline{A0}$
B0
$\overline{A0}$
B1
B0
$\overline{A1}$
B1
BO
$\overline{A0}$
B0
A0
$\overline{B0}$
Z0
A[0:1]
A0
A0
A1
A1
$\overline{A1}$
B1
A0
$\overline{A1}$
B1
$\overline{B0}$
A1
$\overline{B1}$
A0
A1
$\overline{B1}$
$\overline{B0}$
Z1
A1
$\overline{A1}$
$\overline{A1}$
A0
$\overline{A0}$
$\overline{B1}$
$\overline{A0}$
B0
A1
B1
$\overline{A0}$
B0
B0
$\overline{B0}$
B0
B0
B1
B1
B1
$\overline{B1}$
B[0:1]
$\overline{B[0:1]}$

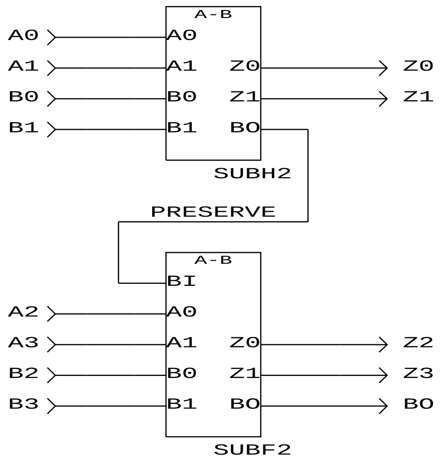
SUBH3.1


A0
B0
Z0
A1
LX2
Z1
A0
B1
$\overline{B0}$
B1
$\overline{A0}$
B0
$\overline{B1}$
$\overline{A0}$
B0
B1
B2
$\overline{A1}$
B1
B2
$\overline{A0}$
$\overline{A2}$
B0
B1
$\overline{A2}$
B2
$\overline{A0}$
$\overline{A1}$
$\overline{A2}$
B0
$\overline{A1}$
$\overline{A2}$
B1
$\overline{A0}$
$\overline{A1}$
B0
B2
BO
A[0:2]
$\overline{A[0:2]}$
$\overline{B[0:2]}$
A0
$\overline{A0}$
A1
$\overline{A1}$
A2
$\overline{A2}$
B[0:2]
B0
$\overline{B0}$
B1
$\overline{B1}$
B2
$\overline{B2}$
A0
A0
A1
A1
A2
A2
B0
B0
B1
B1
B2
B2

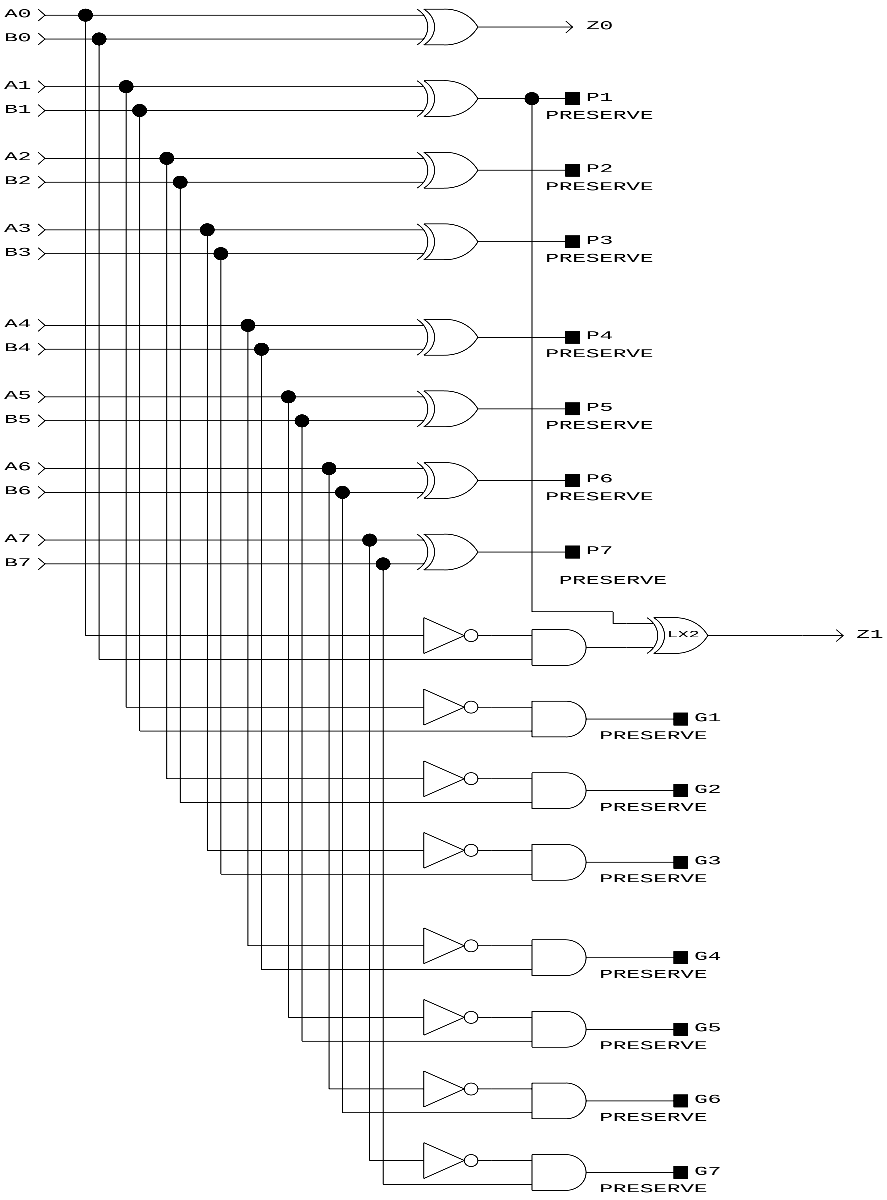
SUBH3.2


$\overline{B[0:2]}$
B[0:2]
$\overline{A[0:1]}$
A[0:2]
A2
A0
A1
B2
A1
$\overline{B0}$
B2
$\overline{A1}$
B1
$\overline{B2}$
A0
$\overline{B1}$
B2
$\overline{A0}$
B0
B1
$\overline{B2}$
A1
$\overline{B1}$
B2
$\overline{A0}$
$\overline{A1}$
B0
$\overline{B2}$
$\overline{B0}$
$\overline{B1}$
B2
LX2
Z2

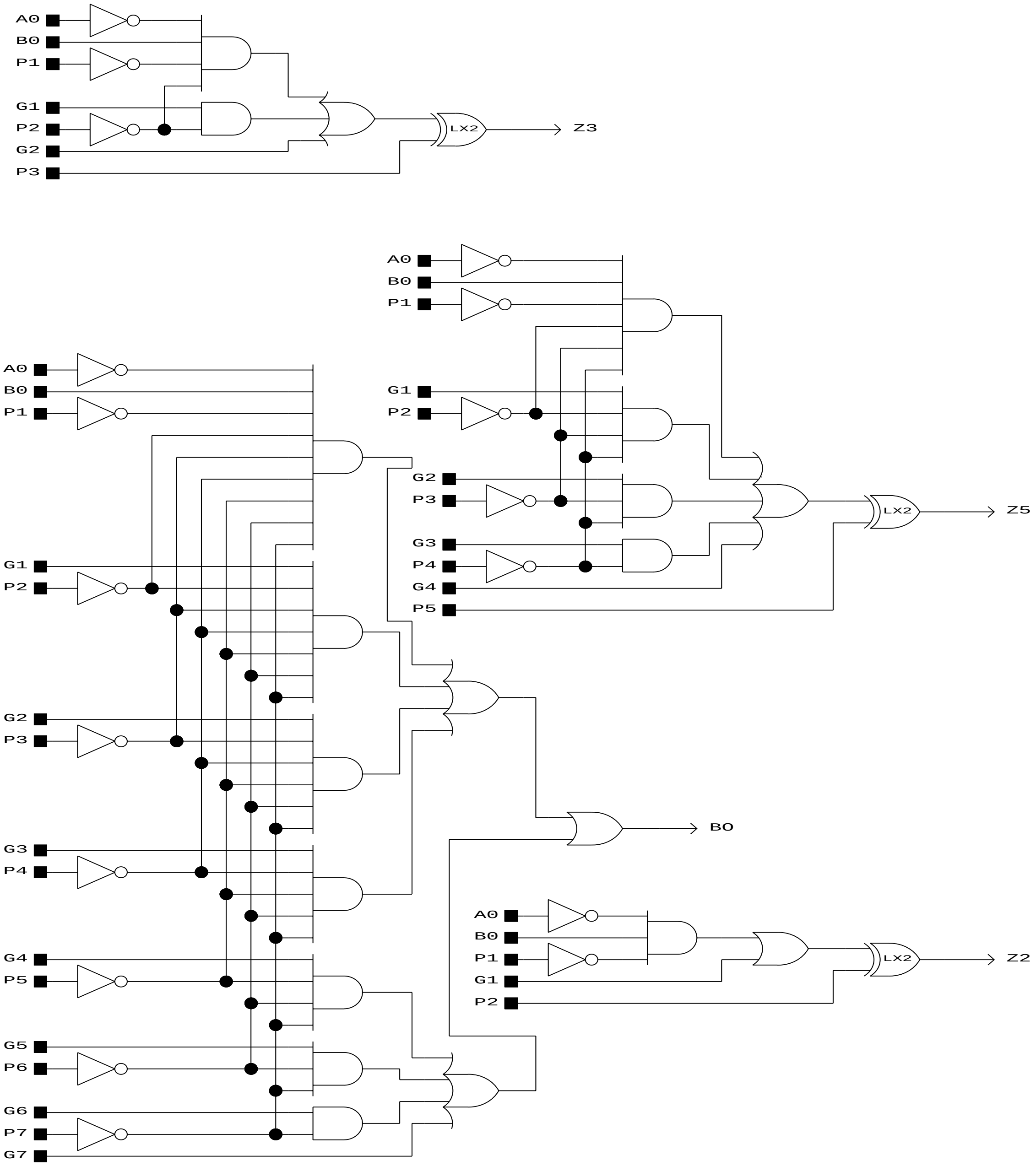
SUBH4


A-B
A0
A1
B0
B1
A0
A1
B0
B1
Z0
Z1
BO
Z0
Z1
SUBH2
PRESERVE
A-B
BI
A2
A3
B2
B3
A0
A1
B0
B1
Z0
Z1
BO
Z2
Z3
BO
SUBF2

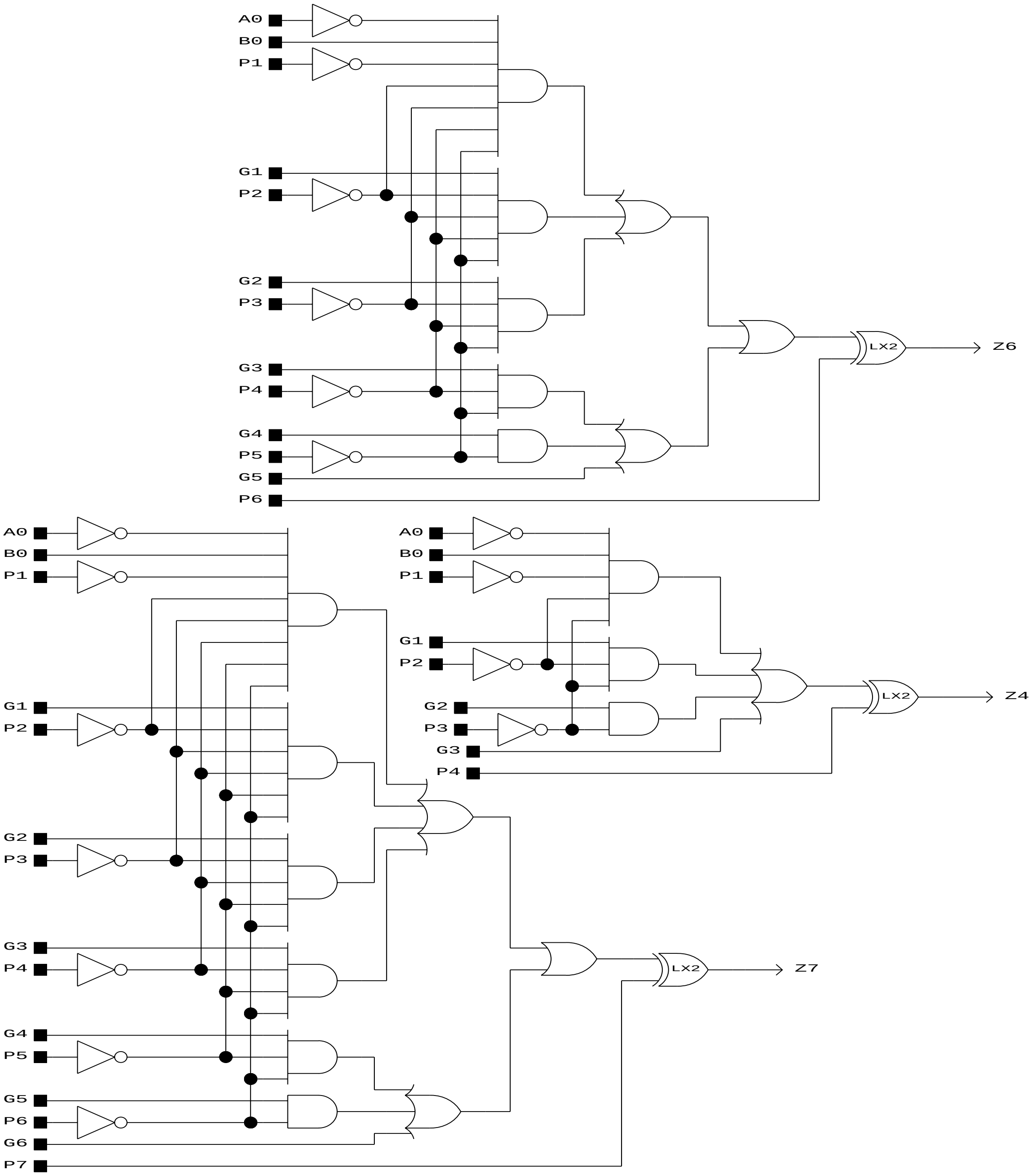
SUBH8.1


A0
B0
Z0
A1
B1
P1
PRESERVE
A2
B2
P2
PRESERVE
A3
B3
P3
PRESERVE
A4
B4
P4
PRESERVE
A5
B5
P5
PRESERVE
A6
B6
P6
PRESERVE
A7
B7
P7
PRESERVE
LX2
Z1
G1
PRESERVE
G2
PRESERVE
G3
PRESERVE
G4
PRESERVE
G5
PRESERVE
G6
PRESERVE
G7
PRESERVE

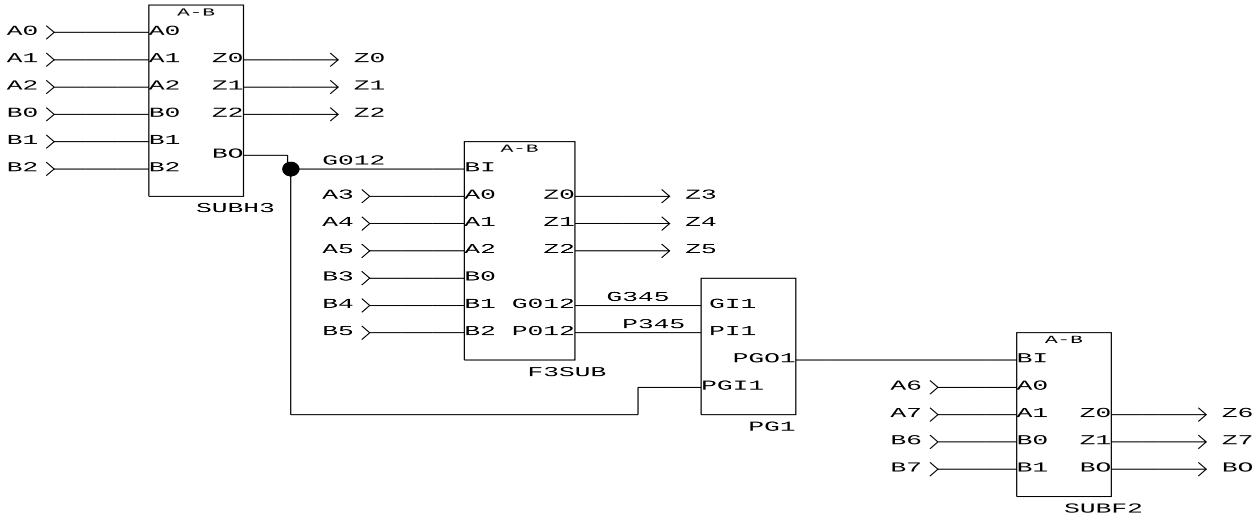
SUBH8.2


A0
B0
P1
G1
P2
G2
P3
LX2
Z3
A0
B0
P1
G1
P2
G2
P3
G3
P4
G4
P5
LX2
Z5
A0
B0
P1
G1
P2
G2
P3
G3
P4
G4
P5
G5
P6
G6
P7
G7
B0
A0
B0
P1
G1
P2
LX2
Z2

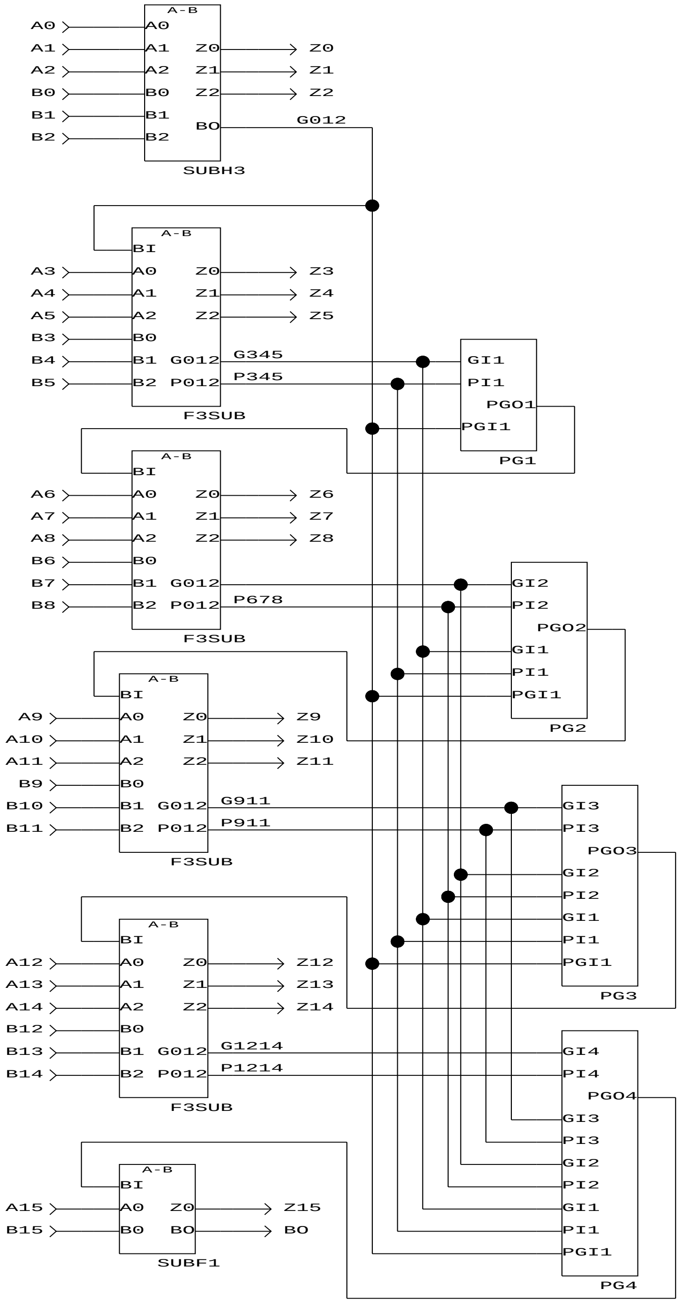
SUBH8.3


A0
B0
P1
G1
P2
G2
P3
G3
P4
G4
P5
G5
P6
LX2
Z6
A0
B0
P1
G1
P2
G2
P3
G3
P4
G4
P5
G5
P6
G6
P7
LX2
Z7
A0
B0
P1
G1
P2
G2
P3
G3
P4
LX2
Z4

SUBH8A


A-B
A0
A1
A2
B0
B1
B2
A0
A1
A2
B0
B1
B2
Z0
Z1
Z2
BO
Z0
Z1
Z2
SUBH3
G012
A-B
BI
A3
A4
A5
B3
B4
B5
A0
A1
A2
B0
B1
B2
Z0
Z1
Z2
G012
P012
Z3
Z4
Z5
F3SUB
G345
P345
GI1
PI1
PGO1
PGI1
PG1
A-B
BI
A6
A7
B6
B7
A0
A1
B0
B1
Z0
Z1
BO
Z6
Z7
BO
SUBF2

SUBH16A


A-B
A0
A1
A2
B0
B1
B2
Z0
Z1
Z2
BO
G012
SUBH3
BI
A3
A4
A5
B3
B4
B5
Z3
Z4
Z5
G012
P012
G345
P345
F3SUB
GI1
PI1
PGO1
PGI1
PG1
A6
A7
A8
B6
B7
B8
Z6
Z7
Z8
P678
GI2
PI2
PGO2
PG2
A9
A10
A11
B9
B10
B11
Z9
Z10
Z11
G911
P911
GI3
PI3
PGO3
PG3
A12
A13
A14
B12
B13
B14
Z12
Z13
Z14
G1214
P1214
GI4
PI4
PGO4
PG4
A15
B15
Z15
BO
SUBF1

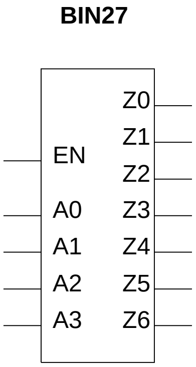
Coders

This chapter contains information on the following macros:

- Decoders
- Encoders

Decoders

BIN27



Function:

Binary to seven segment decoder with enable. A high level on an output turns on the segment.

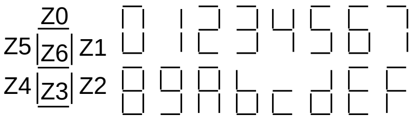
Availability:

BIN27 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Soft

Macro Port Definition:

```
BIN27 ([Z0..Z6],[A0..A3],EN);
  BIN27_1 ([Z0..Z2],[A0..A3],EN);
  BIN27_2 ([Z3..Z6],[A0..A3],EN);
```



Segment Map:

Each BIN27 output corresponds to one of 7 segments. Combinations of these segments form hexadecimal digits.

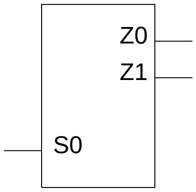
Truth Table:

Input					Output							Character
EN	A3	A2	A1	A0	Z0	Z1	Z2	Z3	Z4	Z5	Z6	
1	0	0	0	0	1	1	1	1	1	1	0	0
1	0	0	0	1	0	1	1	0	0	0	0	1
1	0	0	1	0	1	1	0	1	1	0	1	2
1	0	0	1	1	1	1	1	1	0	0	1	3
1	0	1	0	0	0	1	1	0	0	1	1	4
1	0	1	0	1	1	0	1	1	0	1	1	5
1	0	1	1	0	1	0	1	1	1	1	1	6
1	0	1	1	1	1	1	1	0	0	0	0	7
1	1	0	0	0	1	1	1	1	1	1	1	8
1	1	0	0	1	1	1	1	1	0	1	1	9
1	1	0	1	0	1	1	1	0	1	1	1	A
1	1	0	1	1	0	0	1	1	1	1	1	B
1	1	1	0	0	0	0	0	1	1	0	1	C
1	1	1	0	1	0	1	1	1	1	0	1	D
1	1	1	1	0	1	0	0	1	1	1	1	E
1	1	1	1	1	1	0	0	0	1	1	1	F
0	x	x	x	x	0	0	0	0	0	0	0	Off

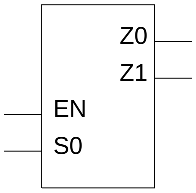
x = don’t care.

DEC2 and DEC2E

DEC2



DEC2E



Function:

DEC2: 1 to 2 decoder.
DEC2E: 1 to 2 decoder with enable.

Availability:

DEC2 and DEC2E can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Soft

Macro Port Definition:

```
DEC2 (Z0,Z1,S0);
DEC2E (Z0,Z1,EN,S0);
```

Truth Table:

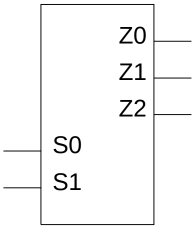
Gray areas (EN) apply only to DEC2E.

Input		**Output**	
EN	**S0**	**Z0**	**Z1**
1	0	1	0
1	1	0	1
0	x	0	0

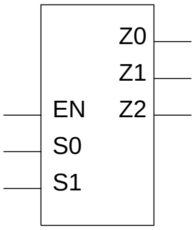
x = don’t care.

DEC3 and DEC3E

DEC3



DEC3E



Function:

DEC3:	1 to 3 decoder.
DEC3E:	1 to 3 decoder with enable.

Availability:

DEC3 and DEC3E can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Soft

Macro Port Definition:

```
DEC3 (Z0,Z1,Z2,S0,S1);
DEC3E (Z0,Z1,Z2,EN,S0,S1);
```

Truth Table:

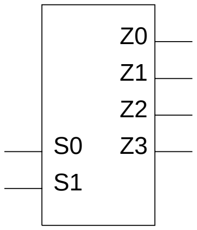
Gray areas (EN) apply only to DEC3E.

Input			**Output**		
EN	**S1**	**S0**	**Z0**	**Z1**	**Z2**
1	0	0	1	0	0
1	0	1	0	1	0
1	1	0	0	0	1
1	1	1	0	0	0
1	x	x	0	0	0

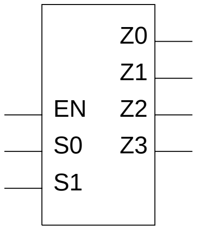
x = don’t care.

DEC4 and DEC4E

DEC4



DEC4E



Function:

DEC4: 1 to 4 decoder.
DEC4E: 1 to 4 decoder with enable.

Availability:

DEC4 and DEC4E can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Soft

Macro Port Definition:

```
DEC4 ([Z0..Z3],S0,S1);
DEC4E ([Z0..Z3],EN,S0,S1);
```

Truth Table:

Gray areas (EN) apply only to DEC4E.

Input			Output			
EN	**S1**	**S0**	**Z0**	**Z1**	**Z2**	**Z3**
1	0	0	1	0	0	0
1	0	1	0	1	0	0
1	1	0	0	0	1	0
1	1	1	0	0	0	1
0	x	x	0	0	0	0

x = don’t care.

Encoders

PREN8 and PREN8E

Function:

PREN8: 7-line to 3-line priority encoder.
PREN8E: 7-line to 3-line priority encoder with enable.

Availability:

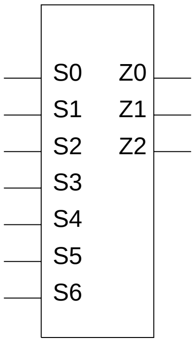
PREN8 and PREN8E can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Soft

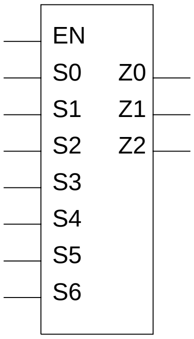
Macro Port Definition:

```
PREN8 ([Z0..Z2],[S0..S6]);
PREN8E ([Z0..Z2],[S0..S6],EN);
```

PREN8



PREN8E



Truth Table:

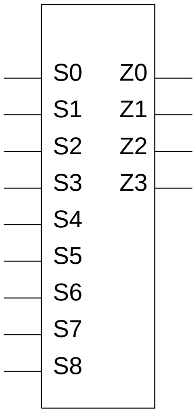
Gray areas (EN) apply only to PREN8E.

Input								Output		
EN	**S0**	**S1**	**S2**	**S3**	**S4**	**S5**	**S6**	**Z2**	**Z1**	**Z0**
1	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	1
1	x	1	0	0	0	0	0	0	1	0
1	x	x	1	0	0	0	0	0	1	1
1	x	x	x	1	0	0	0	1	0	0
1	x	x	x	x	1	0	0	1	0	1
1	x	x	x	x	x	1	0	1	1	0
1	x	x	x	x	x	x	1	1	1	1
0	x	x	x	x	x	x	x	0	0	0

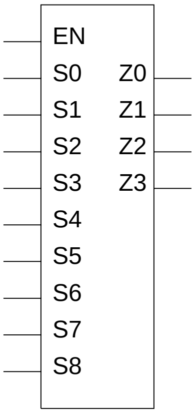
x = don't care

PREN10 and PREN10E

PREN10



PREN10E



Function:

PREN10: 9-line to 4-line priority encoder.
PREN10E: 9-line to 4-line priority encoder with enable.

Availability:

PREN10 and PREN10E can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Soft

Macro Port Definition:

```
PREN10 ([Z0..Z3],[S0..S8]);
PREN10E ([Z0..Z3],[S0..S8],EN);
```

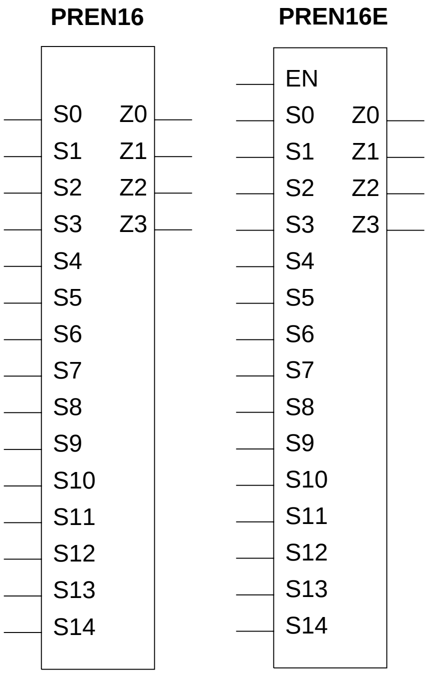
Truth Table:

Gray areas (EN) apply only to PREN10E.

Input										Output			
EN	**S0**	**S1**	**S2**	**S3**	**S4**	**S5**	**S6**	**S7**	**S8**	**Z3**	**Z2**	**Z1**	**Z0**
1	0	0	0	0	0	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	0	0	1
1	x	1	0	0	0	0	0	0	0	0	0	1	0
1	x	x	1	0	0	0	0	0	0	0	0	1	1
1	x	x	x	1	0	0	0	0	0	0	1	0	0
1	x	x	x	x	1	0	0	0	0	0	1	0	1
1	x	x	x	x	x	1	0	0	0	0	1	1	0
1	x	x	x	x	x	x	1	0	0	0	1	1	1
1	x	x	x	x	x	x	x	1	0	1	0	0	0
1	x	x	x	x	x	x	x	x	1	1	0	0	1
0	x	x	x	x	x	x	x	x	x	0	0	0	0

x = don’t care.

PREN16 and PREN16E



Function:

PREN16: 15-line to 4-line priority encoder.
PREN16E: 15-line to 4-line priority encoder with enable.

Availability:

PREN16 and PREN16E can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Soft

Macro Port Definition:

```
PREN16 ([Z0..Z3],[S0..S14]);
  PREN16_1 (Z0,Z1,[S0..S14]);
  PREN16_2 (Z2,Z3,[S3..S14]);
PREN16E ([Z0..Z3],[S0..S14],EN);
  PREN16E_1 (Z0,Z1,[S0..S14],EN);
  PREN16E_2 (Z2,Z3,[S3..S14],EN);
```

Truth Table:

Gray areas (EN) apply only to PREN16E. Some areas of this table are not shown. Refer to the PREN10/10E truth table for the logic pattern.

Input										**Output**			
EN	**S0**	**S1**	**S2**	**S3**		**S11**	**S12**	**S13**	**S14**	**Z3**	**Z2**	**Z1**	**Z0**
1	0	0	0	0		0	0	0	0	0	0	0	0
1	1	0	0	0		0	0	0	0	0	0	0	1
1	x	1	0	0		0	0	0	0	0	0	1	0
1	x	x	1	0	------	0	0	0	0	0	0	1	1
x	x	x	x	x		1	0	0	0	1	1	0	0
1	x	x	x	x		x	1	0	0	0	1	0	1
1	x	x	x	x		x	x	1	0	1	1	1	0
1	x	x	x	x	------	x	x	x	1	1	1	1	1
0	x	x	x	x		x	x	x	x	0	0	0	0

x = don’t care.

Counters

This chapter contains information on the following macros:

- Binary Counters
- Decade Counters
- Gray Code Counters

Binary Counters

CBD11, CBD12, CBD14, and CBD18

Function:

1-, 2-, 4-, and 8-bit down counters with asynchronous clear, CAI, and CAO.

Availability:

CBD11, CBD12, CBD14, and CBD18 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Schematics appear on the following pages.

Type:

Soft:	CBD11 and CBD12.
Hard:	CBD14 and CBD18.

Logic Resources:

Macro	PT	GLB	Output	Level
CBD14	*	2	5	1**
CBD18	*	3	9	1**

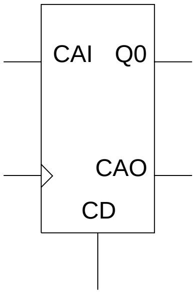
* Q0-Q_{n-1}: 2 PT per output.
CAO: 1 PT.
CLK: 1 PT per GLB if Product Term Clock is used.
CD: 1 PT per GLB.

** (CAO is a 2-level output).

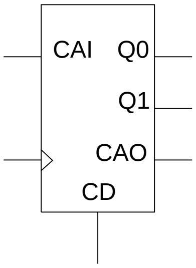
Macro Port Definition:

```
CBD11 (Q0,CAO,CAI,CLK,CD);
CBD12 (Q0,Q1,CAO,CAI,CLK,CD);
CBD14 ([Q0..Q3],CAO,CAI,CLK,CD);
  CBD14_1 ([Q0..Q3],CAI,CLK,CD);
  CBD14_2 (CAO,[Q0..Q3],CAI);
CBD18 ([Q0..Q7],CAO,CAI,CLK,CD);
  CBD18_1 ([Q0..Q3],CAI,CLK,CD);
  CBD18_2 ([Q4..Q7],[Q0..Q3],CAI,CLK,CD);
  CBD18_3 (CAO,[Q0..Q7],CAI);
```

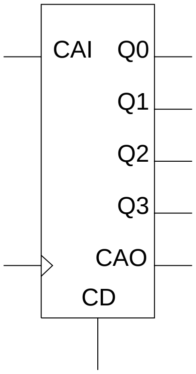
CBD11



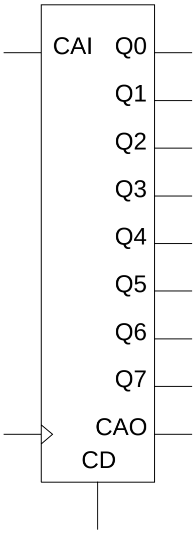
CBD12



CBD14



CBD18



Counting Ranges:

CBD11: 1-0. CBD12: 3-0. CBD14: 15-0. CBD18: 255-0.

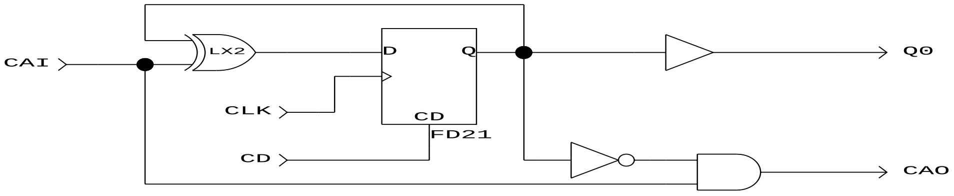
Truth Table:

The truth table is the same for all CBD1s.

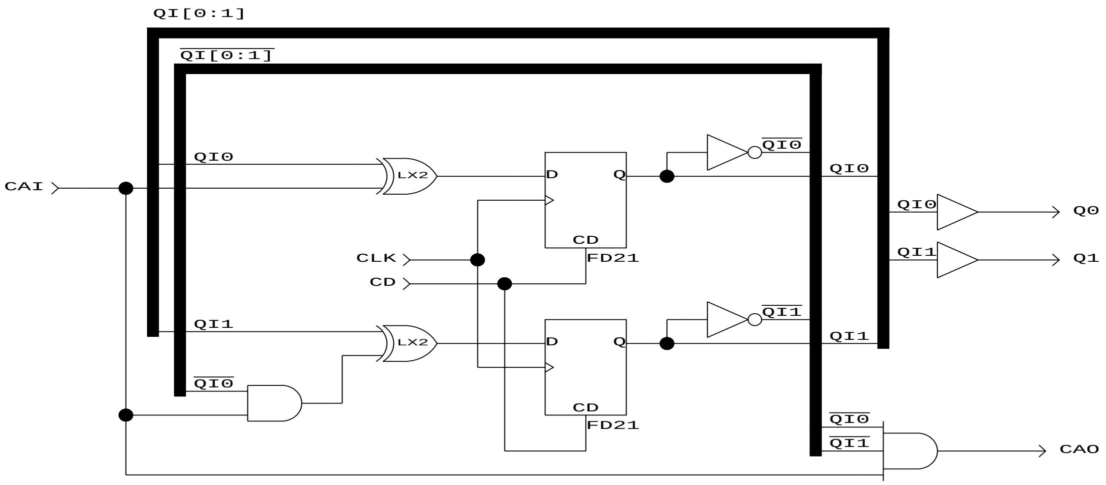
Input			**Output**	
CD	**CAI**	**CLK**	**Q**	**CAO**
1	x	x	0	CAI
0	0	x	Q	0
0	1	↑	count down	*

* CAO = 1 after terminal count, when CAI = 1.
CAI = shift registers: serial input; counters: CAscade In,
Q = output of flip-flop or latch, x = don’t care, ↑ = rising clock edge.

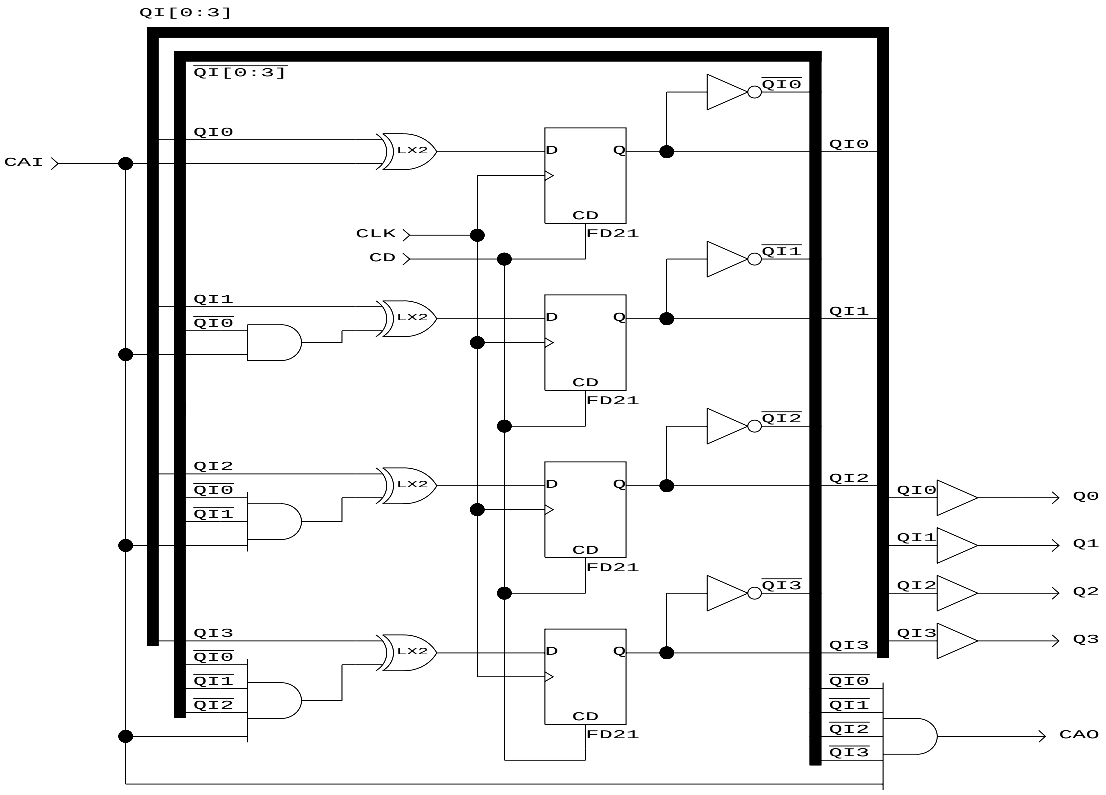
CBD11



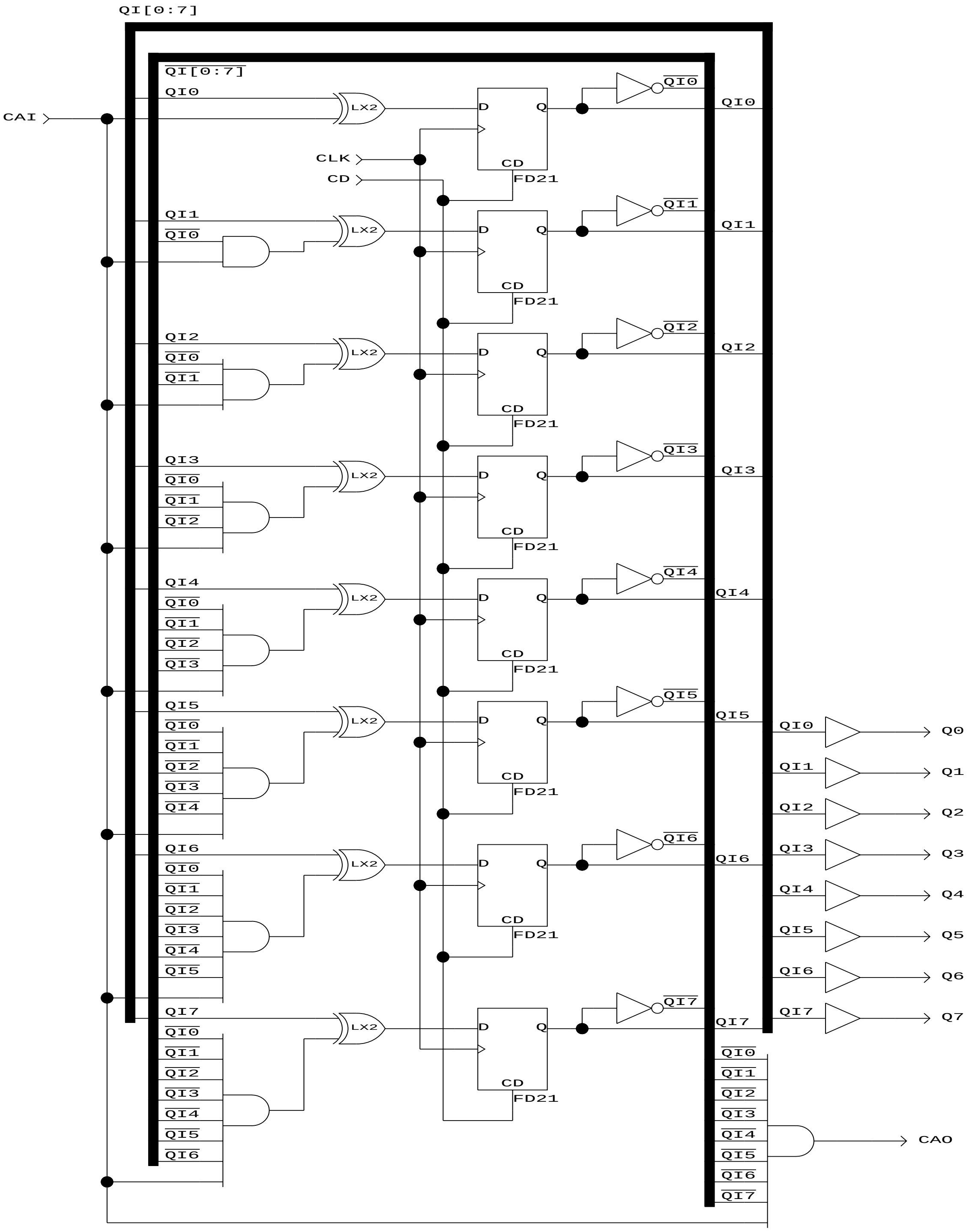
CBD12


QI[0:1]
$\overline{QI[0:1]}$
QI0
CAI
LX2
D
Q
CD
FD21
CLK
CD
$\overline{QI0}$
QI0
QI0
Q0
QI1
Q1
QI1
LX2
D
Q
$\overline{QI1}$
QI1
$\overline{QI0}$
CD
FD21
$\overline{QI0}$
$\overline{QI1}$
CAO

CBD14


QI[0:3]
$\overline{QI[0:3]}$
CAI
CLK
CD
QI0
QI1
$\overline{QI0}$
QI2
$\overline{QI0}$
$\overline{QI1}$
QI3
$\overline{QI0}$
$\overline{QI1}$
$\overline{QI2}$
LX2
LX2
LX2
LX2
D
Q
CD
FD21
D
Q
CD
FD21
D
Q
CD
FD21
D
Q
CD
FD21
$\overline{QI0}$
$\overline{QI1}$
$\overline{QI2}$
$\overline{QI3}$
QI0
QI1
QI2
QI3
QI0
QI1
QI2
QI3
Q0
Q1
Q2
Q3
$\overline{QI0}$
$\overline{QI1}$
$\overline{QI2}$
$\overline{QI3}$
CAO

CBD18


QI[0:7]
$\overline{QI[0:7]}$
CAI
CLK
CD
LX2
D
Q
CD
FD21
QI0
QI1
QI2
QI3
QI4
QI5
QI6
QI7
$\overline{QI0}$
$\overline{QI1}$
$\overline{QI2}$
$\overline{QI3}$
$\overline{QI4}$
$\overline{QI5}$
$\overline{QI6}$
$\overline{QI7}$
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
CAO

CBD21, CBD22, CBD24, and CBD28

Function:

1-, 2-, 4-, and 8-bit down counters with asynchronous clear, enable, CAI, and CAO.

Availability:

CBD21, CBD22, CBD24, and CBD28 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Schematics appear on the following pages.

Type:

Soft:	CBD21 and CBD22.
Hard:	CBD24 and CBD28.

Logic Resources:

Macro	PT	GLB	Output	Level
CBD24	*	2	5	1**
CBD28	*	3	9	1**

* Q0-Q_{n-1}: 2 PT per output.
CAO: 1 PT.
CLK: 1 PT per GLB if Product Term Clock is used.
CD: 1 PT per GLB.

** (CAO is a 2-level output).

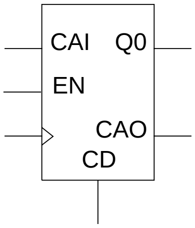
Macro Port Definition:

```
CBD21 (Q0,CAO,CAI,CLK,EN,CD);
CBD22 (Q0,Q1,CAO,CAI,CLK,EN,CD);
CBD24 ([Q0..Q3],CAO,CAI,CLK,EN,CD);
  CBD24_1 ([Q0..Q3],CAI,CLK,EN,CD);
  CBD24_2 (CAO,[Q0..Q3],CAI,EN);
CBD28 ([Q0..Q7],CAO,CAI,CLK,EN,CD);
  CBD28_1 ([Q0..Q3],CAI,CLK,EN,CD);
  CBD28_2 ([Q4..Q7],[Q0..Q3],CAI,CLK,EN,CD);
  CBD28_3 (CAO,[Q0..Q7],CAI,EN);
```

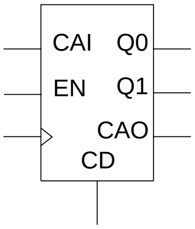
Counting Ranges:

CBD21: 1-0. CBD22: 3-0. CBD24: 15-0. CBD28: 255-0.

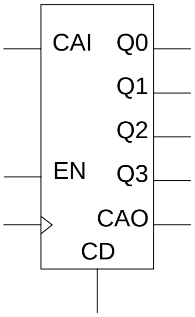
CBD21



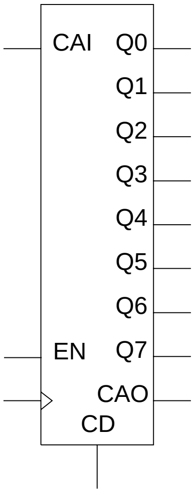
CBD22



CBD24



CBD28



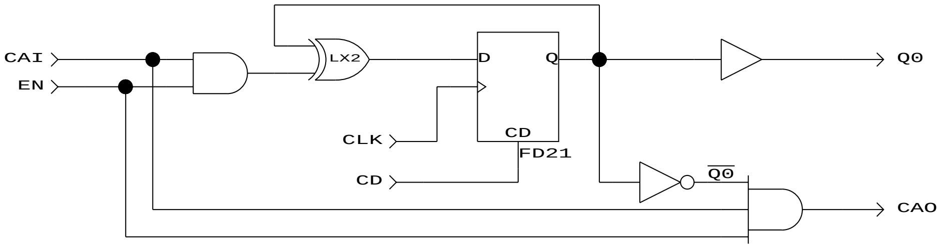
Truth Table:

The truth table is the same for all CBD2s.

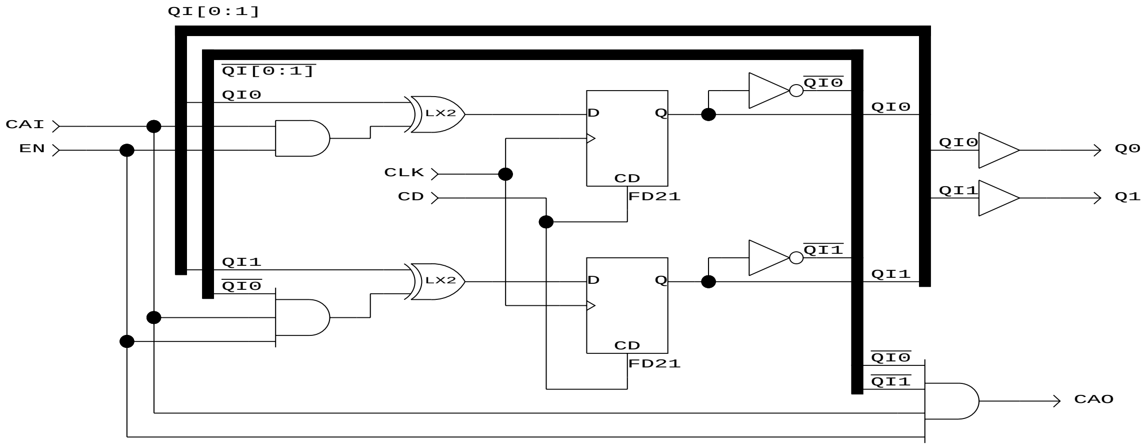
Input				Output	
CD	**EN**	**CAI**	**CLK**	**Q**	**CAO**
1	x	x	x	0	CAI·EN
0	0	x	x	Q	0
0	x	0	x	Q	0
0	1	1	↑	count down	*

* CAO = 1 after terminal count, when CAI = 1 and EN = 1
CAI·EN = shift registers: serial input; counters:
CAscade In, enable for multiplexors and counters, Q = output.

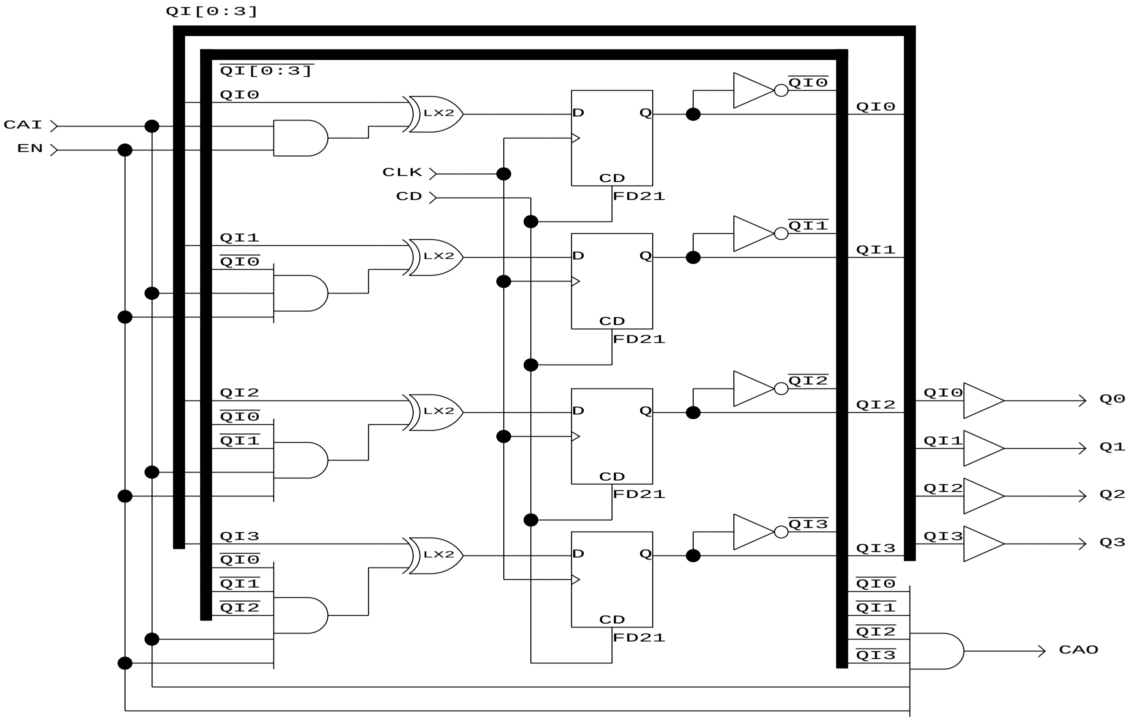
CBD21



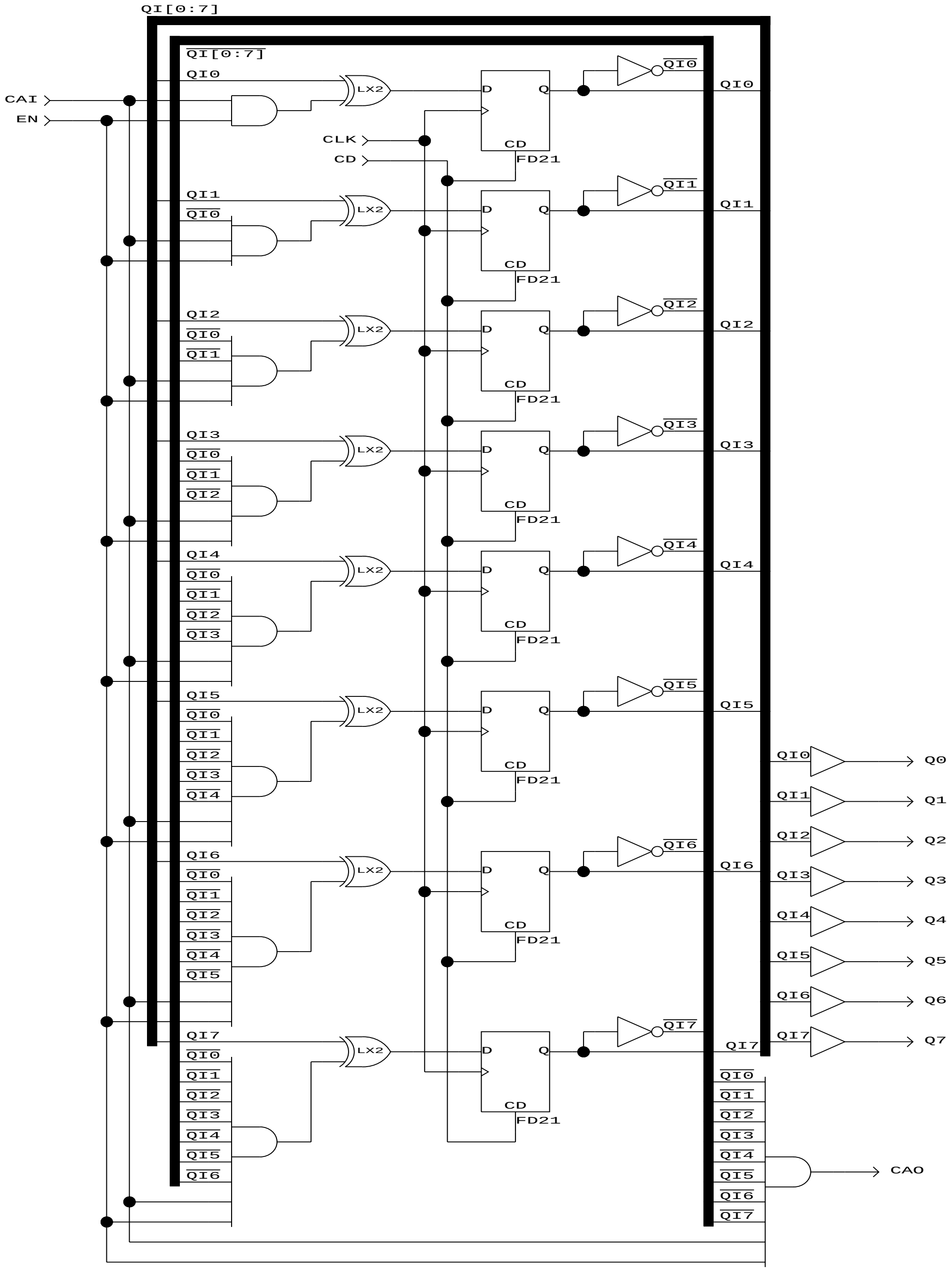
CBD22


QI[0:1]
$\overline{QI[0:1]}$
QI0
CAI
EN
LX2
D
Q
$\overline{QI0}$
QI0
QI0
Q0
CLK
CD
CD
FD21
QI1
Q1
QI1
$\overline{QI0}$
LX2
D
Q
$\overline{QI1}$
QI1
CD
FD21
$\overline{QI0}$
$\overline{QI1}$
CAO

CBD24

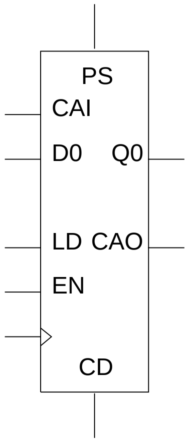

QI[0:3]
$\overline{QI[0:3]}$
QI0
CAI
EN
LX2
D
Q
CD
FD21
CLK
CD
$\overline{QI0}$
QI0
QI1
$\overline{QI0}$
LX2
D
Q
CD
FD21
$\overline{QI1}$
QI1
QI2
$\overline{QI0}$
$\overline{QI1}$
LX2
D
Q
CD
FD21
$\overline{QI2}$
QI2
QI0
Q0
QI1
Q1
QI2
Q2
QI3
Q3
QI3
$\overline{QI0}$
$\overline{QI1}$
$\overline{QI2}$
LX2
D
Q
CD
FD21
$\overline{QI3}$
QI3
$\overline{QI0}$
$\overline{QI1}$
$\overline{QI2}$
$\overline{QI3}$
CAO

CBD28

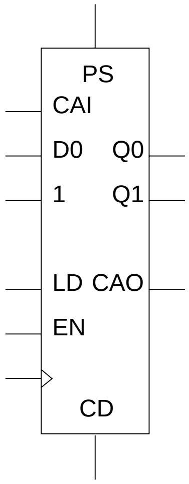

QI[0:7]
$\overline{\text{QI[0:7]}}$
CAI
EN
CLK
CD
QI0
QI1
QI2
QI3
QI4
QI5
QI6
QI7
$\overline{\text{QI0}}$
$\overline{\text{QI1}}$
$\overline{\text{QI2}}$
$\overline{\text{QI3}}$
$\overline{\text{QI4}}$
$\overline{\text{QI5}}$
$\overline{\text{QI6}}$
$\overline{\text{QI7}}$
LX2
D
Q
CD
FD21
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
CAO

CBD31, CBD32, CBD34, and CBD38

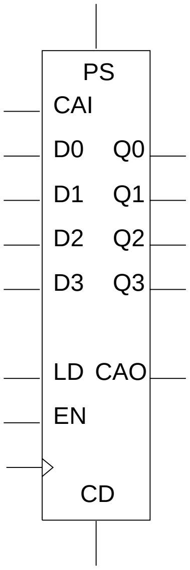
CBD31



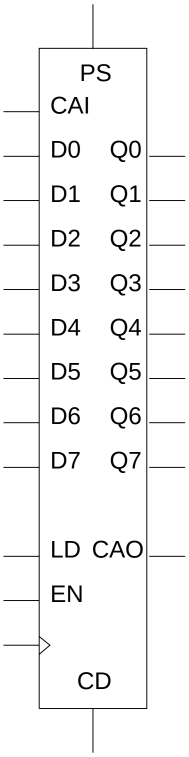
CBD32



CBD34



CBD38



Function:

1-, 2-, 4-, and 8-bit down counters with asynchronous clear, enable, parallel data load, synchronous preset, CAI, and CAO.

Availability:

CBD31, CBD32, CBD34, and CBD38 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Schematics appear on the following pages.

Type:

Soft:	CBD31 and CBD32.
Hard:	CBD34 and CBD38.

Logic Resources:

Macro	PT	GLB	Output	Level
CBD34	*	2	5	1**
CBD38	*	3	9	1**

* Q0-Q_{n-1}: 4 PT per output.
CAO: 1 PT.
CLK: 1 PT per GLB if Product Term Clock is used.
CD: 1 PT per GLB.

** (CAO is a 2-level output).

Macro Port Definition:

```
CBD31 (Q0,CAO,D0,CAI,CLK,PS,LD,EN,CD);
CBD32 (Q0,Q1,CAO,D0,D1,CAI,CLK,PS,LD,EN,CD);
CBD34 ([Q0..Q3],CAO,[D0..D3],CAI,CLK,PS,LD,EN,CD);
  CBD34_1 ([Q0..Q3],[D0..D3],CAI,CLK,PS,LD,EN,CD);
  CBD34_2 (CAO,[Q0..Q3],CAI,EN);
CBD38 ([Q0..Q7],CAO,[D0..D7],CAI,CLK,PS,LD,EN,CD);
  CBD38_1 ([Q0..Q3],[D0..D3],CAI,CLK,PS,LD,EN,CD);
  CBD38_2 (Q4,Q5,[Q0..Q3],D4,D5,CAI,CLK,PS,LD,EN,CD);
  CBD38_3 (Q6,Q7,[Q0..Q5],D6,D7,CAI,CLK,PS,LD,EN,CD);
  CBD38_4 (CAO,[Q0..Q7],CAI,EN);
```

Counting Ranges:

CBD31: 1-0. CBD32: 3-0. CBD34: 15-0. CBD38: 255-0.

Truth Table:

The truth table is the same for all CBD3s.

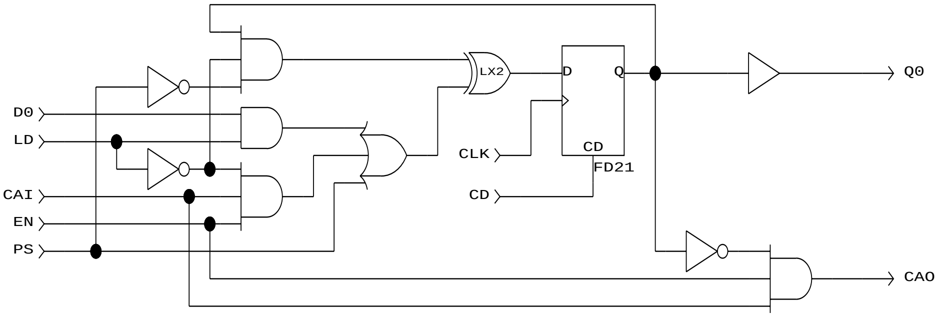
Input							Output	
CD	**PS**	**LD**	**D**	**EN**	**CAI**	**CLK**	**Q**	**CAO**
1	x	x	x	x	x	x	0	CAI·EN
0	1	x	x	x	x	↑	1	0
0	0	1	d	x	x	↑	d	*
0	0	0	x	0	x	x	Q	0
0	0	0	x	x	0	x	Q	0
0	0	0	x	1	1	↑	count down	**

* CBD31: CAO = CAI·EN·$\overline{D0}$
CBD32: CAO = CAI·EN·$\overline{D0}\cdot\overline{D1}$
CBD34: CAO = CAI·EN·$\overline{D0}\cdot\overline{D1}\cdot\overline{D2}\cdot\overline{D3}$
CBD38: CAO = CAI·EN·$\overline{D0}\cdot\overline{D1}\cdot\overline{D2}\cdot\overline{D3}\cdot\overline{D4}\cdot\overline{D5}\cdot\overline{D6}\cdot\overline{D7}$

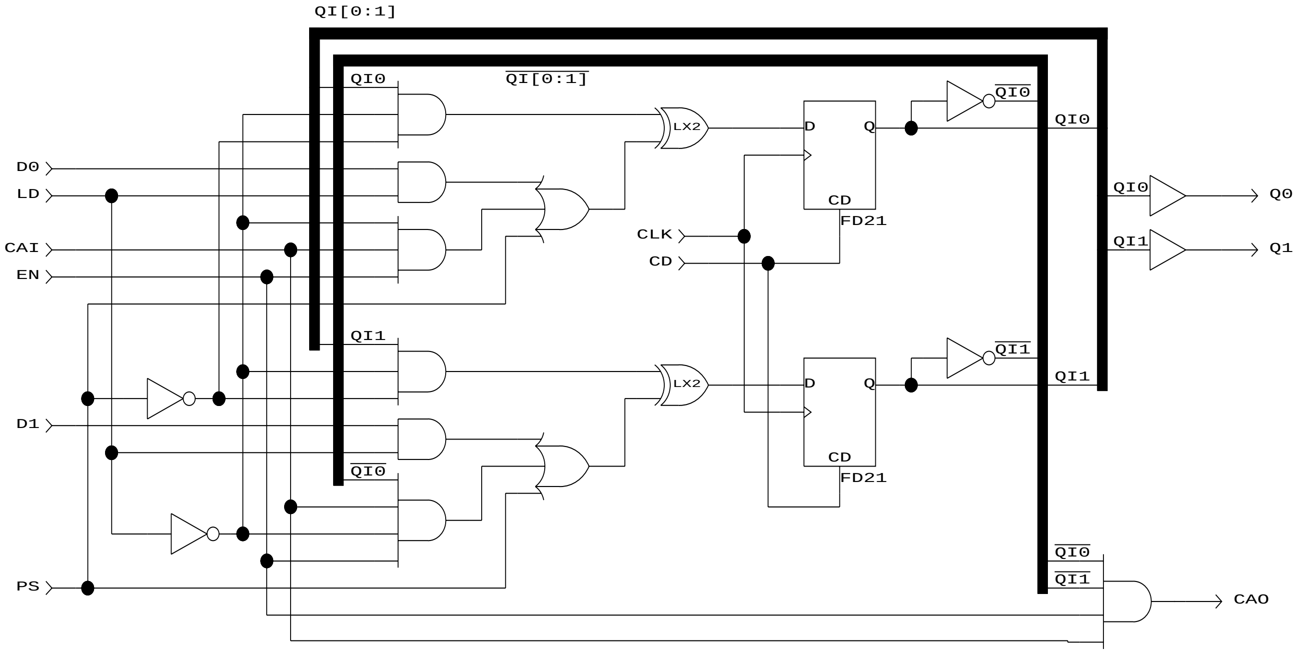
** CAO = 1 after terminal count, when CAI = 1 and EN = 1.

CAI·EN = shift registers: serial input; counters: CAscade In, enable for multiplexors and counters, d = any pattern of 1s and 0s on an input or set of inputs, Q = output of flip-flop or latch, ↑ = rising clock edge.

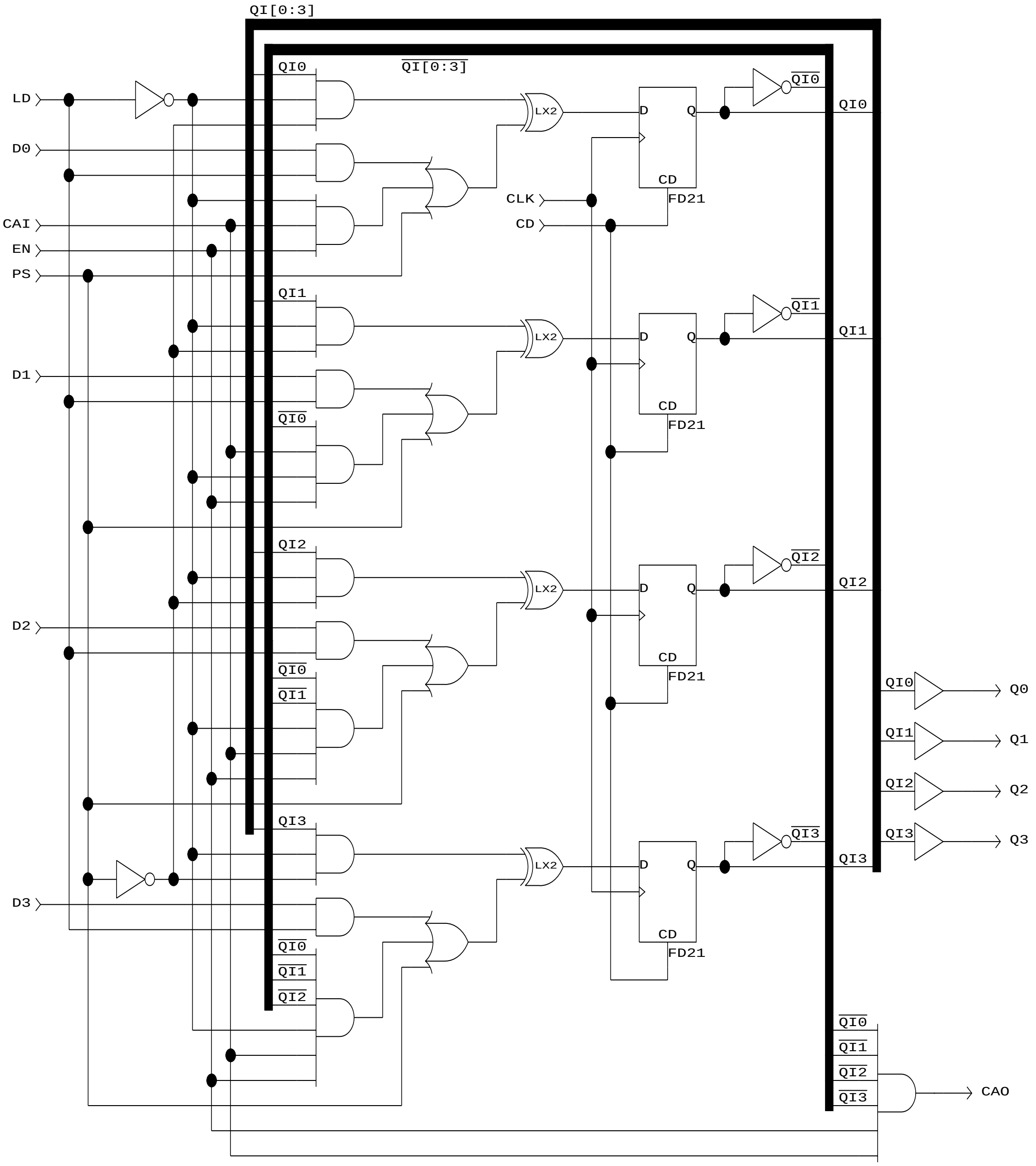
CBD31



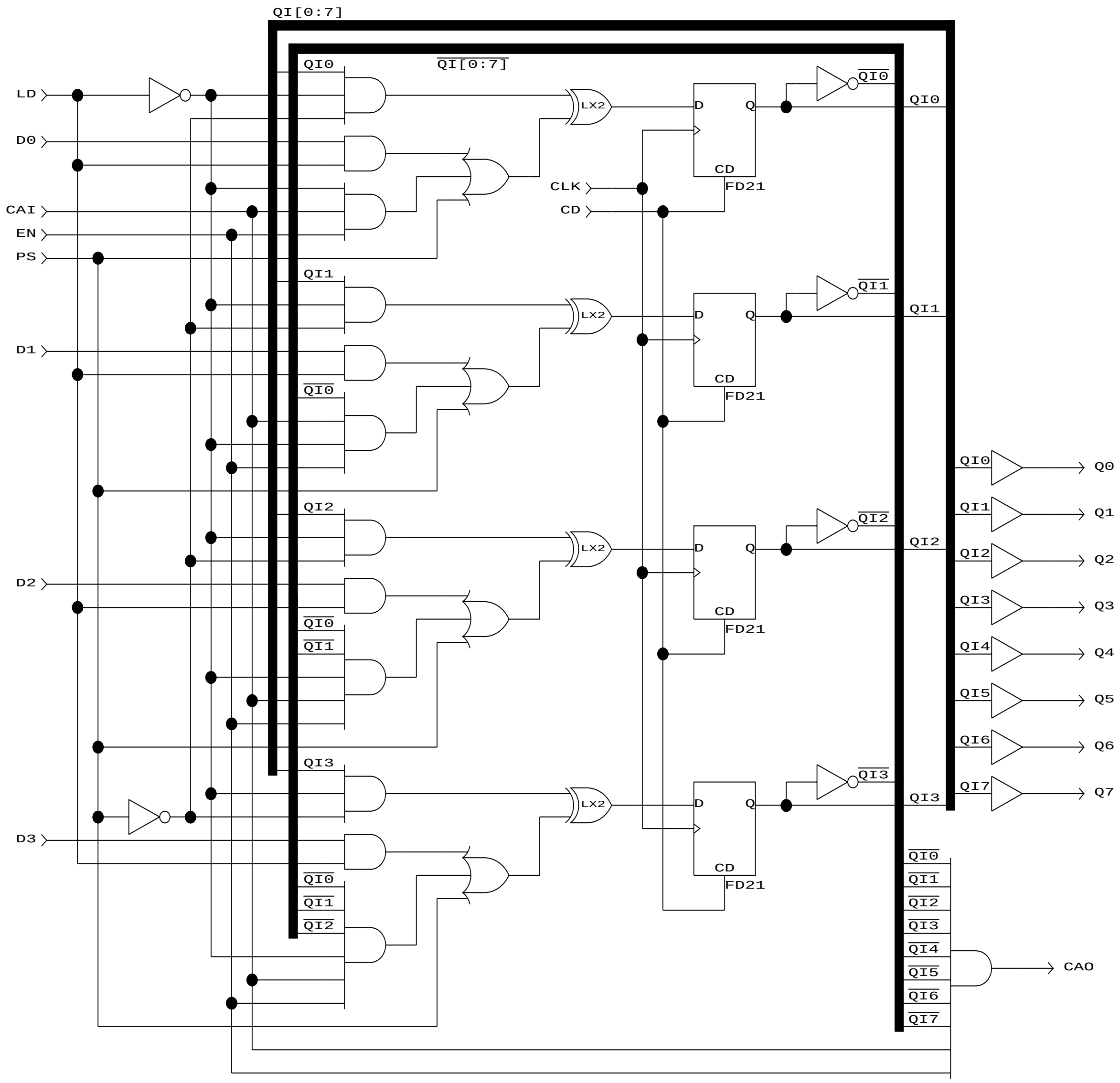
CBD32


QI[0:1]
QI0
$\overline{QI[0:1]}$
LX2
D
Q
CD
FD21
$\overline{QI0}$
QI0
QI0
Q0
QI1
Q1
D0
LD
CAI
EN
CLK
CD
QI1
LX2
D
Q
CD
FD21
$\overline{QI1}$
QI1
D1
$\overline{QI0}$
PS
$\overline{QI0}$
$\overline{QI1}$
CAO

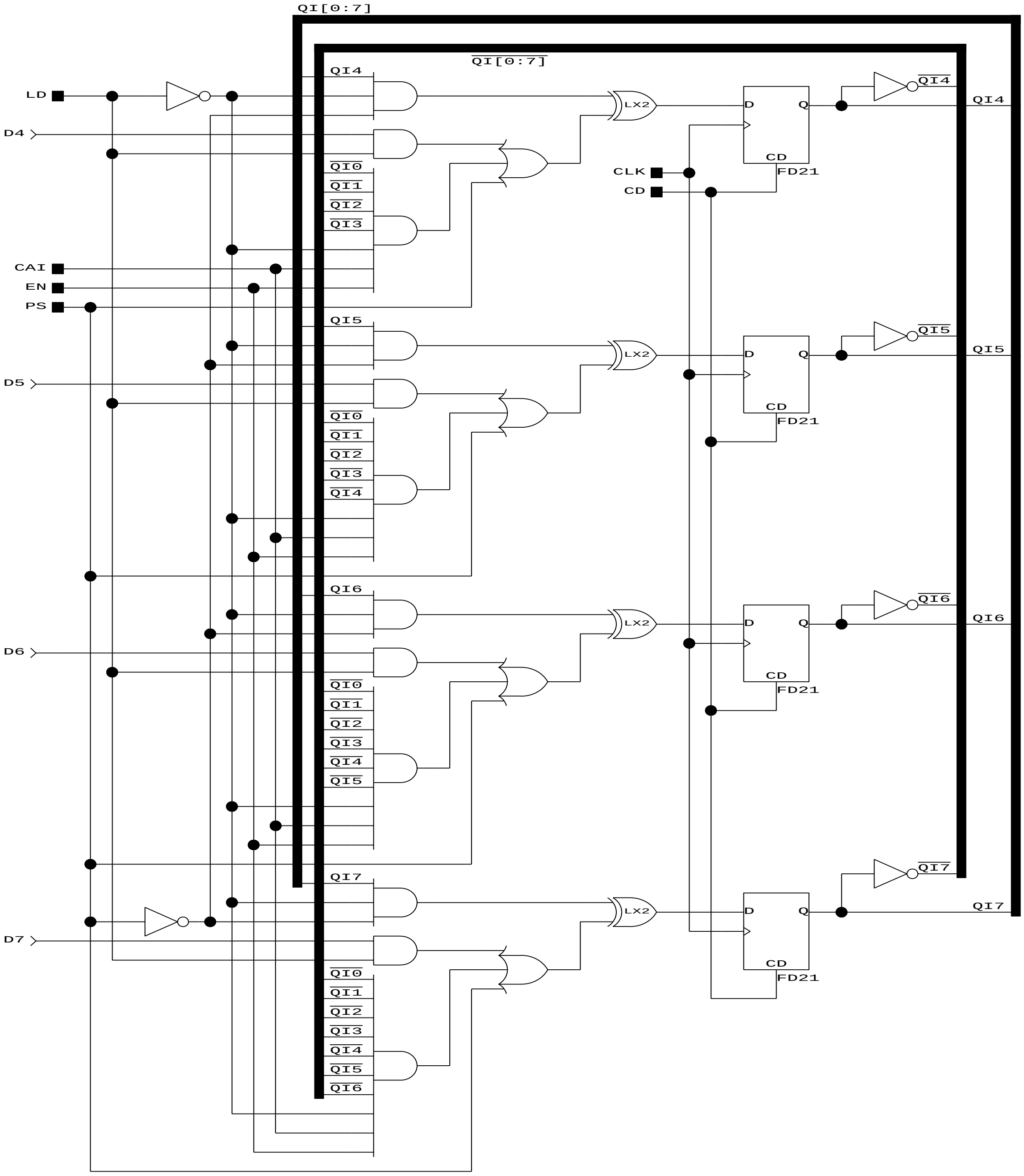
CBD34


QI[0:3]
$\overline{QI[0:3]}$
QI0
LD
D0
CAI
EN
PS
CLK
CD
LX2
D
Q
CD
FD21
$\overline{QI0}$
QI0
QI1
D1
$\overline{QI1}$
QI2
D2
$\overline{QI2}$
QI3
D3
$\overline{QI3}$
Q0
Q1
Q2
Q3
CAO

CBD38.1

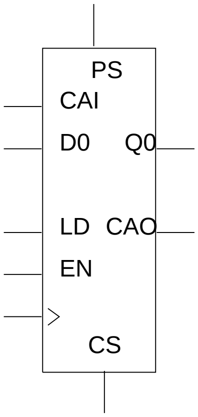

QI[0:7]
QI0
$\overline{QI[0:7]}$
LD
D0
CAI
EN
PS
LX2
D
Q
CD
FD21
CLK
CD
$\overline{QI0}$
QI0
QI1
D1
$\overline{QI0}$
LX2
D
Q
CD
FD21
$\overline{QI1}$
QI1
QI2
D2
$\overline{QI0}$
$\overline{QI1}$
LX2
D
Q
CD
FD21
$\overline{QI2}$
QI2
QI3
D3
$\overline{QI0}$
$\overline{QI1}$
$\overline{QI2}$
LX2
D
Q
CD
FD21
$\overline{QI3}$
QI3
QI0
Q0
QI1
Q1
QI2
Q2
QI3
Q3
QI4
Q4
QI5
Q5
QI6
Q6
QI7
Q7
$\overline{QI0}$
$\overline{QI1}$
$\overline{QI2}$
$\overline{QI3}$
$\overline{QI4}$
$\overline{QI5}$
$\overline{QI6}$
$\overline{QI7}$
CAO

CBD38.2

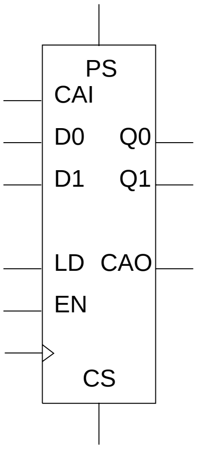

QI[0:7]
$\overline{QI[0:7]}$
LD
D4
D5
D6
D7
CAI
EN
PS
CLK
CD
QI4
QI5
QI6
QI7
$\overline{QI0}$
$\overline{QI1}$
$\overline{QI2}$
$\overline{QI3}$
$\overline{QI4}$
$\overline{QI5}$
$\overline{QI6}$
$\overline{QI7}$
LX2
D
Q
CD
FD21

CBD41, CBD42, CBD44, and CBD48

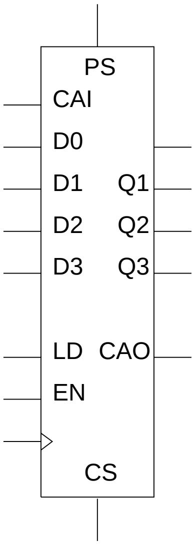
CBD41



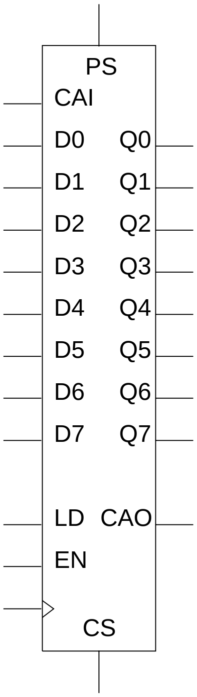
CBD42



CBD44



CBD48



Function:

1-, 2-, 4-, and 8-bit down counters with synchronous clear, enable, parallel data load, synchronous preset, CAI, and CAO.

Availability:

CBD41, CBD42, CBD44, and CBD48 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Schematics appear on the following pages.

Type:

Soft: CBD41 and CBD42.
Hard: CBD44 and CBD48.

Logic Resources:

Macro	PT	GLB	Output	Level
CBD44	*	2	5	1**
CBD48	*	3	9	1**

* Q0-Q_{n-1}: 4 PT per output.
CAO: 1 PT.
CLK: 1 PT per GLB if Product Term Clock is used.
** (CAO is a 2-level output).

Macro Port Definition:

```
CBD41 (Q0,CAO,D0,CAI,CLK,PS,LD,EN,CS);
CBD42 (Q0,Q1,CAO,D0,D1,CAI,CLK,PS,LD,EN,CS);
CBD44 ([Q0..Q3],CAO,[D0..D3],CAI,CLK,PS,LD,EN,CS);
  CBD44_1 ([Q0..Q3],[D0..D3],CAI,CLK,PS,LD,EN,CS);
  CBD44_2 (CAO,[Q0..Q3],CAI,EN);
CBD48 ([Q0..Q7],CAO,[D0..D7],CAI,CLK,PS,LD,EN,CS);
  CBD48_2 (Q4,Q5,[Q0..Q3],D4,D5,CAI,CLK,PS,LD,EN,CS);
  CBD48_3 (Q6,Q7,[Q0..Q5],D6,D7,CAI,CLK,PS,LD,EN,CS);
  CBD48_4 (CAO,[Q0..Q7],CAI,EN);
```

Counting Ranges:

CBD41: 1-0. CBD42: 3-0. CBD44: 15-0. CBD48: 255-0.

Truth Table:

The truth table is the same for all CBD4s.

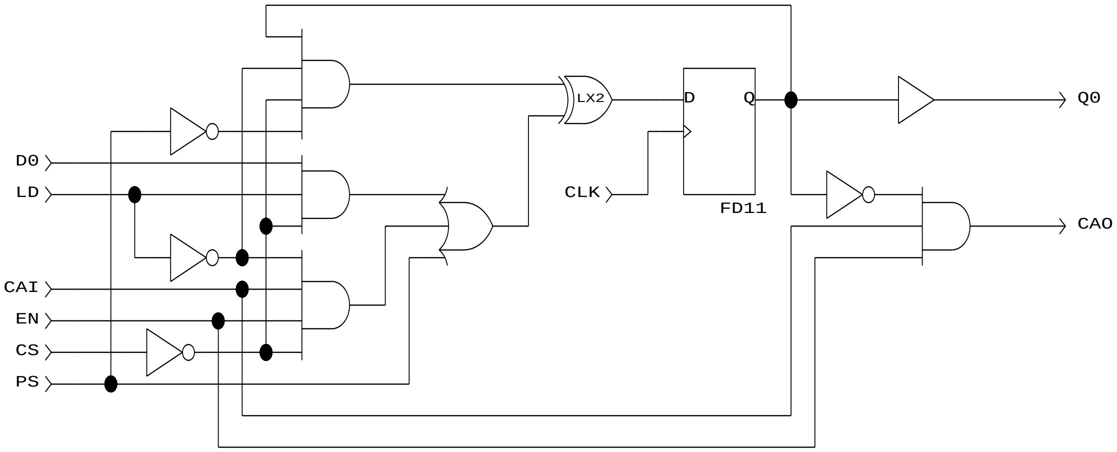
Input							Output	
PS	**CS**	**LD**	**D**	**EN**	**CAI**	**CLK**	**Q**	**CAO**
1	x	x	x	x	x	↑	1	0
0	1	x	x	x	x	↑	0	CAI·EN
0	0	1	d	x	x	↑	d	*
0	0	0	x	0	x	x	Q	0
0	0	0	x	x	0	x	Q	0
0	0	0	x	1	1	↑	count down	**

* CBD41: CAO = $\text{CAI}\cdot\text{EN}\cdot\overline{\text{D0}}$
CBD42: CAO = $\text{CAI}\cdot\text{EN}\cdot\overline{\text{D0}}\cdot\overline{\text{D1}}$
CBD44: CAO = $\text{CAI}\cdot\text{EN}\cdot\overline{\text{D0}}\cdot\overline{\text{D1}}\cdot\overline{\text{D2}}\cdot\overline{\text{D3}}$
CBD48: CAO = $\text{CAI}\cdot\text{EN}\cdot\overline{\text{D0}}\cdot\overline{\text{D1}}\cdot\overline{\text{D2}}\cdot\overline{\text{D3}}\cdot\overline{\text{D4}}\cdot\overline{\text{D5}}\cdot\overline{\text{D6}}\cdot\overline{\text{D7}}$

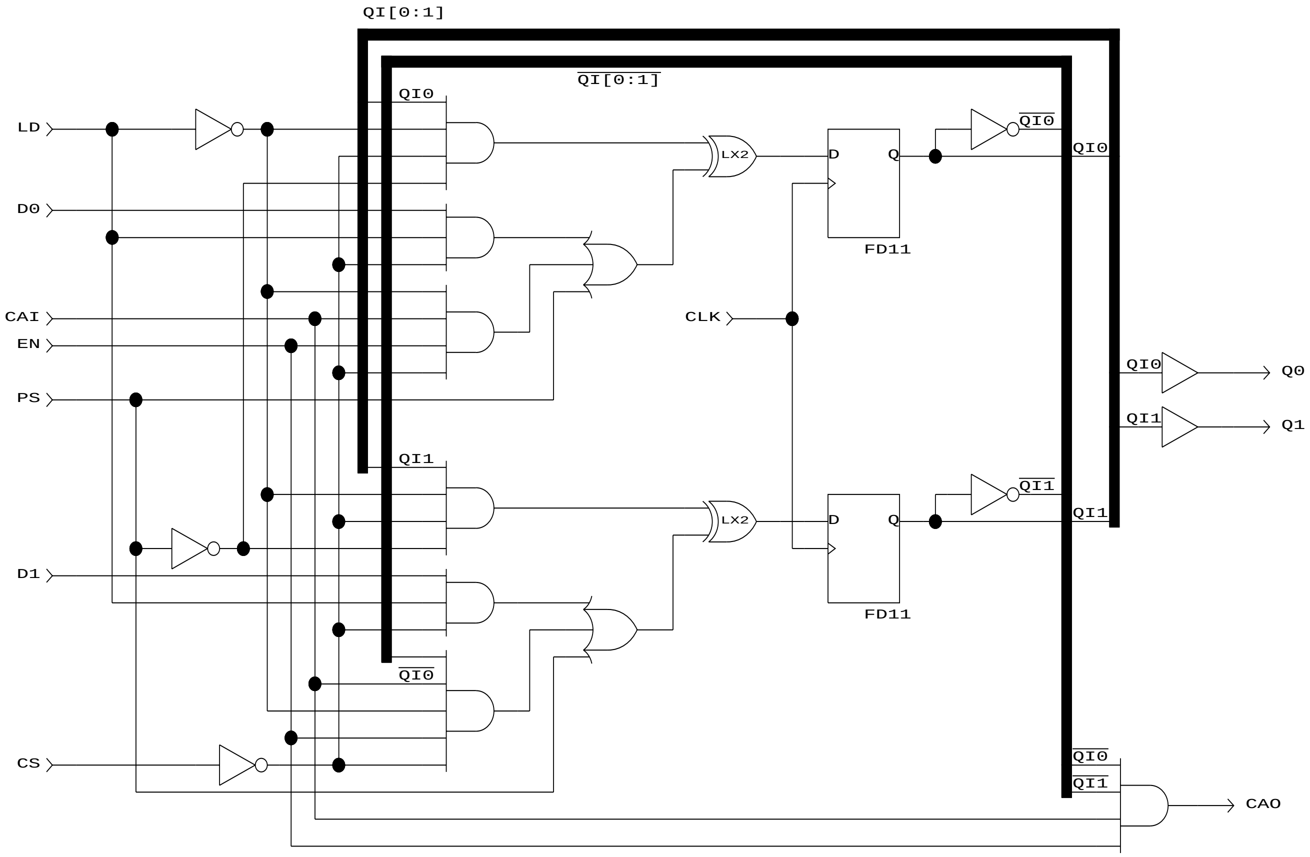
** CAO = 1 after terminal count, when CAI = 1 and EN = 1.

CAI·EN = shift registers: serial input; counters: CAscade In, enable for multiplexors and counters, d = any pattern of 1s and 0s on an input or set of inputs, Q = output of flip-flop or latch, ↑= rising clock edge.

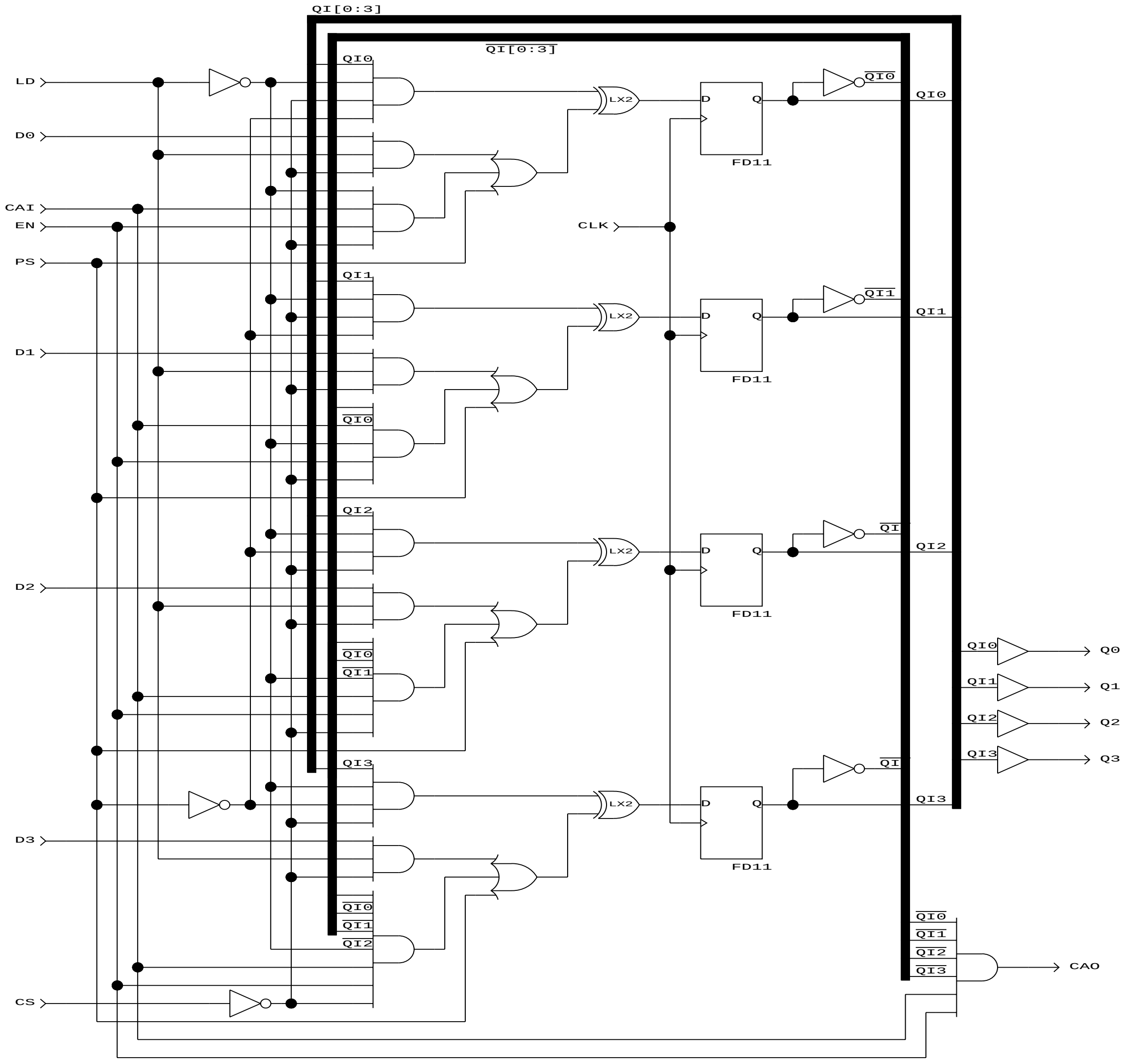
CBD41



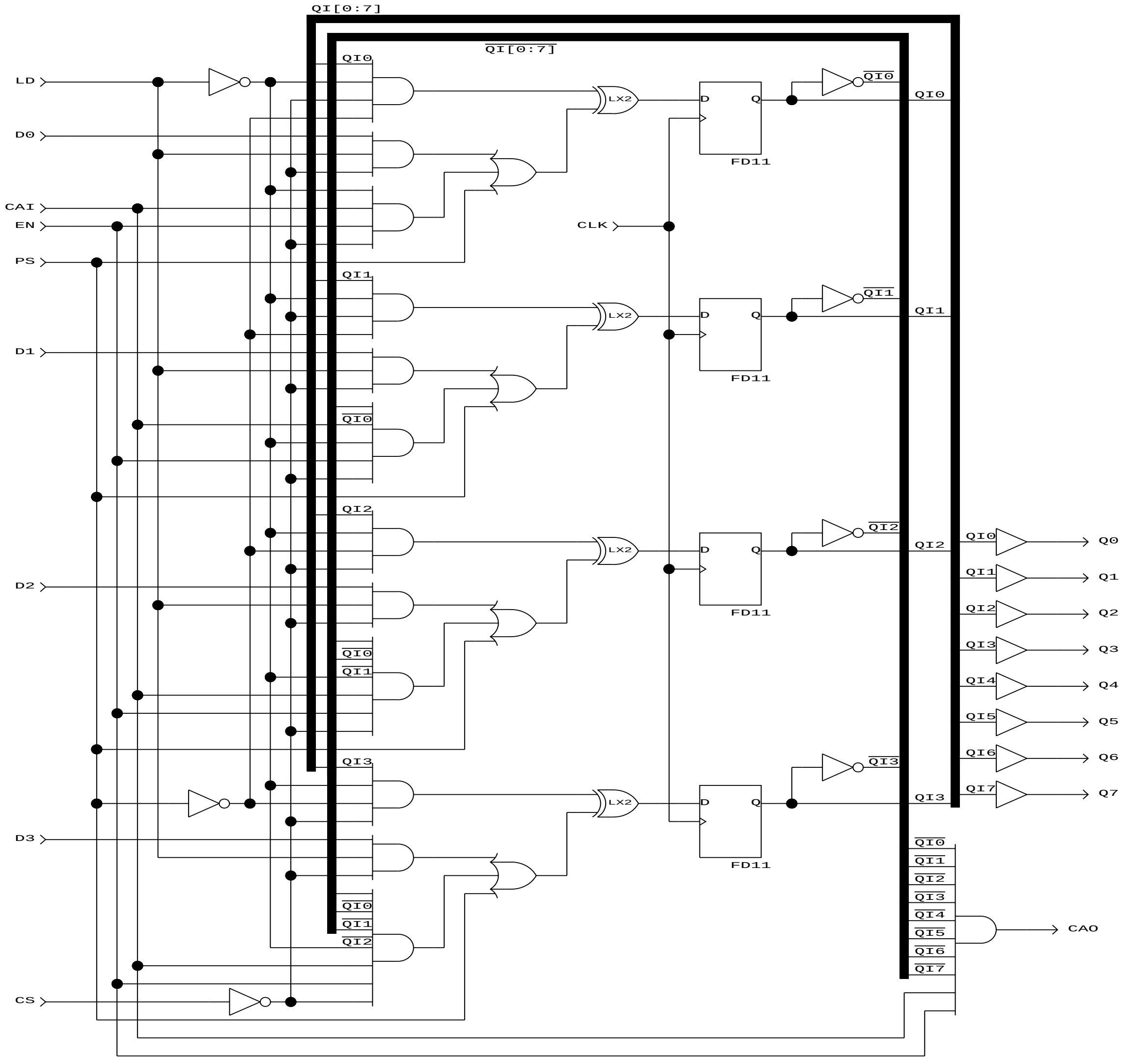
CBD42


QI[0:1]
$\overline{QI[0:1]}$
QI0
LD
D0
CAI
EN
PS
LX2
D
Q
FD11
$\overline{QI0}$
QI0
CLK
QI0
Q0
QI1
Q1
QI1
D1
$\overline{QI0}$
CS
LX2
D
Q
FD11
$\overline{QI1}$
QI1
$\overline{QI0}$
$\overline{QI1}$
CAO

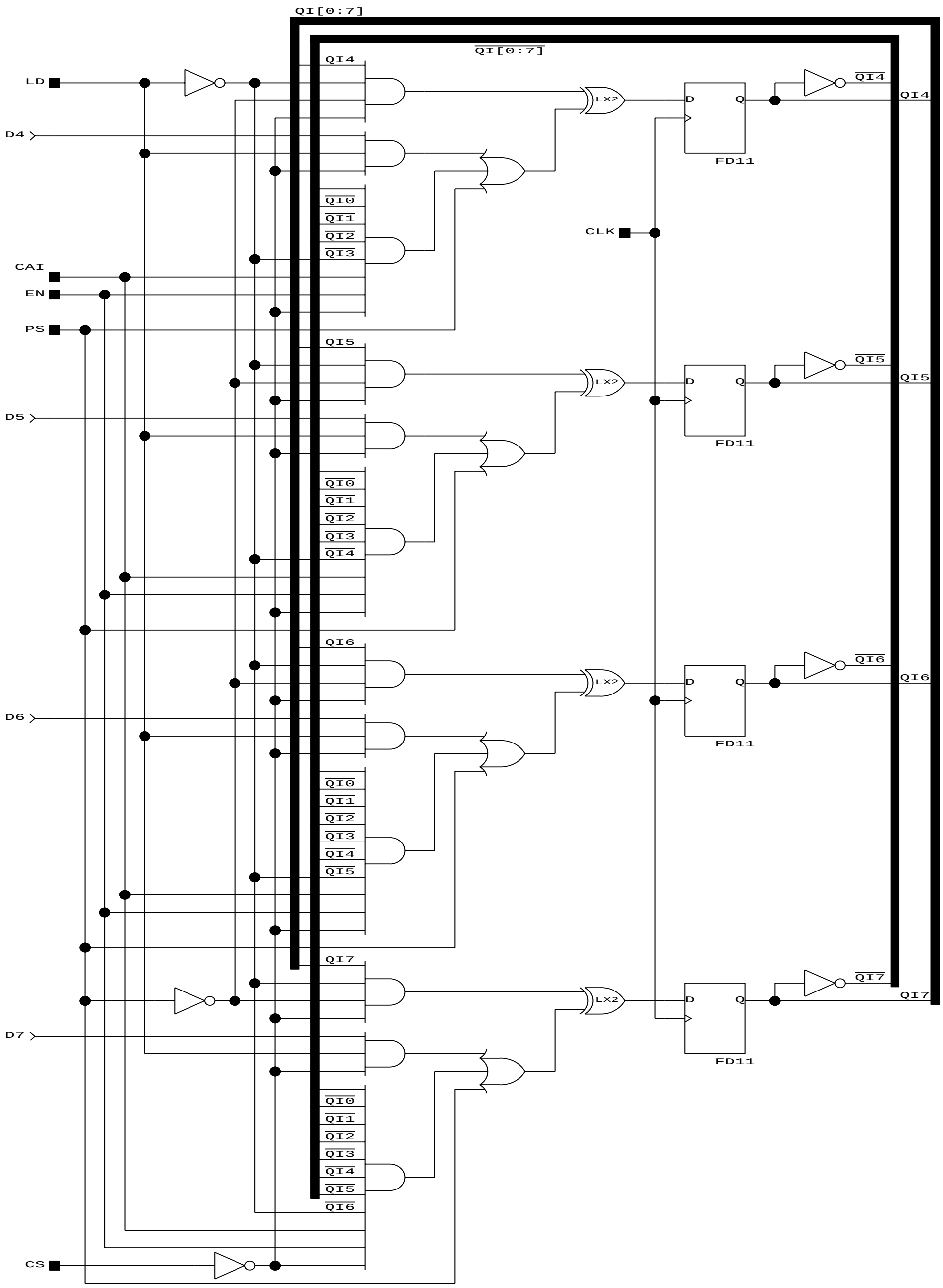
CBD44


QI[0:3]
$\overline{QI[0:3]}$
QI0
LD
D0
CAI
EN
PS
D1
D2
D3
CS
QI1
$\overline{QI0}$
QI2
$\overline{QI1}$
QI3
$\overline{QI2}$
LX2
D
Q
FD11
CLK
$\overline{QI0}$
$\overline{QI1}$
$\overline{QI}$
QI0
QI1
QI2
QI3
Q0
Q1
Q2
Q3
$\overline{QI3}$
CAO

CBD48.1

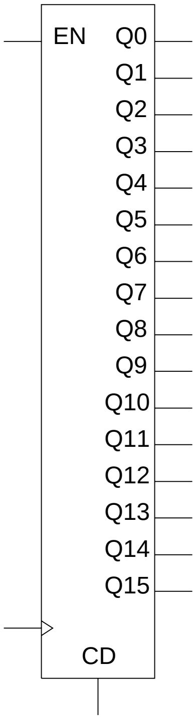

QI[0:7]
$\overline{QI[0:7]}$
LD
D0
CAI
EN
PS
D1
D2
D3
CS
CLK
QI0
QI1
QI2
QI3
$\overline{QI0}$
$\overline{QI1}$
$\overline{QI2}$
$\overline{QI3}$
LX2
D
Q
FD11
QI0
QI1
QI2
QI3
QI4
QI5
QI6
QI7
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
$\overline{QI0}$
$\overline{QI1}$
$\overline{QI2}$
$\overline{QI3}$
$\overline{QI4}$
$\overline{QI5}$
$\overline{QI6}$
$\overline{QI7}$
CA0

CBD48.2

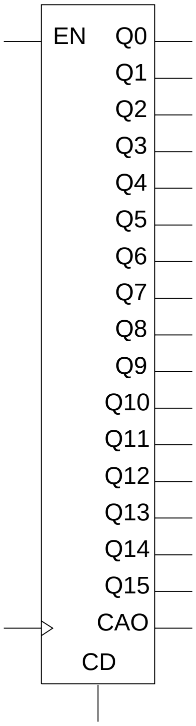

QI[0:7]
$\overline{QI[0:7]}$
LD
D4
CAI
EN
PS
D5
D6
D7
CS
CLK
QI4
QI5
QI6
QI7
$\overline{QI0}$
$\overline{QI1}$
$\overline{QI2}$
$\overline{QI3}$
$\overline{QI4}$
$\overline{QI5}$
QI6
LX2
D
Q
FD11
$\overline{QI4}$
QI4
$\overline{QI5}$
QI5
$\overline{QI6}$
QI6
$\overline{QI7}$
QI7

CBD516 and CBD616

CBD516



CBD616



Function:

16-bit down counters with asynchronous clear and enable. CBD616 also has CAO.

Availability:

CBD516 and CBD616 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Schematics appear on the following pages.

Type: Hard

Logic Resources:

Macro	PT	GLB	Output	Level
CBD516	*	4	16	1
CBD616	**	5	18	2***

* Q0-Q_{n-1}: 2 PT per output.
CLK: 1 PT per GLB if Product Term Clock is used.
CD: 1 PT per GLB.

** Q0-Q_{n-1}: 2 PT per output.
CAO: 1 PT.
CLK: 1 PT per GLB if Product Term Clock is used.
CD: 1 PT per GLB.

*** (CAO is a 2-level output).

Macro Port Definition:

```
CBD516 ([Q0..Q15],CLK,EN,CD);
  CBD516_1 ([Q0..Q3],CLK,EN,CD);
  CBD516_2 ([Q4..Q7],[Q0..Q3],CLK,EN,CD);
  CBD516_3 ([Q8..Q11],[Q0..Q7],CLK,EN,CD);
  CBD516_4 ([Q12..Q15],[Q0..Q11],CLK,EN,CD);
CBD616 ([Q0..Q15],CAO,CLK,EN,CD);
  CBD616_1 ([Q0..Q3],CLK,EN,CD);
  CBD616_2 ([Q4..Q7],[Q0..Q3],CLK,EN,CD);
  CBD616_3 ([Q8..Q11],[Q0..Q7],CLK,EN,CD);
  CBD616_4 (Q12,Q13,[Q0..Q11],CLK,EN,CD);
  CBD616_5 (Q14,Q15,CAO,[Q0..Q13],CLK,EN,CD);
```

Counting Ranges:

CBD516: 65,535-0. CBD616: 65,535-0.

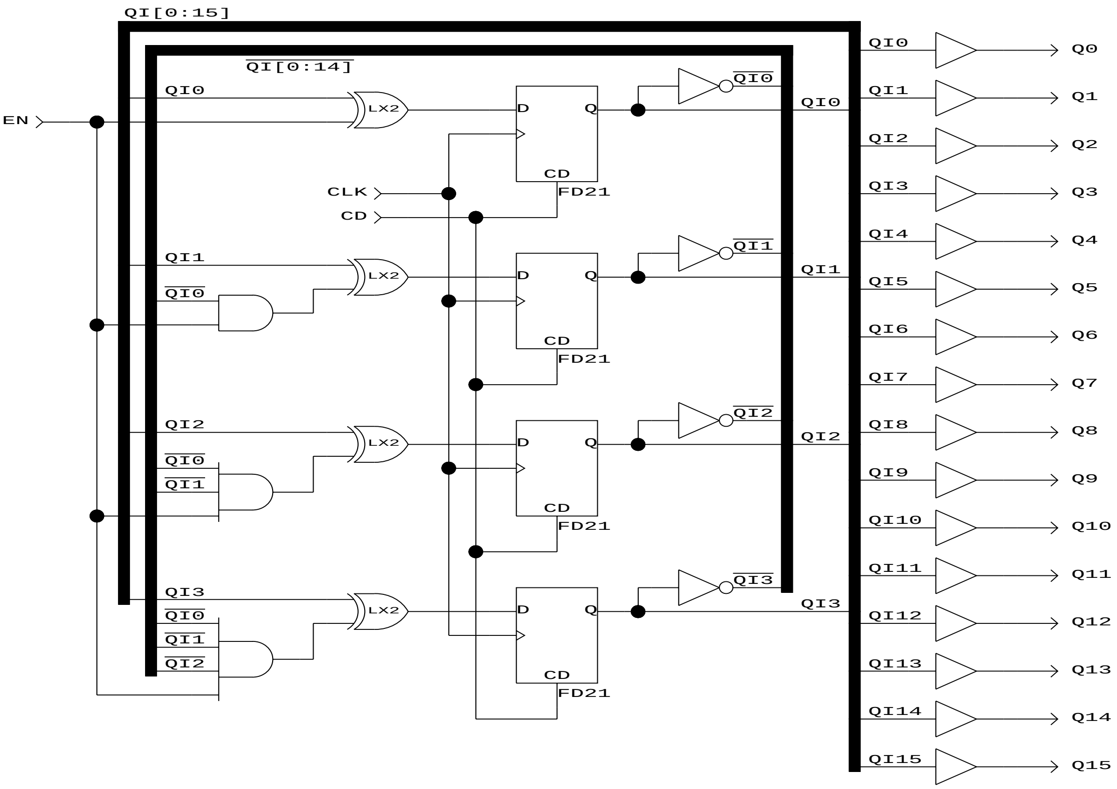
Truth Table:

Gray areas (CAO) apply only to the CBD616.

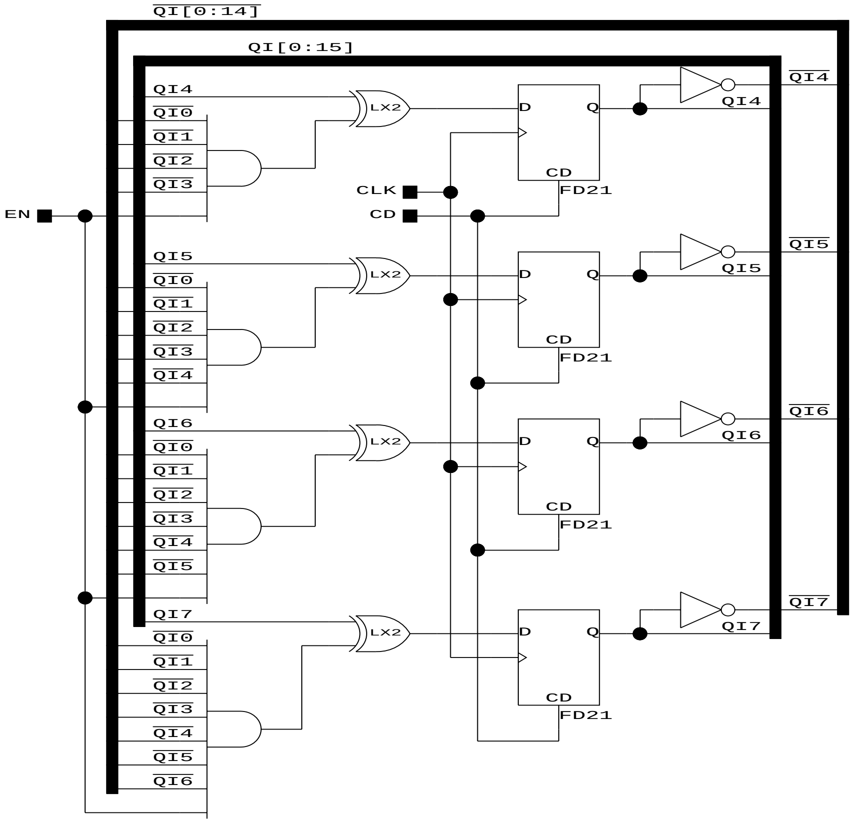
Input			Output	
CD	**EN**	**CLK**	**Q**	**CAO**
1	x	x	0	EN
0	0	x	Q	0
0	1	↑	count down	*

* CAO = 1 after terminal count, when EN = 1 and terminal count = 0.
EN = enable for multiplexors and counters,
Q = output of flip-flop or latch, x = don't care,
↑ = rising clock edge.

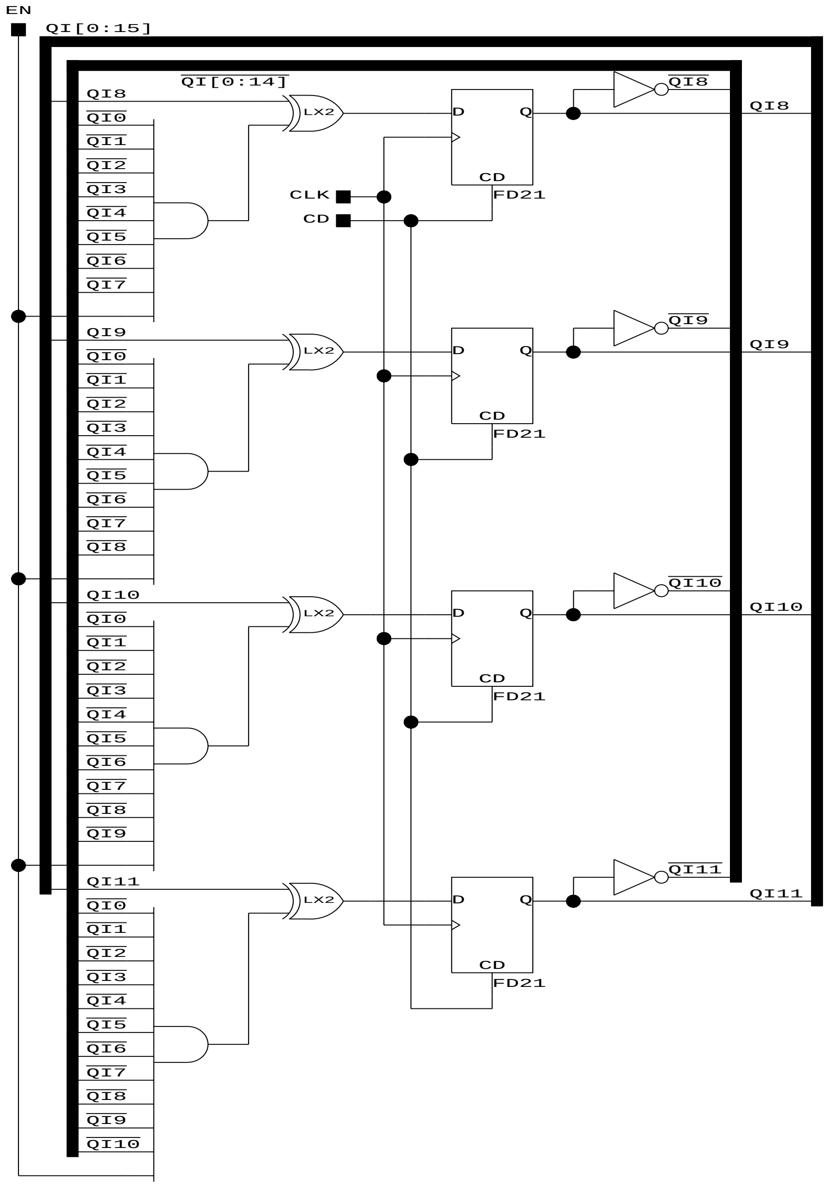
CBD516.1


QI[0:15]
QI[0:14]
EN
QI0
QI1
QI2
QI3
QI0
QI1
QI2
LX2
D
Q
CD
FD21
CLK
CD
QI0
QI1
QI2
QI3
QI0
QI1
QI2
QI3
QI0
QI1
QI2
QI3
QI4
QI5
QI6
QI7
QI8
QI9
QI10
QI11
QI12
QI13
QI14
QI15
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15

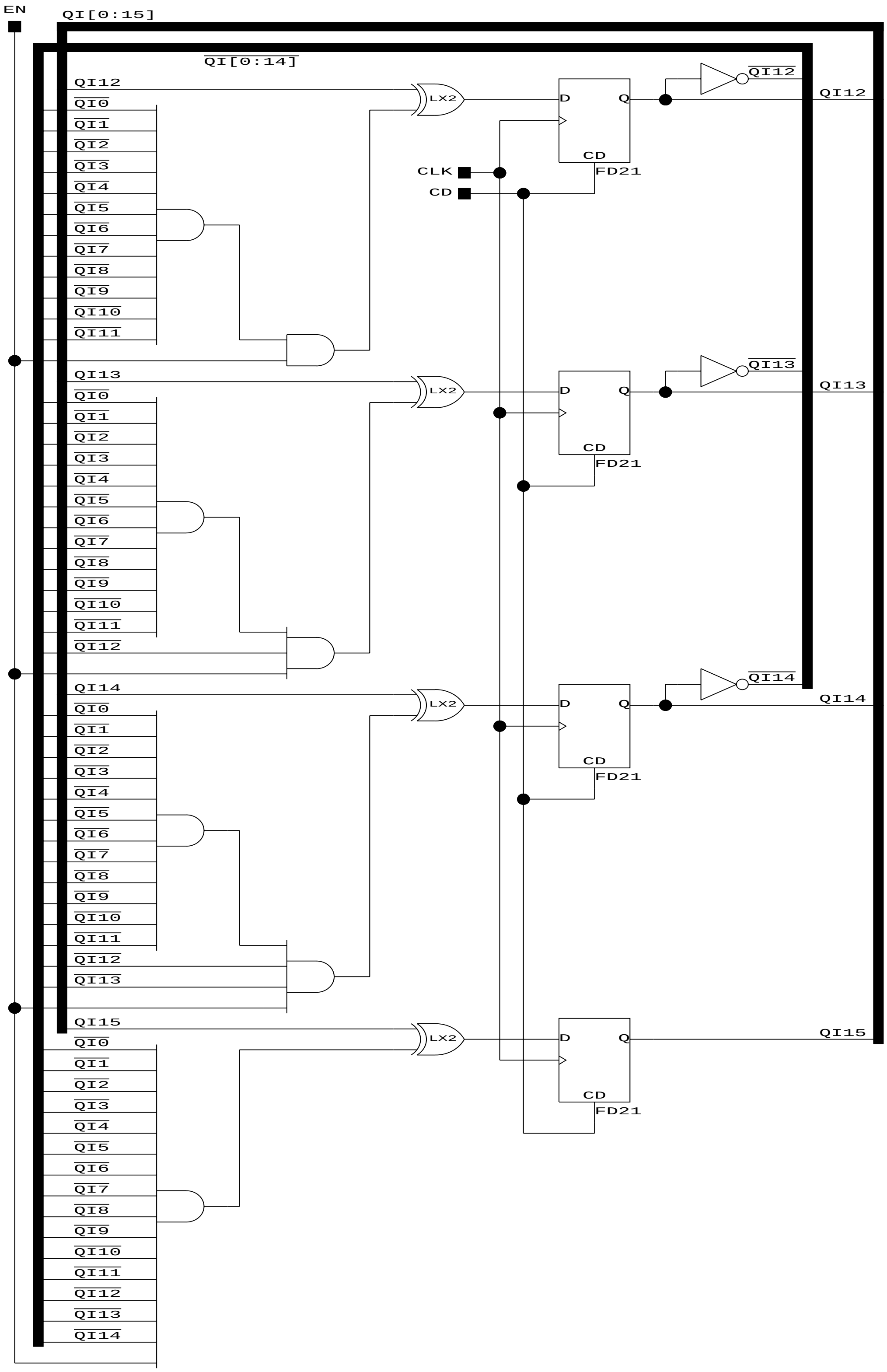
CBD516.2


$\overline{QI[0:14]}$
QI[0:15]
QI4
$\overline{QI0}$
$\overline{QI1}$
$\overline{QI2}$
$\overline{QI3}$
LX2
D
Q
CD
FD21
CLK
CD
EN
$\overline{QI4}$
QI4
QI5
$\overline{QI0}$
$\overline{QI1}$
$\overline{QI2}$
$\overline{QI3}$
$\overline{QI4}$
LX2
D
Q
CD
FD21
$\overline{QI5}$
QI5
QI6
$\overline{QI0}$
$\overline{QI1}$
$\overline{QI2}$
$\overline{QI3}$
$\overline{QI4}$
$\overline{QI5}$
LX2
D
Q
CD
FD21
$\overline{QI6}$
QI6
QI7
$\overline{QI0}$
$\overline{QI1}$
$\overline{QI2}$
$\overline{QI3}$
$\overline{QI4}$
$\overline{QI5}$
$\overline{QI6}$
LX2
D
Q
CD
FD21
$\overline{QI7}$
QI7

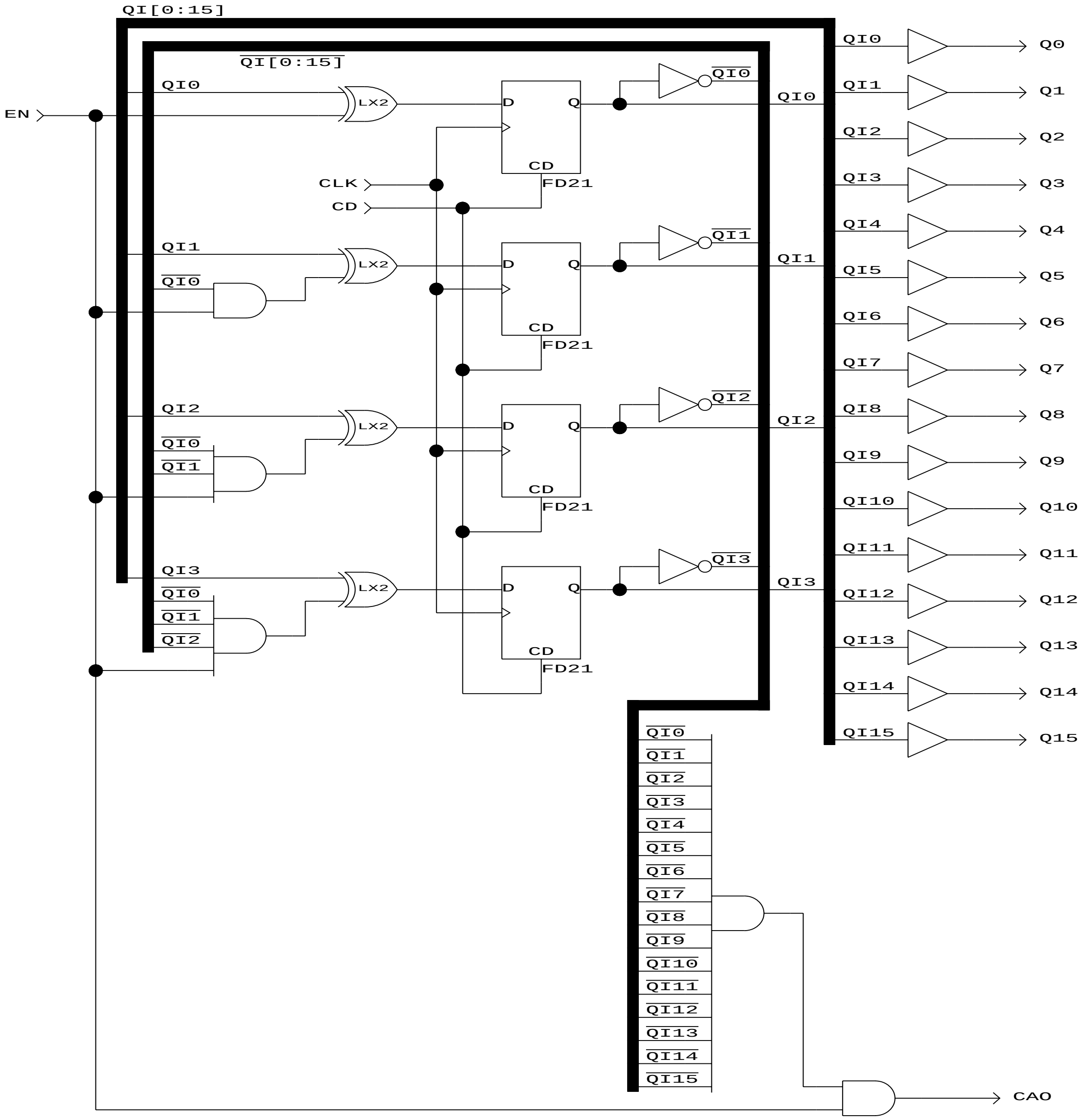
CBD516.3


EN
QI[0:15]
$\overline{\text{QI[0:14]}}$
QI8
QI9
QI10
QI11
$\overline{\text{QI0}}$
$\overline{\text{QI1}}$
$\overline{\text{QI2}}$
$\overline{\text{QI3}}$
$\overline{\text{QI4}}$
$\overline{\text{QI5}}$
$\overline{\text{QI6}}$
$\overline{\text{QI7}}$
$\overline{\text{QI8}}$
$\overline{\text{QI9}}$
$\overline{\text{QI10}}$
$\overline{\text{QI11}}$
LX2
D
Q
CD
FD21
CLK
CD

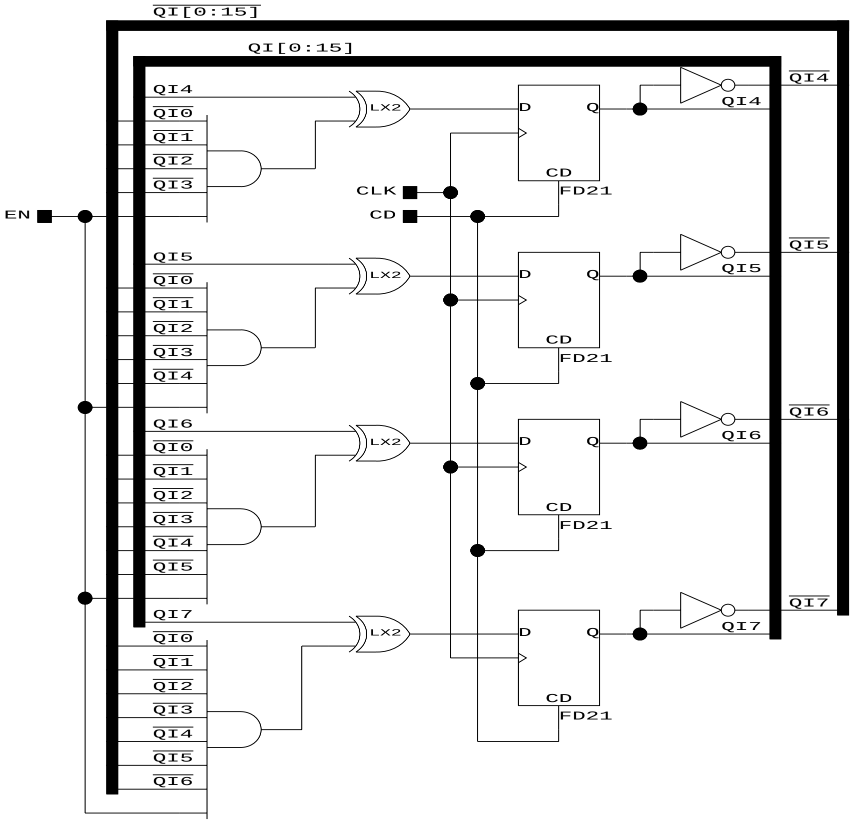
CBD516.4


EN
QI[0:15]
$\overline{QI[0:14]}$
QI12
$\overline{QI0}$
$\overline{QI1}$
$\overline{QI2}$
$\overline{QI3}$
$\overline{QI4}$
$\overline{QI5}$
$\overline{QI6}$
$\overline{QI7}$
$\overline{QI8}$
$\overline{QI9}$
$\overline{QI10}$
$\overline{QI11}$
LX2
D
Q
CD
FD21
CLK
CD
$\overline{QI12}$
QI12
QI13
$\overline{QI12}$
$\overline{QI13}$
QI13
QI14
$\overline{QI13}$
$\overline{QI14}$
QI14
QI15
QI15

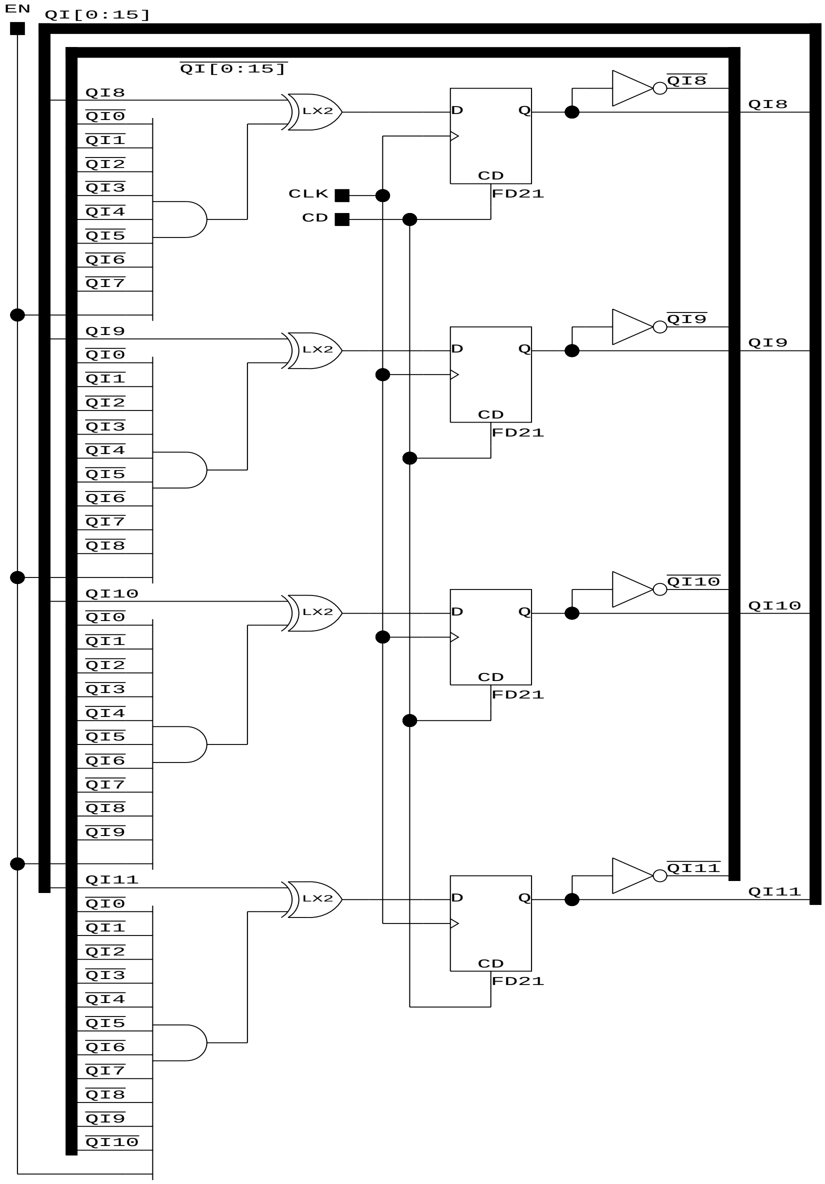
CBD616.1


QI[0:15]
$\overline{QI[0:15]}$
EN
CLK
CD
QI0
QI1
QI2
QI3
$\overline{QI0}$
$\overline{QI1}$
$\overline{QI2}$
$\overline{QI3}$
LX2
D
Q
CD
FD21
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
QI4
QI5
QI6
QI7
QI8
QI9
QI10
QI11
QI12
QI13
QI14
QI15
$\overline{QI4}$
$\overline{QI5}$
$\overline{QI6}$
$\overline{QI7}$
$\overline{QI8}$
$\overline{QI9}$
$\overline{QI10}$
$\overline{QI11}$
$\overline{QI12}$
$\overline{QI13}$
$\overline{QI14}$
$\overline{QI15}$
CAO

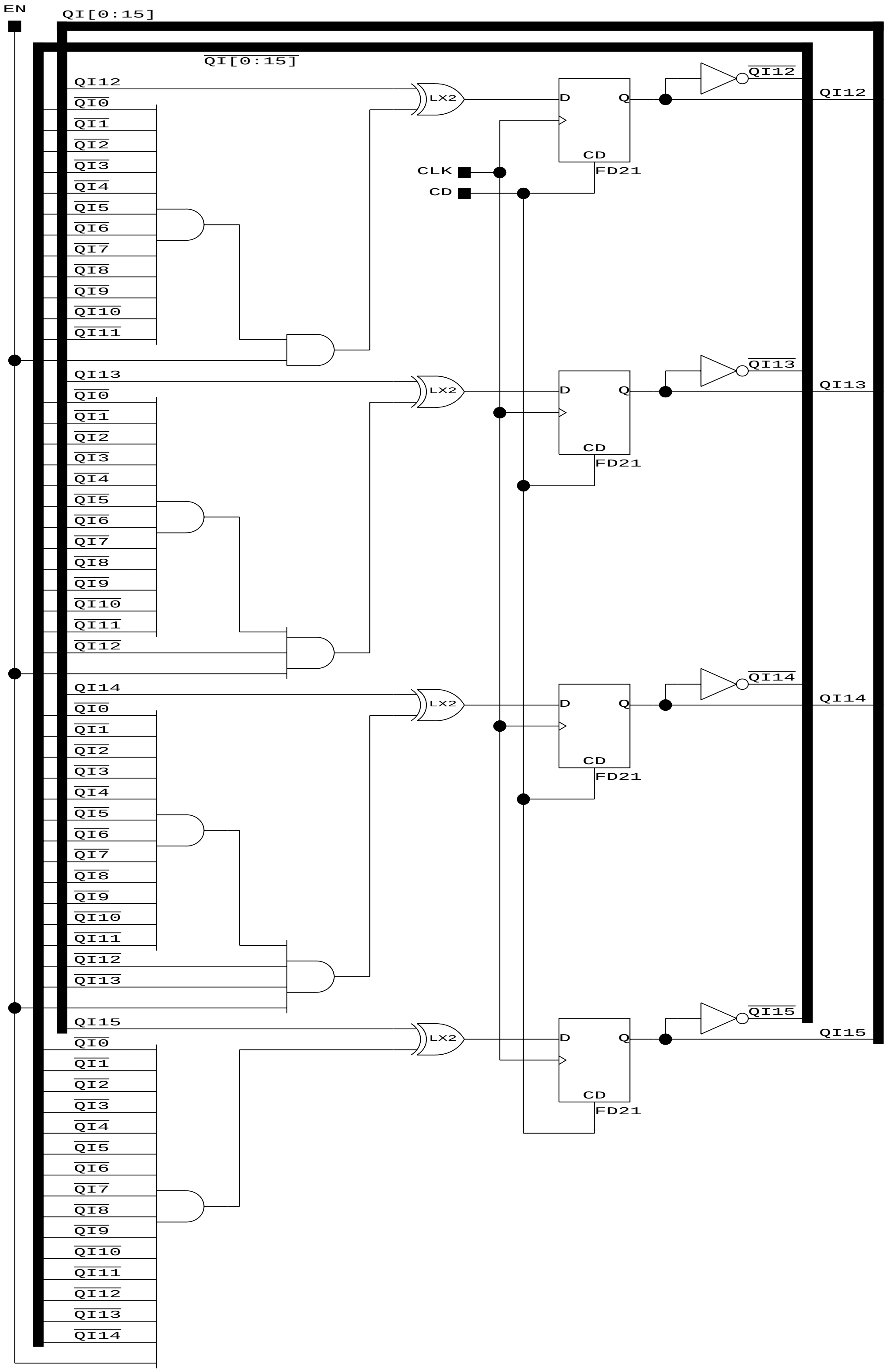
CBD616.2


$\overline{QI[0:15]}$
QI[0:15]
QI4
$\overline{QI0}$
$\overline{QI1}$
$\overline{QI2}$
$\overline{QI3}$
LX2
D
Q
CD
FD21
QI4
$\overline{QI4}$
CLK
CD
EN
QI5
$\overline{QI0}$
$\overline{QI1}$
$\overline{QI2}$
$\overline{QI3}$
$\overline{QI4}$
LX2
D
Q
CD
FD21
QI5
$\overline{QI5}$
QI6
$\overline{QI0}$
$\overline{QI1}$
$\overline{QI2}$
$\overline{QI3}$
$\overline{QI4}$
$\overline{QI5}$
LX2
D
Q
CD
FD21
QI6
$\overline{QI6}$
QI7
$\overline{QI0}$
$\overline{QI1}$
$\overline{QI2}$
$\overline{QI3}$
$\overline{QI4}$
$\overline{QI5}$
$\overline{QI6}$
LX2
D
Q
CD
FD21
QI7
$\overline{QI7}$

CBD616.3


EN
QI[0:15]
$\overline{QI[0:15]}$
QI8
$\overline{QI0}$
$\overline{QI1}$
$\overline{QI2}$
$\overline{QI3}$
$\overline{QI4}$
$\overline{QI5}$
$\overline{QI6}$
$\overline{QI7}$
LX2
D
Q
CD
FD21
CLK
CD
$\overline{QI8}$
QI8
QI9
$\overline{QI8}$
$\overline{QI9}$
QI9
QI10
$\overline{QI9}$
$\overline{QI10}$
QI10
QI11
$\overline{QI10}$
$\overline{QI11}$
QI11

CBD616.4


EN
QI[0:15]
$\overline{QI[0:15]}$
QI12
$\overline{QI0}$
$\overline{QI1}$
$\overline{QI2}$
$\overline{QI3}$
$\overline{QI4}$
$\overline{QI5}$
$\overline{QI6}$
$\overline{QI7}$
$\overline{QI8}$
$\overline{QI9}$
$\overline{QI10}$
$\overline{QI11}$
LX2
D
Q
CD
FD21
CLK
CD
$\overline{QI12}$
QI12
QI13
$\overline{QI0}$
$\overline{QI1}$
$\overline{QI2}$
$\overline{QI3}$
$\overline{QI4}$
$\overline{QI5}$
$\overline{QI6}$
$\overline{QI7}$
$\overline{QI8}$
$\overline{QI9}$
$\overline{QI10}$
$\overline{QI11}$
$\overline{QI12}$
LX2
D
Q
CD
FD21
$\overline{QI13}$
QI13
QI14
$\overline{QI0}$
$\overline{QI1}$
$\overline{QI2}$
$\overline{QI3}$
$\overline{QI4}$
$\overline{QI5}$
$\overline{QI6}$
$\overline{QI7}$
$\overline{QI8}$
$\overline{QI9}$
$\overline{QI10}$
$\overline{QI11}$
$\overline{QI12}$
$\overline{QI13}$
LX2
D
Q
CD
FD21
$\overline{QI14}$
QI14
QI15
$\overline{QI0}$
$\overline{QI1}$
$\overline{QI2}$
$\overline{QI3}$
$\overline{QI4}$
$\overline{QI5}$
$\overline{QI6}$
$\overline{QI7}$
$\overline{QI8}$
$\overline{QI9}$
$\overline{QI10}$
$\overline{QI11}$
$\overline{QI12}$
$\overline{QI13}$
$\overline{QI14}$
LX2
D
Q
CD
FD21
$\overline{QI15}$
QI15

CBU11, CBU12, CBU14, and CBU18

Function:

1-, 2-, 4-, and 8-bit up counters with asynchronous clear, CAI, and CAO.

Availability:

CBU11, CBU12, CBU14, and CBU18 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Schematics appear on the following pages.

Type:

Soft:	CBU11 and CBU12.
Hard:	CBU14 and CBU18.

Logic Resources:

Macro	PT	GLB	Output	Level
CBU14	*	2	5	1**
CBU18	*	3	9	1**

* Q0-Q_{n-1}: 2 PT per output.
CAO: 1 PT.
CLK: 1 PT per GLB if Product Term Clock is used.
CD: 1 PT per GLB.

** (CAO is a 2-level output).

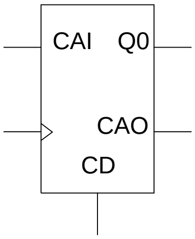
Macro Port Definition:

```
CBU11 (Q0,CAO,CAI,CLK,CD);
CBU12 (Q0,Q1,CAO,CAI,CLK,CD);
CBU14 ([Q0..Q3],CAO,CAI,CLK,CD);
  CBU14_1 ([Q0..Q3],CAI,CLK,CD);
  CBU14_2 (CAO,[Q0..Q3],CAI);
CBU18 ([Q0..Q7],CAO,CAI,CLK,CD);
  CBU18_1 ([Q0..Q3],CAI,CLK,CD);
  CBU18_2 ([Q4..Q7],[Q0..Q3],CAI,CLK,CD);
  CBU18_3 (CAO,[Q0..Q7],CAI);
```

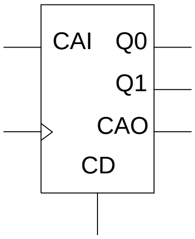
Counting Ranges:

CBU11: 0-1. CBU12: 0-3. CBU14: 0-15. CBU18: 0-255.

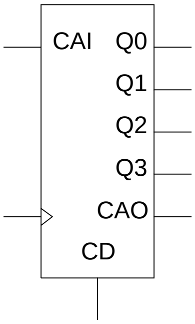
CBU11



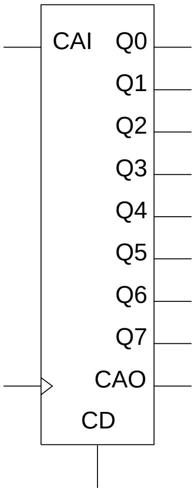
CBU12



CBU14



CBU18



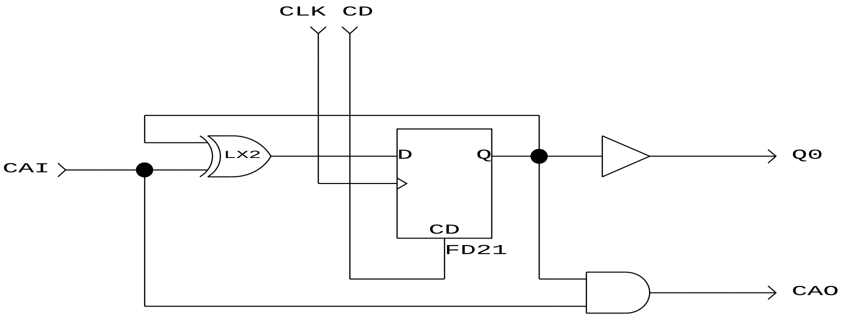
Truth Table:

The truth table is the same for all CBU1s.

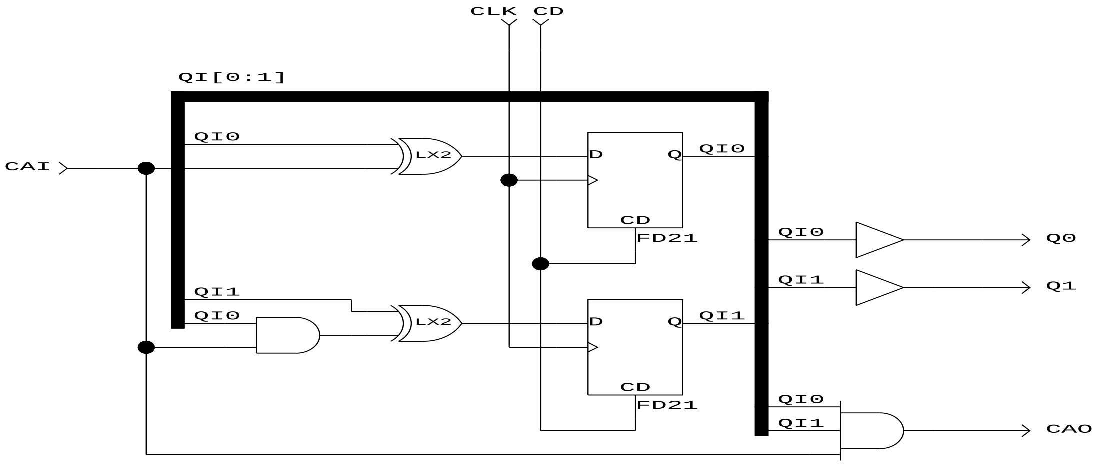
Input			Output	
CD	**CAI**	**CLK**	**Q**	**CAO**
1	x	x	0	0
0	0	x	Q	0
0	1	↑	count up	*

* CAO = 1 after terminal count, when CAI = 1.
Q = output of flip-flop or latch,
x = don't care, ↑ = rising clock edge.

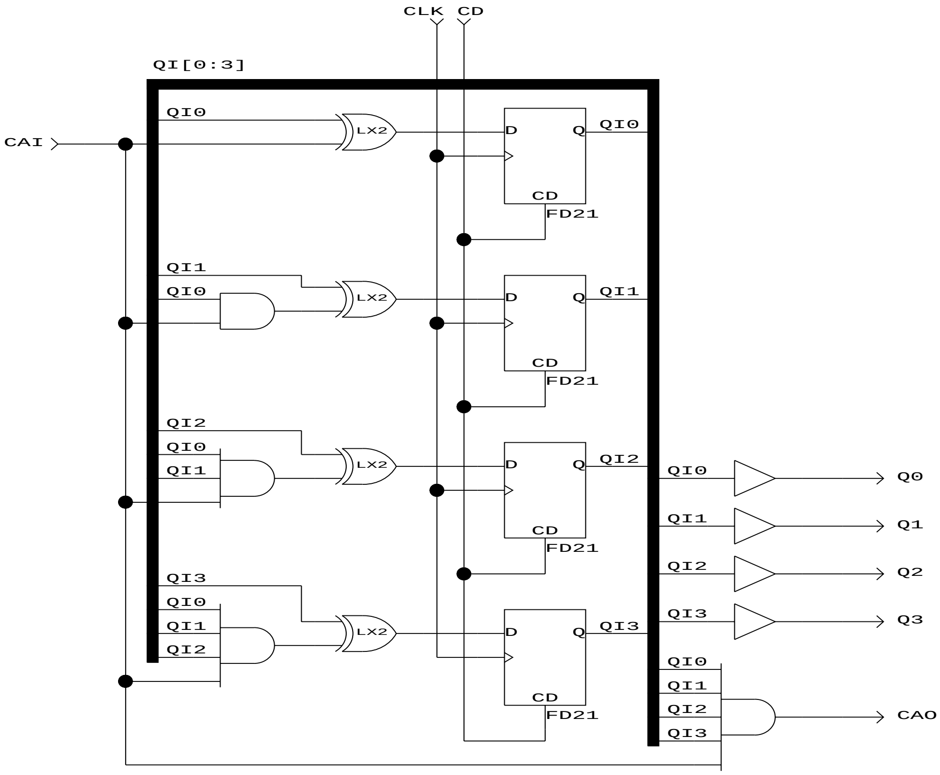
CBU11



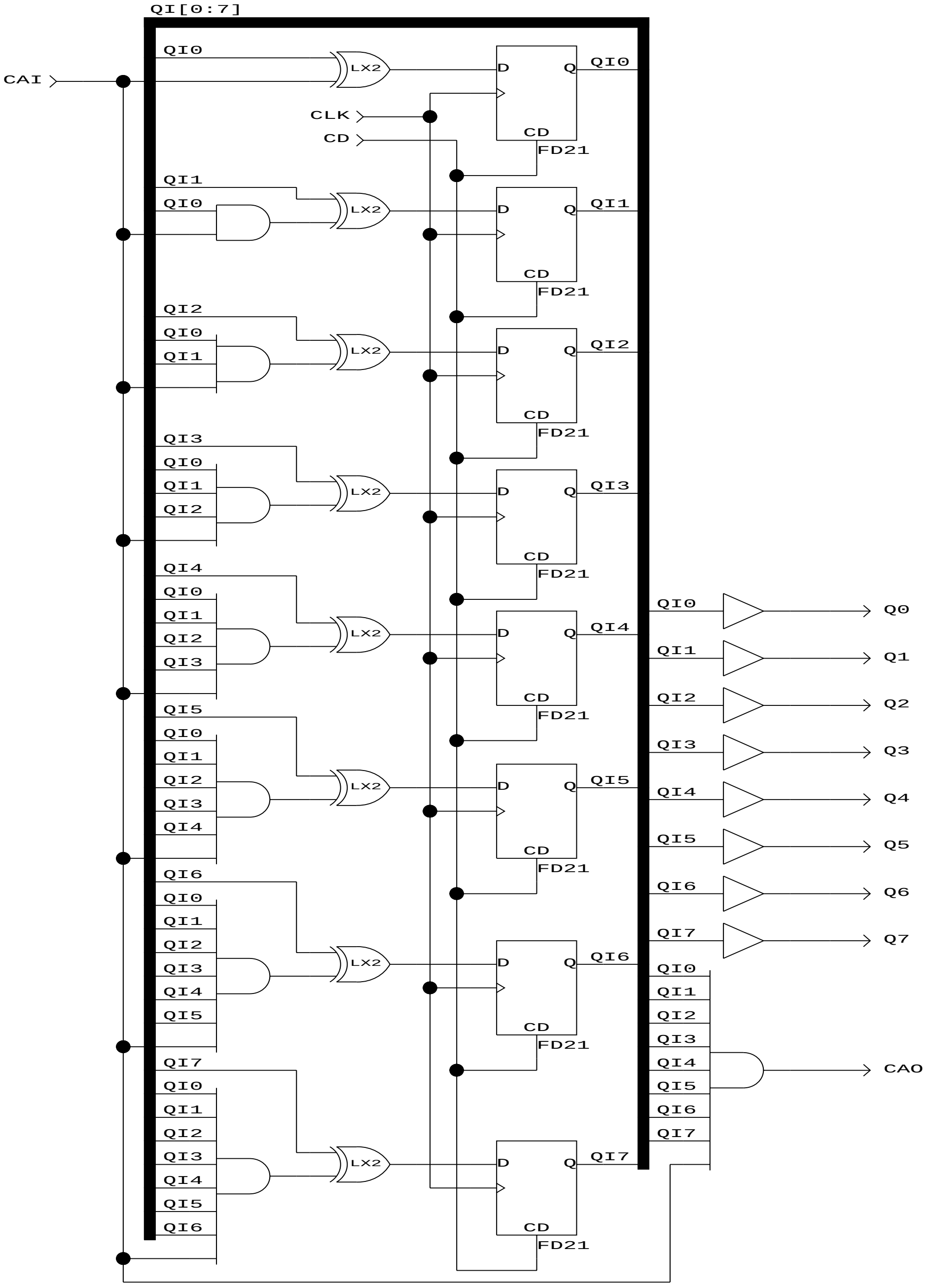
CBU12


CLK
CD
QI[0:1]
QI0
CAI
LX2
D
Q
QI0
CD
FD21
QI0
Q0
QI1
Q1
QI1
QI0
LX2
D
Q
QI1
CD
FD21
QI0
QI1
CAO

CBU14



CBU18


QI[0:7]
CAI
QI0
LX2
D
Q
QI0
CLK
CD
CD
FD21
QI1
QI0
LX2
D
Q
QI1
CD
FD21
QI2
QI0
QI1
LX2
D
Q
QI2
CD
FD21
QI3
QI0
QI1
QI2
LX2
D
Q
QI3
CD
FD21
QI4
QI0
QI1
QI2
QI3
LX2
D
Q
QI4
CD
FD21
QI5
QI0
QI1
QI2
QI3
QI4
LX2
D
Q
QI5
CD
FD21
QI6
QI0
QI1
QI2
QI3
QI4
QI5
LX2
D
Q
QI6
CD
FD21
QI7
QI0
QI1
QI2
QI3
QI4
QI5
QI6
LX2
D
Q
QI7
CD
FD21
QI0
Q0
QI1
Q1
QI2
Q2
QI3
Q3
QI4
Q4
QI5
Q5
QI6
Q6
QI7
Q7
QI0
QI1
QI2
QI3
QI4
QI5
QI6
QI7
CAO

CBU21, CBU22, CBU24, and CBU28

Function:

1-, 2-, 4-, and 8-bit up counters with asynchronous clear, enable, CAI, and CAO.

Availability:

CBU21, CBU22, CBU24, and CBU28 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Schematics appear on the following pages.

Type:

Soft:	CBU21 and CBU22.
Hard:	CBU24 and CBU28.

Logic Resources:

Macro	PT	GLB	Output	Level
CBU24	*	2	5	1**
CBU28	*	3	9	1**

* Q0-Q_{n-1}: 2 PT per output.
CAO: 1 PT.
CLK: 1 PT per GLB if Product Term Clock is used.
CD: 1 PT per GLB.

** (CAO is a 2-level output).

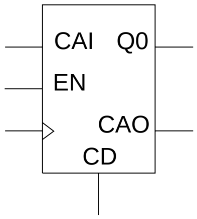
Macro Port Definition:

```
CBU21 (Q0,CAO,CAI,CLK,EN,CD);
CBU22 (Q0,Q1,CAO,CAI,CLK,EN,CD);
CBU24 ([Q0..Q3],CAO,CAI,CLK,EN,CD);
  CBU24_1 ([Q0..Q3],CAI,CLK,EN,CD);
  CBU24_2 (CAO,[Q0..Q3],CAI,EN);
CBU28 ([Q0..Q7],CAO,CAI,CLK,EN,CD);
  CBU28_1 ([Q0..Q3],CAI,CLK,EN,CD);
  CBU28_2 ([Q4..Q7],[Q0..Q3],CAI,CLK,EN,CD);
  CBU28_3 (CAO,[Q0..Q7],CAI,EN);
```

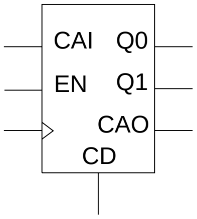
Counting Ranges:

CBU21: 0-1. CBU22: 0-3. CBU24: 0-15. CBU28: 0-255.

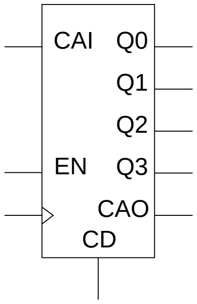
CBU21



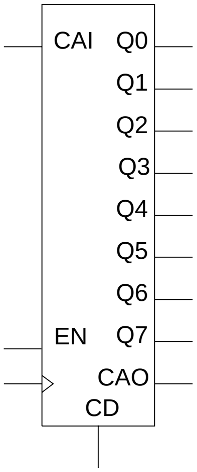
CBU22



CBU24



CBU28



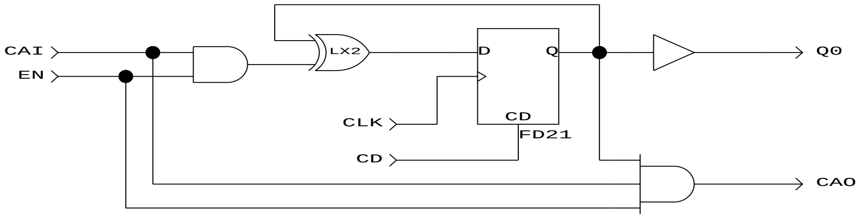
Truth Table:

The truth table is the same for all CBU2s.

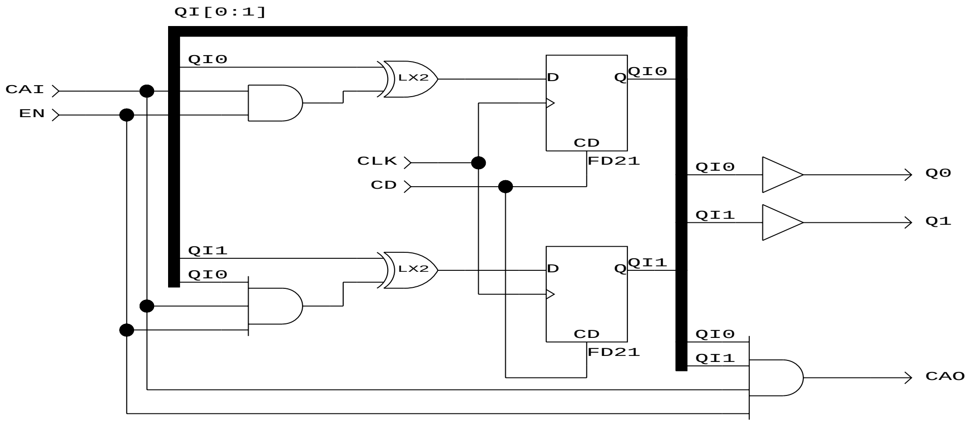
Input				Output	
CD	**EN**	**CAI**	**CLK**	**Q**	**CAO**
1	x	x	x	0	0
0	0	x	x	Q	0
0	x	0	x	Q	0
0	1	1	↑	count up	*

* CAO = 1 after terminal count, when CAI = 1 and EN = 1.
Q = output of flip-flop or latch, x = don’t care,
↑= rising clock edge.

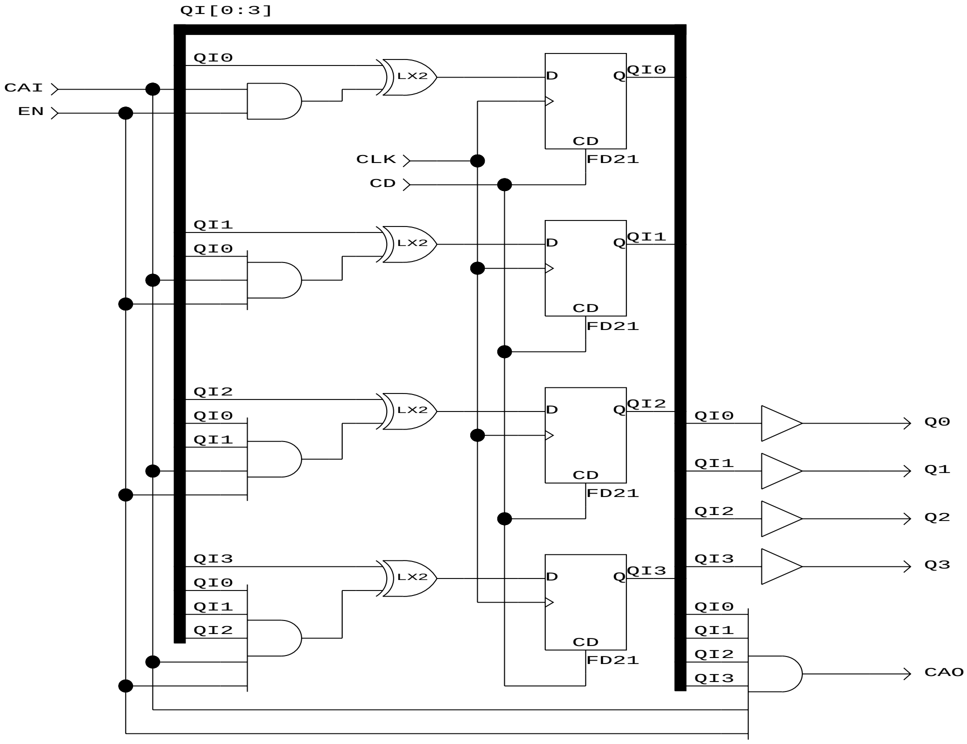
CBU21



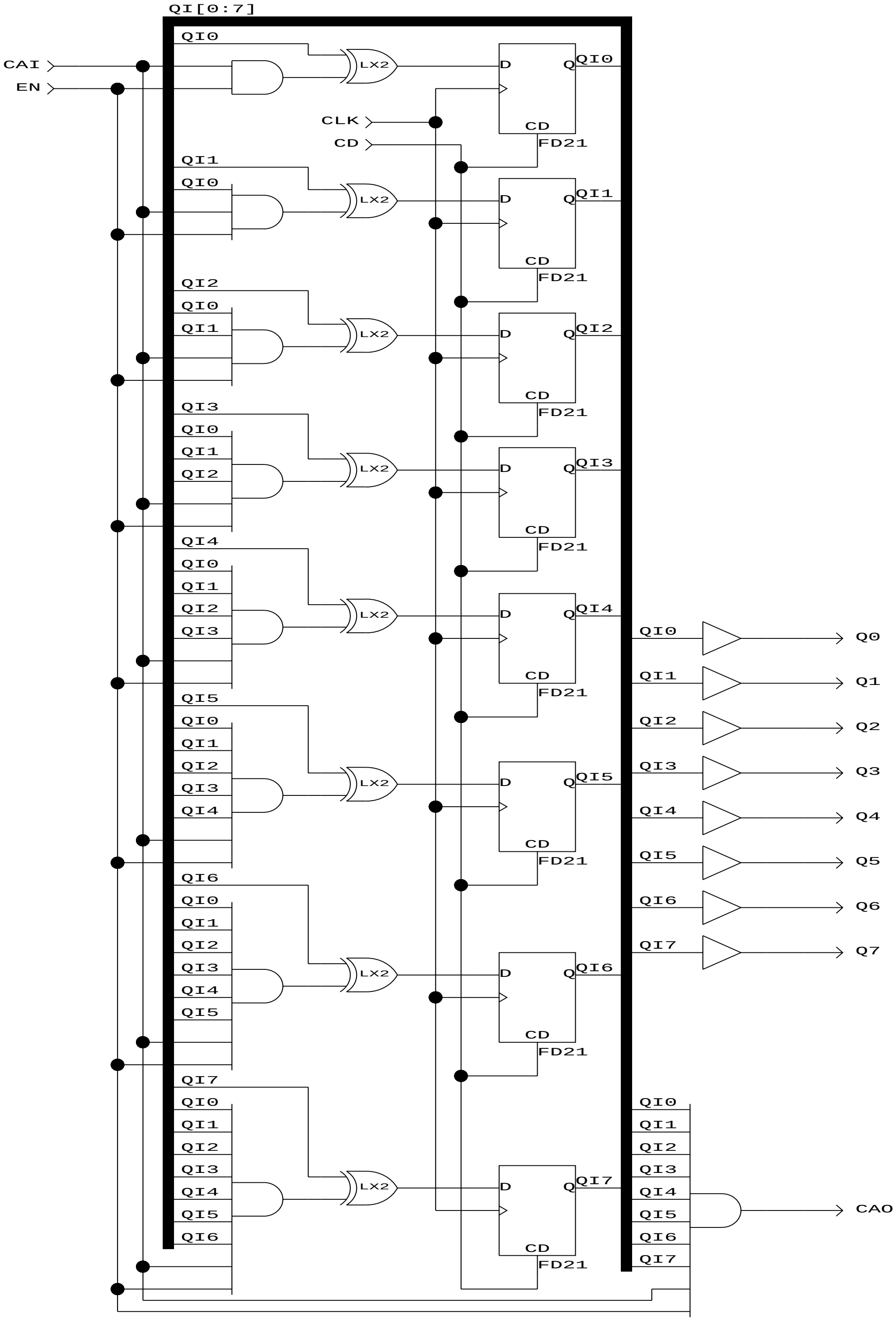
CBU22


QI[0:1]
QI0
CAI
EN
LX2
D
Q
QI0
CD
FD21
CLK
CD
QI0
Q0
QI1
Q1
QI1
QI0
LX2
D
Q
QI1
CD
FD21
QI0
QI1
CAO

CBU24

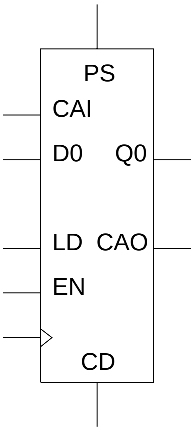

QI[0:3]
QI0
CAI
EN
LX2
D
Q
QI0
CD
FD21
CLK
CD
QI1
QI0
LX2
D
Q
QI1
CD
FD21
QI2
QI0
QI1
LX2
D
Q
QI2
CD
FD21
QI0
Q0
QI1
Q1
QI2
Q2
QI3
QI0
QI1
QI2
LX2
D
Q
QI3
CD
FD21
QI3
Q3
QI0
QI1
QI2
QI3
CAO

CBU28

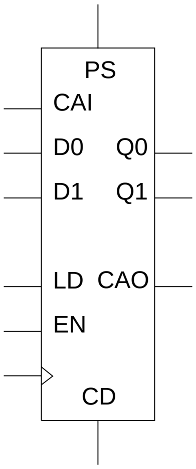

QI[0:7]
CAI
EN
CLK
CD
QI0
QI1
QI2
QI3
QI4
QI5
QI6
QI7
LX2
D
Q
CD
FD21
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
CAO

CBU31, CBU32, CBU34, and CBU38

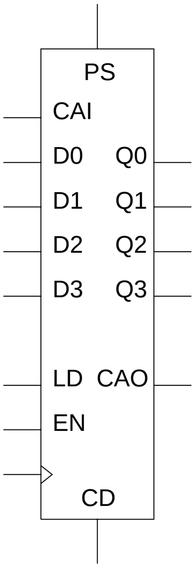
CBU31



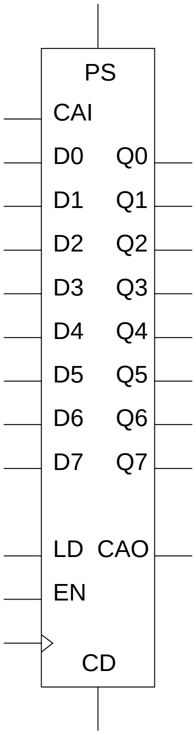
CBU32



CBU34



CBU38



Function:

1-, 2-, 4-, and 8-bit up counters with asynchronous clear, enable, parallel data load, synchronous preset, CAI, and CAO.

Availability:

CBU31, CBU32, CBU34, and CBU38 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Schematics appear on the following pages.

Type:

Soft:	CBU31 and CBU32.
Hard:	CBU34 and CBU38.

Logic Resources:

Macro	PT	GLB	Output	Level
CBU34	*	2	5	1**
CBU38	*	3	9	1**

* Q0-Q_{n-1}: 4 PT per output.
CAO: 1 PT.
CLK: 1 PT per GLB if Product Term Clock is used.
CD: 1 PT per GLB.

** (CAO is a 2-level output).

Macro Port Definition:

```
CBU31 (Q0,CAO,D0,CAI,CLK,PS,LD,EN,CD);
CBU32 (Q0,Q1,CAO,D0,D1,CAI,CLK,PS,LD,EN,CD);
CBU34 ([Q0..Q3],CAO,[D0..D3],CAI,CLK,PS,LD,EN,CD);
  CBU34_1 ([Q0..Q3],[D0..D3],CAI,CLK,PS,LD,EN,CD);
  CBU34_2 (CAO,[Q0..Q3],CAI,EN);
CBU38 ([Q0..Q7],CAO,[D0..D7],CAI,CLK,PS,LD,EN,CD);
  CBU38_1 ([Q0..Q3],[D0..D3],CAI,CLK,PS,LD,EN,CD);
  CBU38_2 (Q4,Q5,[Q0..Q3],D4,D5,CAI,CLK,PS,LD,EN,CD);
  CBU38_3 (Q6,Q7,[Q0..Q5],D6,D7,CAI,CLK,PS,LD,EN,CD);
  CBU38_4 (CAO,[Q0..Q7],CAI,EN);
```

Counting Ranges:

CBU31: 0-1. CBU32: 0-3. CBU34: 0-15. CBU38: 0-255.

Truth Table:

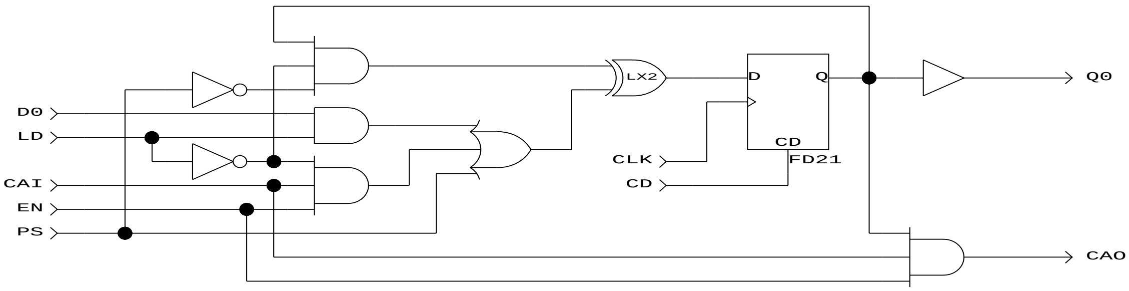
The truth table is the same for all CBU3s.

Input							Output	
CD	**PS**	**LD**	**D**	**EN**	**CAI**	**CLK**	**Q**	**CAO**
1	x	x	x	x	x	x	0	0
0	1	x	x	x	x	↑	1	CAI·EN
0	0	1	d	x	x	↑	d	*
0	0	0	x	0	x	x	Q	0
0	0	0	x	x	0	x	Q	0
0	0	0	x	1	1	↑	count up	**

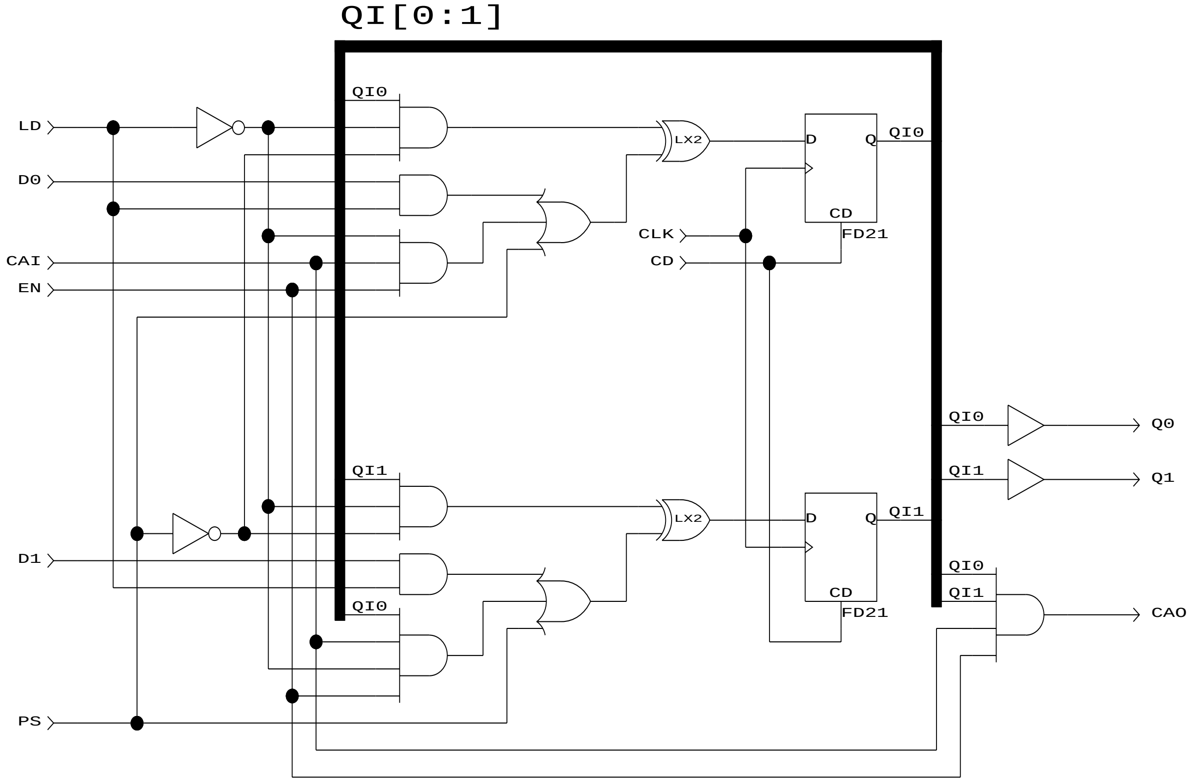
* CBU31: CAO = CAI·EN·D0
CBU32: CAO = CAI·EN·D0·D1
CBU34: CAO = CAI·EN·D0·D1·D2·D3
CBU38: CAO = CAI·EN·D0·D1·D2·D3·D4·D5·D6·D7

** CAO = 1 after terminal count, when CAI = 1 and EN = 1.
CAI·EN = shift registers: serial input, counters:
CAscade In, enable for multiplexors and counters,
d = any pattern of 1s and 0s on an input or set of inputs,
Q = output of flip-flop or latch, x = don’t care,
↑ = rising clock edge.

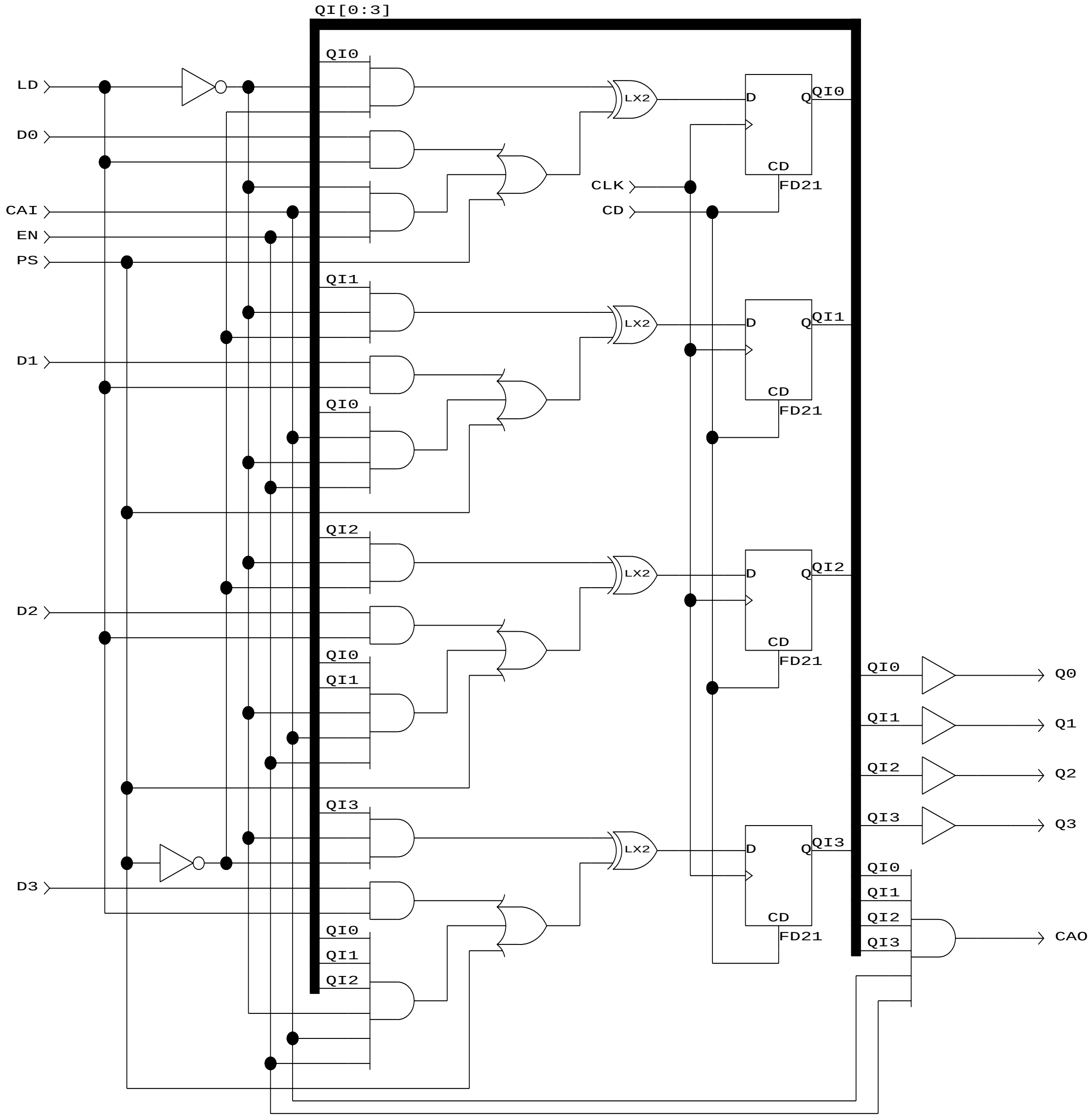
CBU31



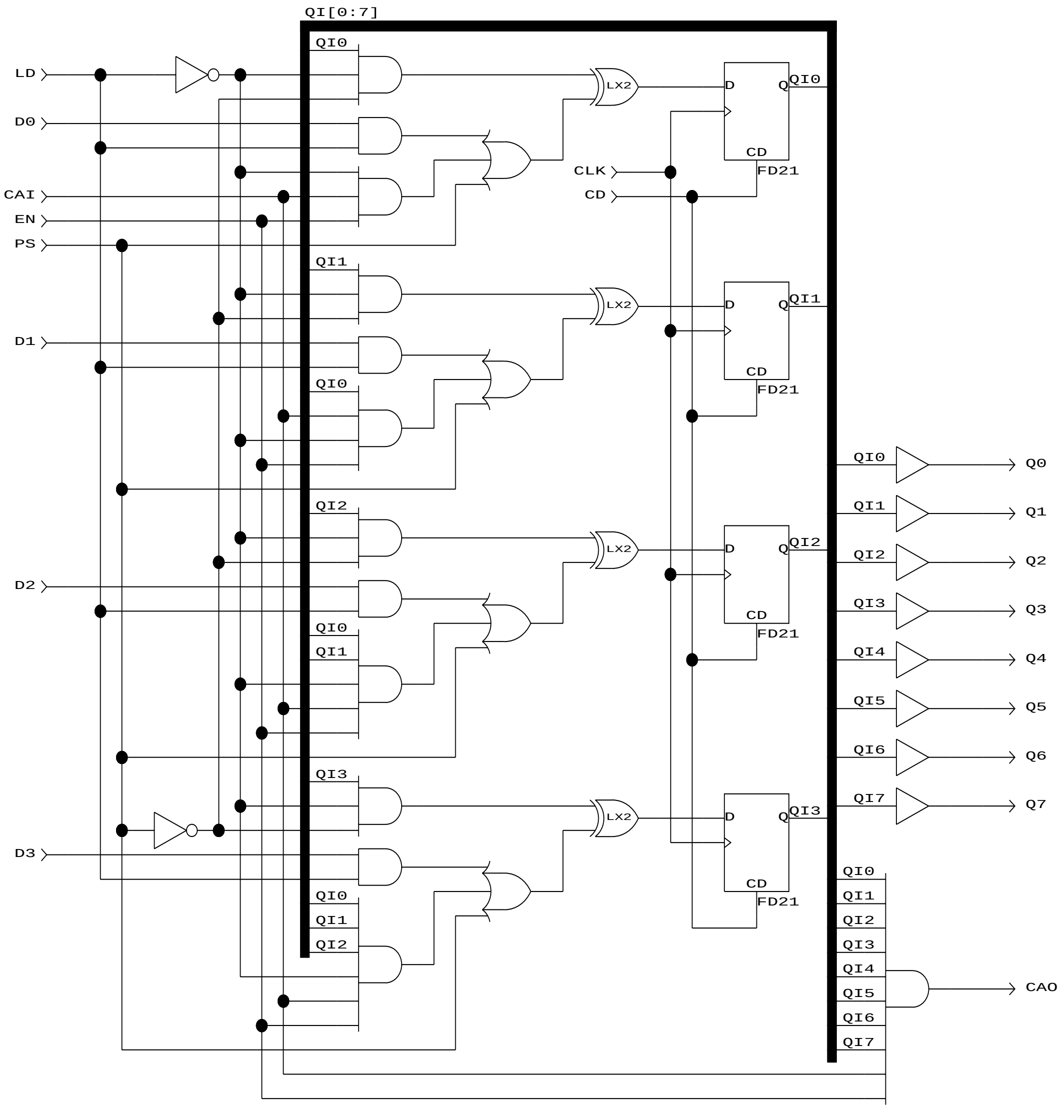
CBU32


QI[0:1]
QI0
LD
D0
CAI
EN
LX2
D
Q
QI0
CD
FD21
CLK
CD
QI0
Q0
QI1
Q1
QI1
LX2
D
Q
QI1
D1
CD
FD21
QI0
QI1
CAO
QI0
PS

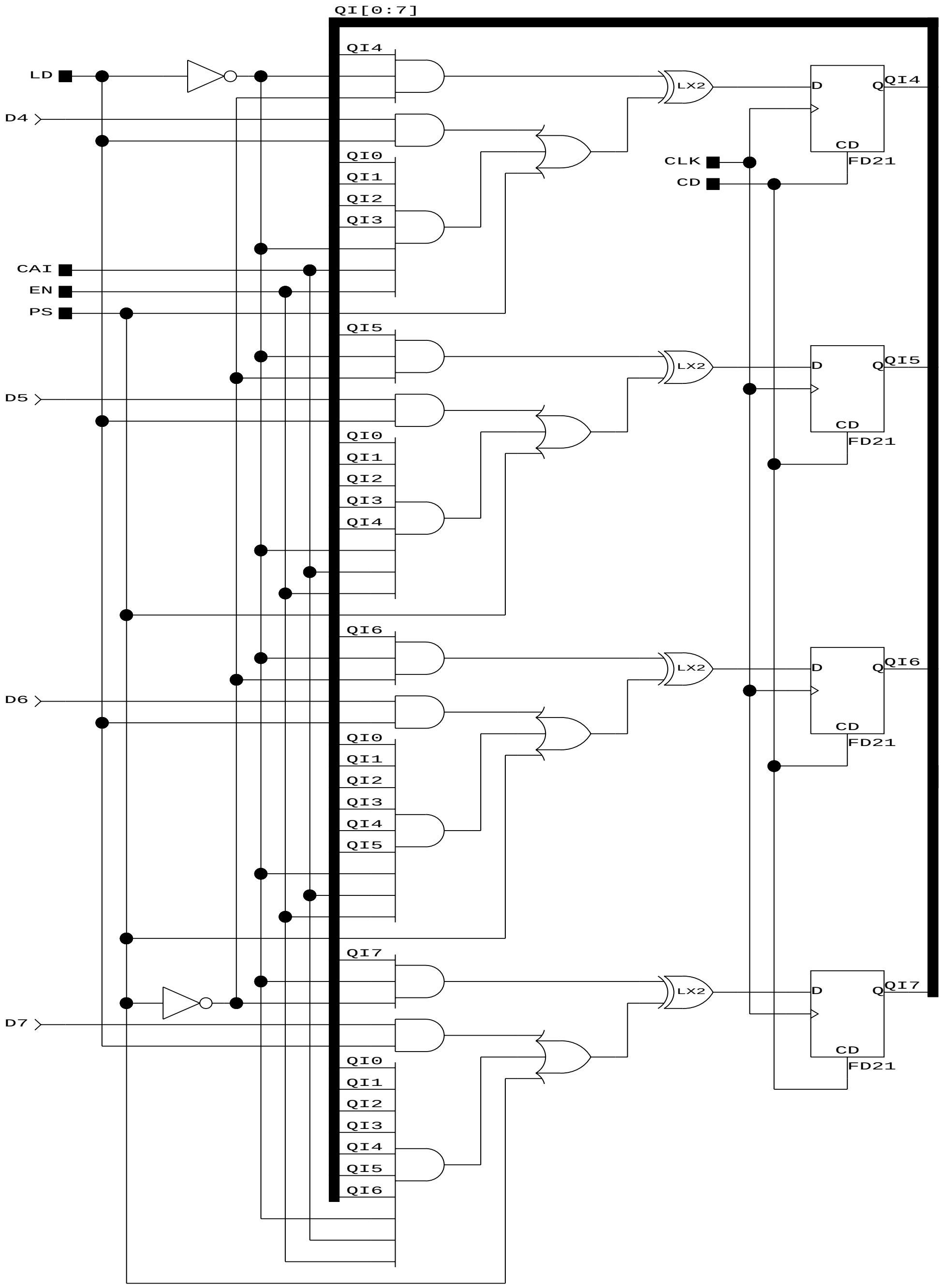
CBU34


QI[0:3]
LD
D0
CAI
EN
PS
D1
D2
D3
QI0
QI1
QI2
QI3
LX2
D
Q
CD
FD21
CLK
CD
Q0
Q1
Q2
Q3
CAO

CBU38.1

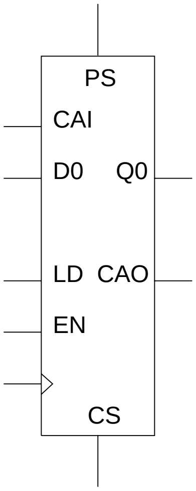

QI[0:7]
LD
D0
CAI
EN
PS
D1
D2
D3
CLK
CD
QI0
QI1
QI2
QI3
LX2
D
Q
CD
FD21
QI0
QI1
QI2
QI3
QI4
QI5
QI6
QI7
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
CAO

CBU38.2

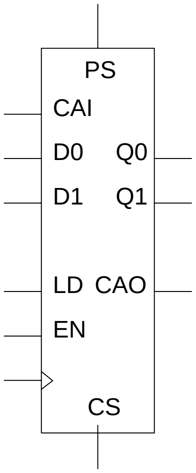

QI[0:7]
QI4
LD
D4
QI0
QI1
QI2
QI3
CAI
EN
PS
LX2
D
Q
QI4
CD
FD21
CLK
CD
QI5
D5
QI0
QI1
QI2
QI3
QI4
LX2
D
Q
QI5
CD
FD21
QI6
D6
QI0
QI1
QI2
QI3
QI4
QI5
LX2
D
Q
QI6
CD
FD21
QI7
D7
QI0
QI1
QI2
QI3
QI4
QI5
QI6
LX2
D
Q
QI7
CD
FD21

CBU41, CBU42, CBU44, and CBU48

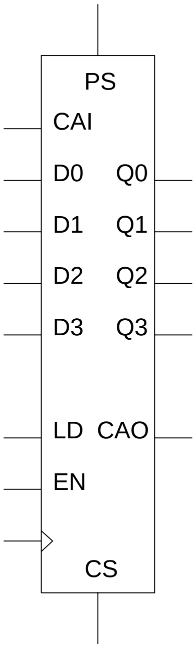
CBU41



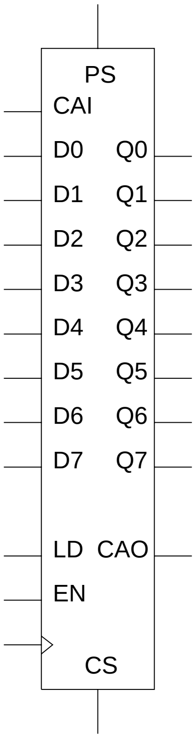
CBU42



CBU44



CBU48



Function:

1-, 2-, 4-, and 8-bit up counters with synchronous clear, enable, parallel data load, synchronous preset, CAI, and CAO.

Availability:

CBU41, CBU42, CBU44, and CBU48 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Schematics appear on the following pages.

Type:

Soft: CBU41 and CBU42.
Hard: CBU44 and CBU48.

Logic Resources:

Macro	PT	GLB	Output	Level
CBU44	*	2	5	1**
CBU48	*	3	9	1**

* Q0-Q_{n-1}: 4 PT per output.
CAO: 1 PT.
CLK: 1 PT per GLB if Product Term Clock is used.
** (CAO is a 2-level output).

Macro Port Definition:

```
CBU41 (Q0,CAO,D0,CAI,CLK,PS,LD,EN,CS);
CBU42 (Q0,Q1,CAO,D0,D1,CAI,CLK,PS,LD,EN,CS);
CBU44 ([Q0..Q3],CAO,[D0..D3],CAI,CLK,PS,LD,EN,CS);
  CBU44_1 ([Q0..Q3],[D0..D3],CAI,CLK,PS,LD,EN,CS);
  CBU44_2 (CAO,[Q0..Q3],CAI,EN);
CBU48 ([Q0..Q7],CAO,[D0..D7],CAI,CLK,PS,LD,EN,CS);
  CBU48_1 ([Q0..Q3],[D0..D3],CAI,CLK,PS,LD,EN,CS);
  CBU48_2 (Q4,Q5,[Q0..Q3],D4,D5,CAI,CLK,PS,LD,EN,CS);
  CBU48_3 (Q6,Q7,[Q0..Q5],D6,D7,CAI,CLK,PS,LD,EN,CS);
  CBU48_4 (CAO,[Q0..Q7],CAI,EN);
```

Counting Ranges:

CBU41: 0-1. CBU42: 0-3. CBU44: 0-15. CBU48: 0-255.

Truth Table:

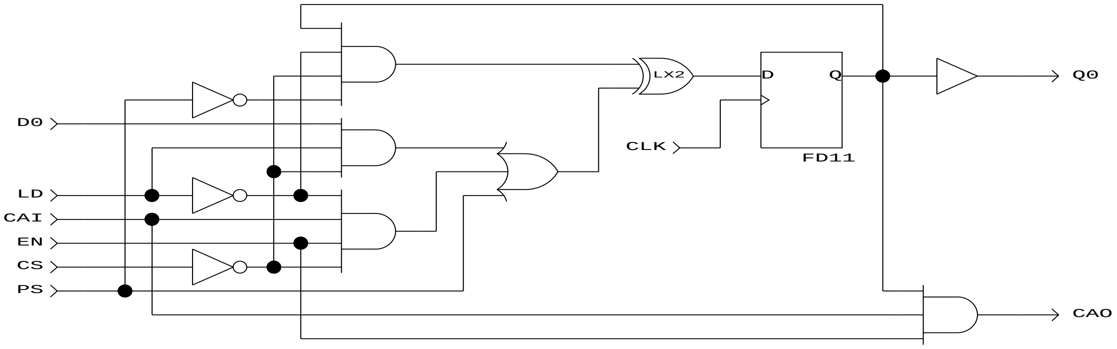
The truth table is the same for all CBU4s.

Input							Output	
PS	**CS**	**LD**	**D**	**EN**	**CAI**	**CLK**	**Q**	**CAO**
1	x	x	x	x	x	↑	1	CAI·EN
0	1	x	x	x	x	↑	0	0
0	0	1	d	x	x	↑	d	*
0	0	0	x	0	x	x	Q	0
0	0	0	x	x	0	x	Q	0
0	0	0	x	1	1	↑	count up	**

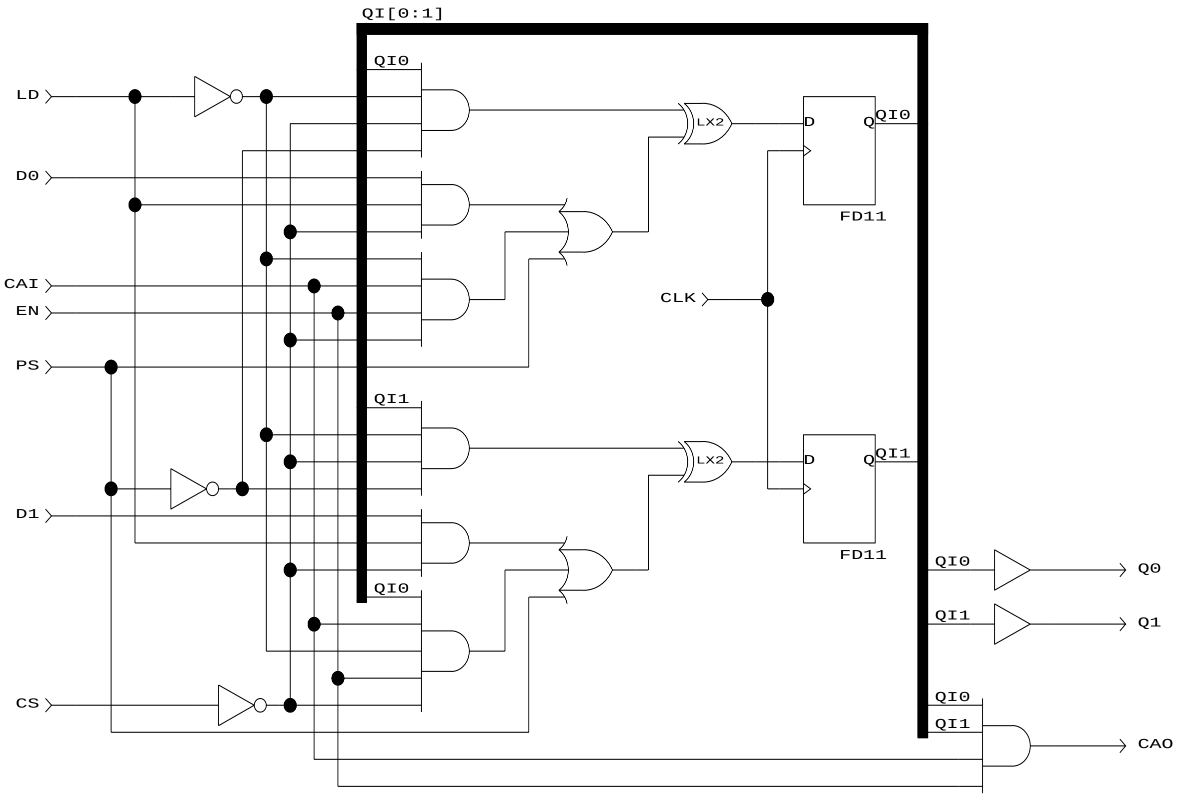
* CBU41: CAO = CAI·EN·D0
CBU42: CAO = CAI·EN·D0·D
CBU44: CAO = CAI·EN·D0·D1·D2·D3
CBU48: CAO = CAI·EN·D0·D1·D2·D3·D4·D5·D6·D7

** CAO = 1 after terminal count, when CAI = 1 and EN = 1.
CAI·EN = shift registers: serial input, counters:
CAscade In, enable for multiplexors and counters,
d = any pattern of 1s and 0s on an input or set of inputs,
Q = output of flip-flop or latch, x = don’t care,
↑ = rising clock edge.

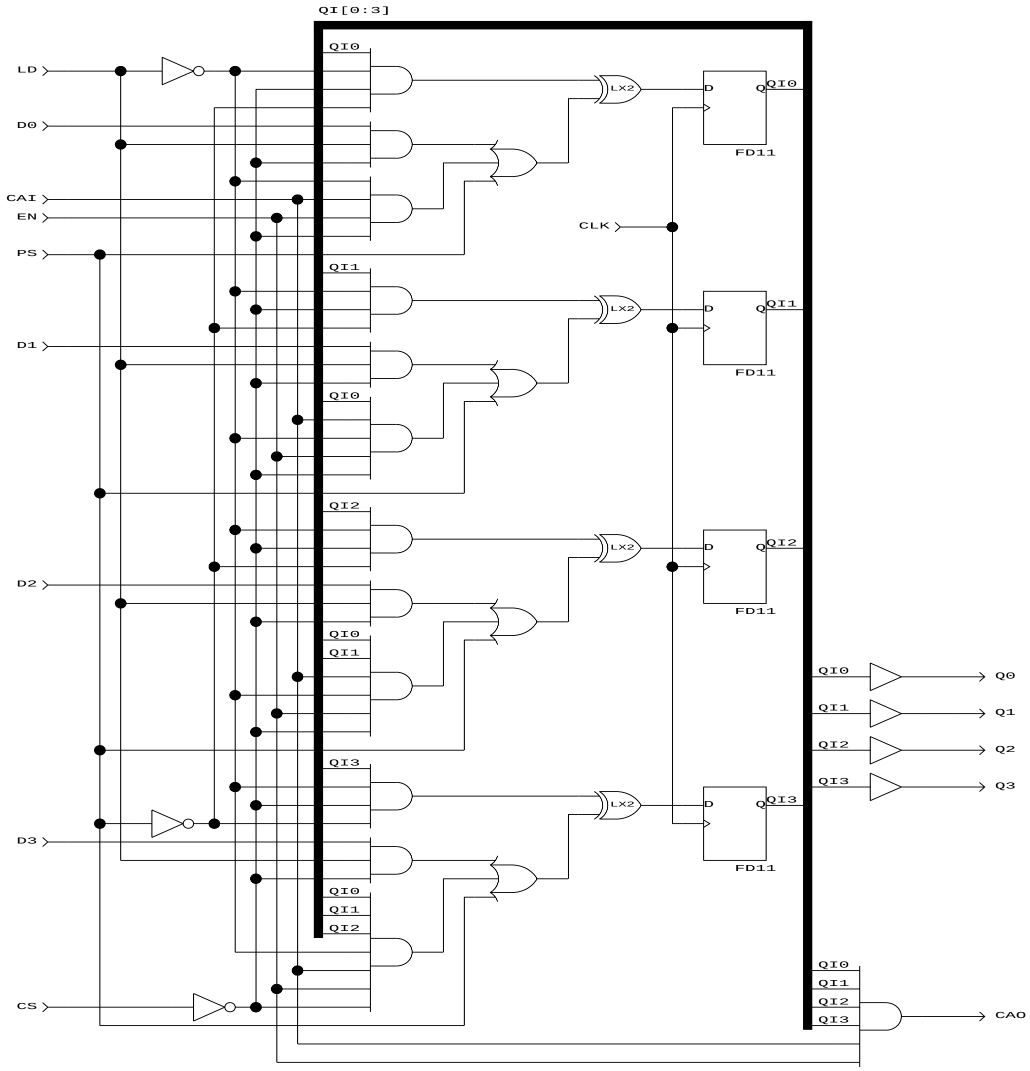
CBU41



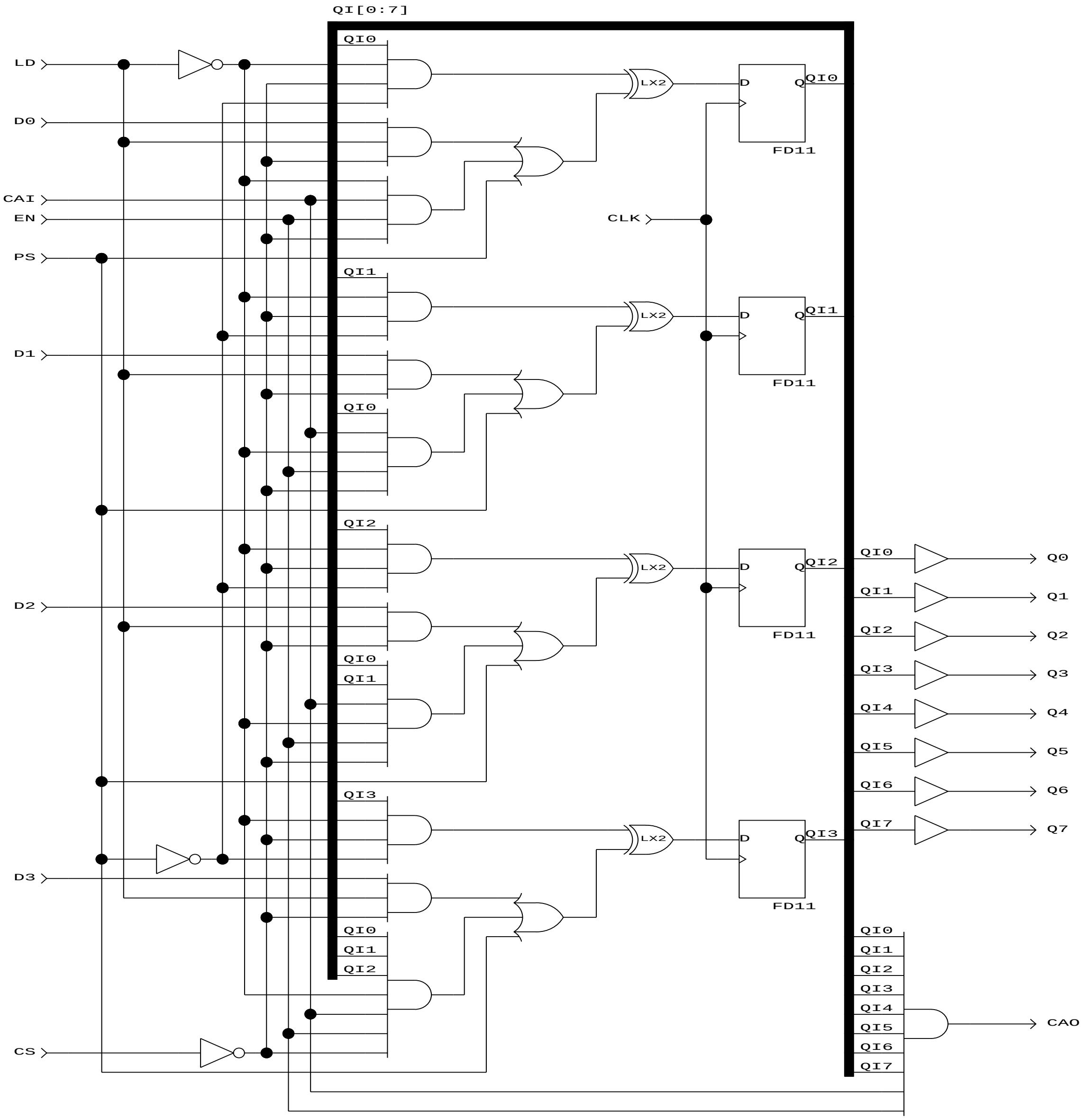
CBU42


QI[0:1]
QI0
LD
D0
CAI
EN
PS
QI1
D1
QI0
CS
LX2
D
Q
QI0
FD11
CLK
LX2
D
Q
QI1
FD11
QI0
Q0
QI1
Q1
QI0
QI1
CAO

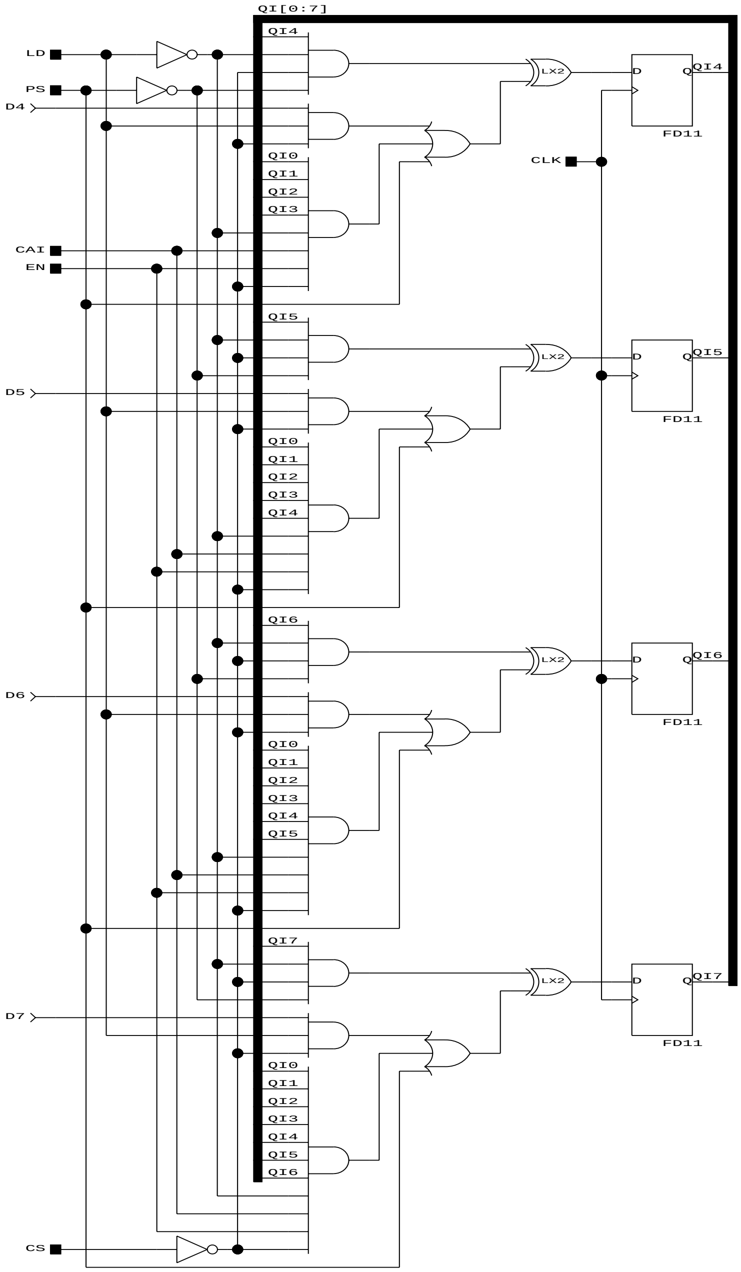
CBU44


QI[0:3]
LD
D0
CAI
EN
PS
D1
D2
D3
CS
CLK
QI0
QI1
QI2
QI3
LX2
D
Q
FD11
Q0
Q1
Q2
Q3
CAO

CBU48.1


QI[0:7]
QI0
LD
D0
CAI
EN
PS
QI1
D1
QI0
QI2
D2
QI0
QI1
QI3
D3
QI0
QI1
QI2
CS
LX2
LX2
LX2
LX2
D
Q
QI0
FD11
CLK
D
Q
QI1
FD11
D
Q
QI2
FD11
D
Q
QI3
FD11
QI0
Q0
QI1
Q1
QI2
Q2
QI3
Q3
QI4
Q4
QI5
Q5
QI6
Q6
QI7
Q7
QI0
QI1
QI2
QI3
QI4
QI5
QI6
QI7
CAO

CBU48.2


QI[0:7]
QI4
LD
PS
D4
QI0
QI1
QI2
QI3
CAI
EN
LX2
D
Q
QI4
FD11
CLK
QI5
D5
QI0
QI1
QI2
QI3
QI4
QI5
FD11
QI6
D6
QI0
QI1
QI2
QI3
QI4
QI5
QI6
FD11
QI7
D7
QI0
QI1
QI2
QI3
QI4
QI5
QI6
QI7
FD11
CS

CBU516 and CBU616

Function:

16-bit up counters with asynchronous clear and enable. CBU616 also has CAO.

Availability:

CBU516 and CBU616 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Schematics appear on the following pages.

Type: Hard

Logic Resources:

Macro	PT	GLB	Output	Level
CBU516	*	4	16	1
CBU616	*	5	18	2**

* Q0-Q_{n-1}: 2 PT per output.
CLK: 1 PT per GLB if Product Term Clock is used.
CD: 1 PT per GLB.

** (CAO is a 2-level output).

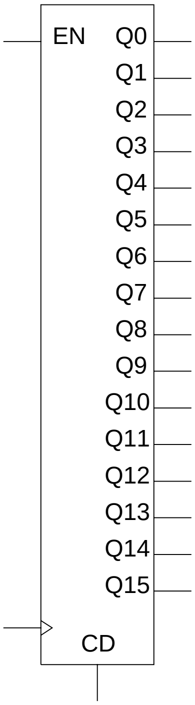
Macro Port Definition:

```
CBU516 ([Q0..Q15],CLK,EN,CD);
  CBU516_1 ([Q0..Q3],CLK,EN,CD);
  CBU516_2 ([Q4..Q7],[Q0..Q3],CLK,EN,CD);
  CBU516_3 ([Q8..Q11],[Q0..Q7],CLK,EN,CD);
  CBU516_4 ([Q12..Q15],[Q0..Q11],CLK,EN,CD);
CBU616 ([Q0..Q15],CAO,CLK,EN,CD);
  CBU616_1 ([Q0..Q3],CLK,EN,CD);
  CBU616_2 ([Q4..Q7],[Q0..Q3],CLK,EN,CD);
  CBU616_3 ([Q8..Q11],[Q0..Q7],CLK,EN,CD);
  CBU616_4 (Q12,Q13,[Q0..Q11],CLK,EN,CD);
  CBU616_5 (Q14,Q15,CAO,[Q0..Q13],CLK,EN,CD);
```

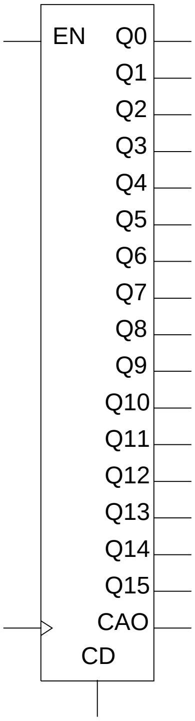
Counting Ranges:

CBU516: 0-65,535. CBU616: 0-65,535.

CBU516



CBU616



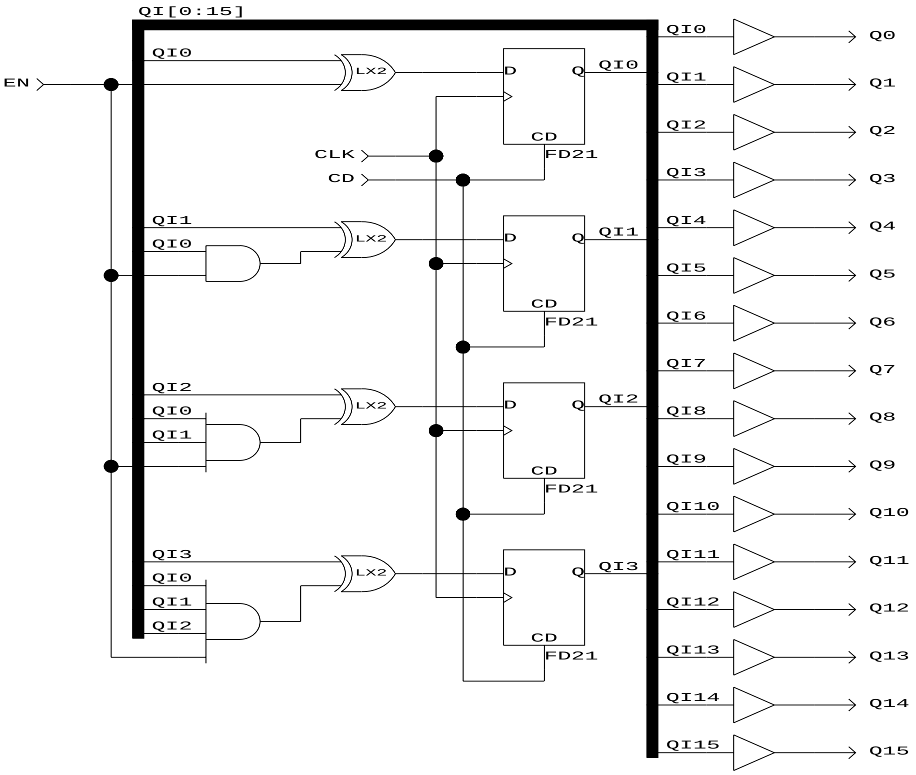
Truth Table:

Gray areas (CAO) apply only to the CBU616.

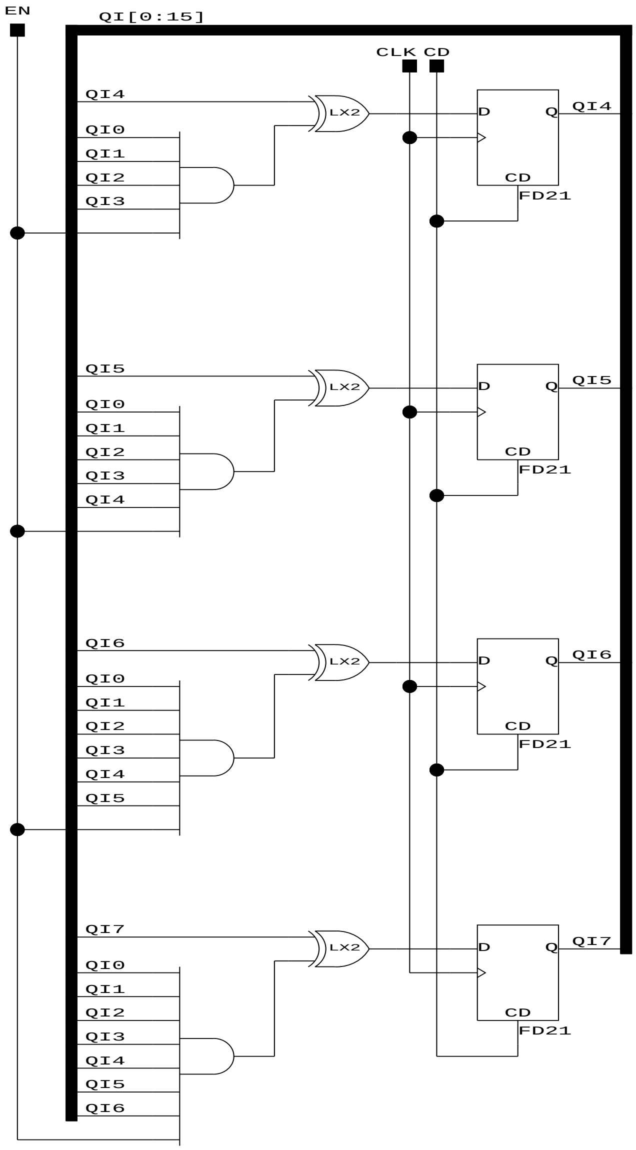
Input			Output	
CD	**EN**	**CLK**	**Q**	**CAO**
1	x	CLK	0	0
0	0	x	Q	0
0	1	↑	count up	*

* CAO = 1 after terminal count,
when EN = 1 and each terminal count bit = 1.
Q = output of flip-flop or latch, x = don’t care,
↑ = rising clock edge.

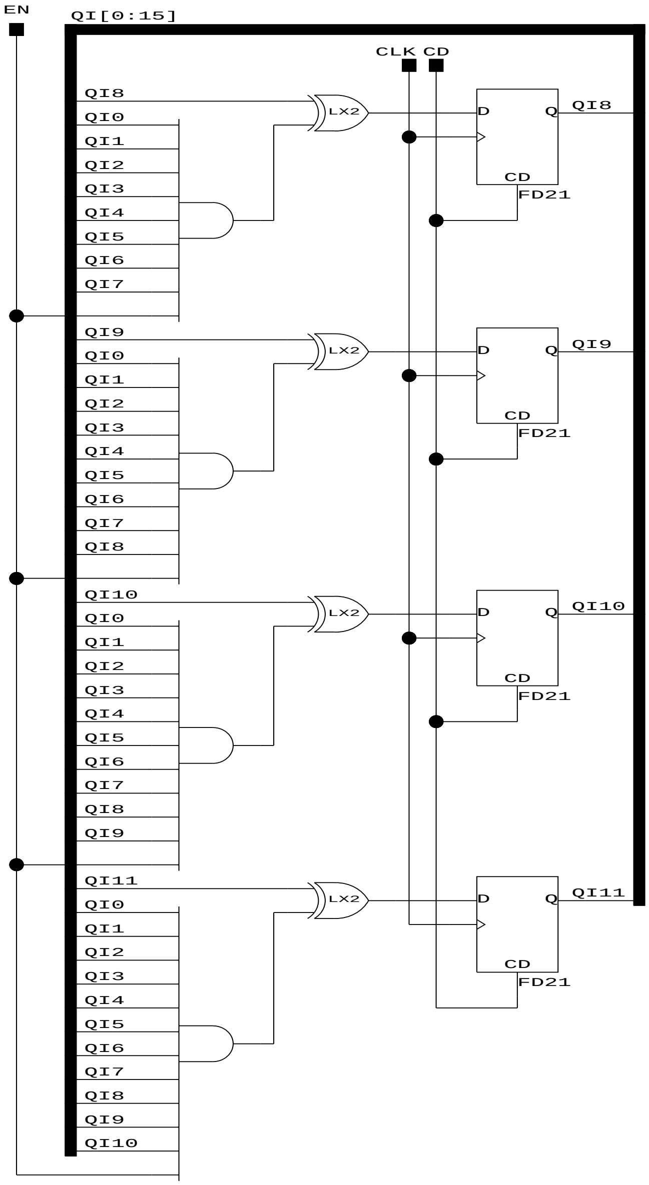
CBU516.1


QI[0:15]
EN
QI0
LX2
D
Q
QI0
CD
FD21
CLK
CD
QI1
QI0
LX2
D
Q
QI1
CD
FD21
QI2
QI0
QI1
LX2
D
Q
QI2
CD
FD21
QI3
QI0
QI1
QI2
LX2
D
Q
QI3
CD
FD21
QI0
Q0
QI1
Q1
QI2
Q2
QI3
Q3
QI4
Q4
QI5
Q5
QI6
Q6
QI7
Q7
QI8
Q8
QI9
Q9
QI10
Q10
QI11
Q11
QI12
Q12
QI13
Q13
QI14
Q14
QI15
Q15

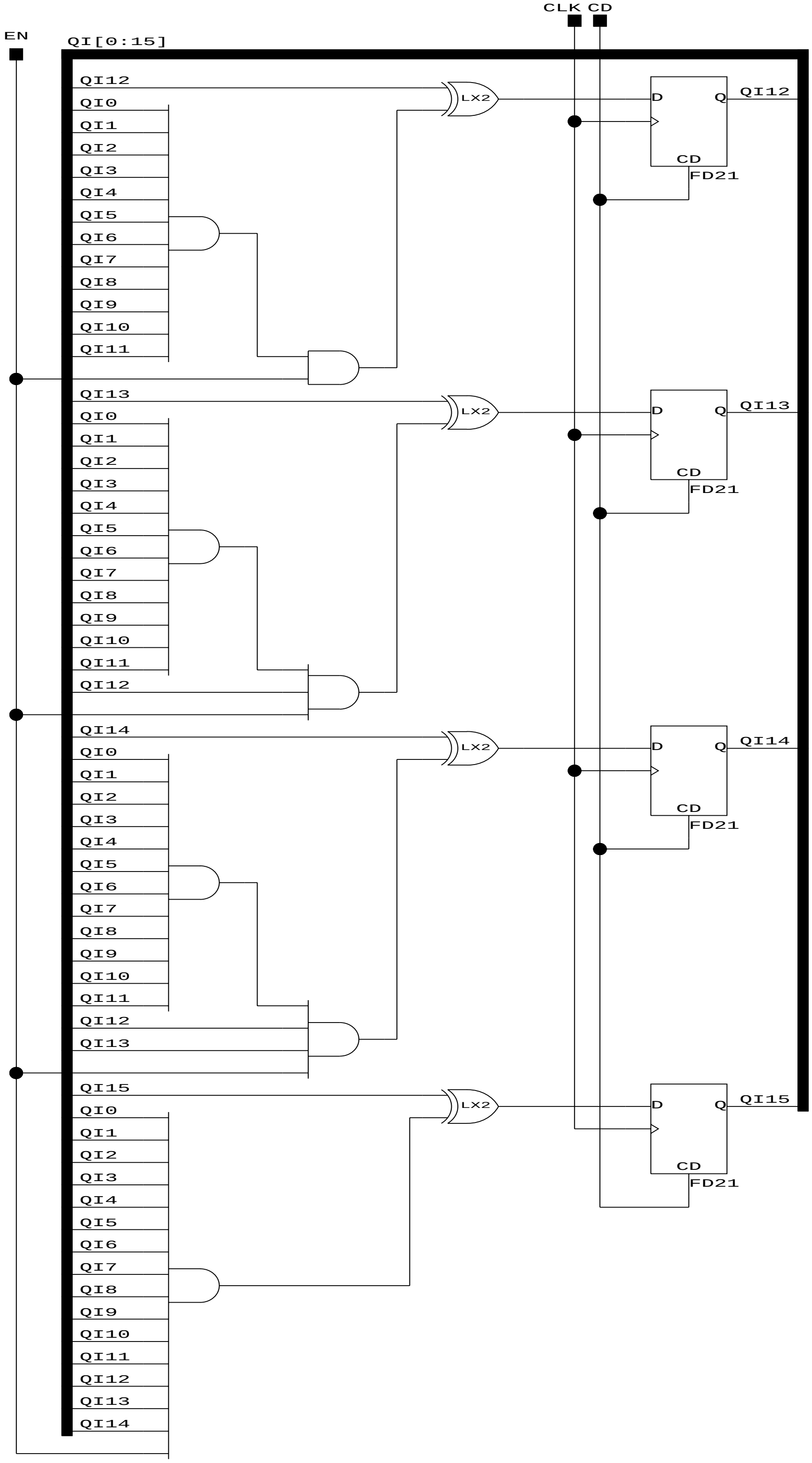
CBU516.2


EN
QI[0:15]
CLK
CD
QI4
QI0
QI1
QI2
QI3
LX2
D
Q
CD
FD21
QI4
QI5
QI0
QI1
QI2
QI3
QI4
LX2
D
Q
CD
FD21
QI5
QI6
QI0
QI1
QI2
QI3
QI4
QI5
LX2
D
Q
CD
FD21
QI6
QI7
QI0
QI1
QI2
QI3
QI4
QI5
QI6
LX2
D
Q
CD
FD21
QI7

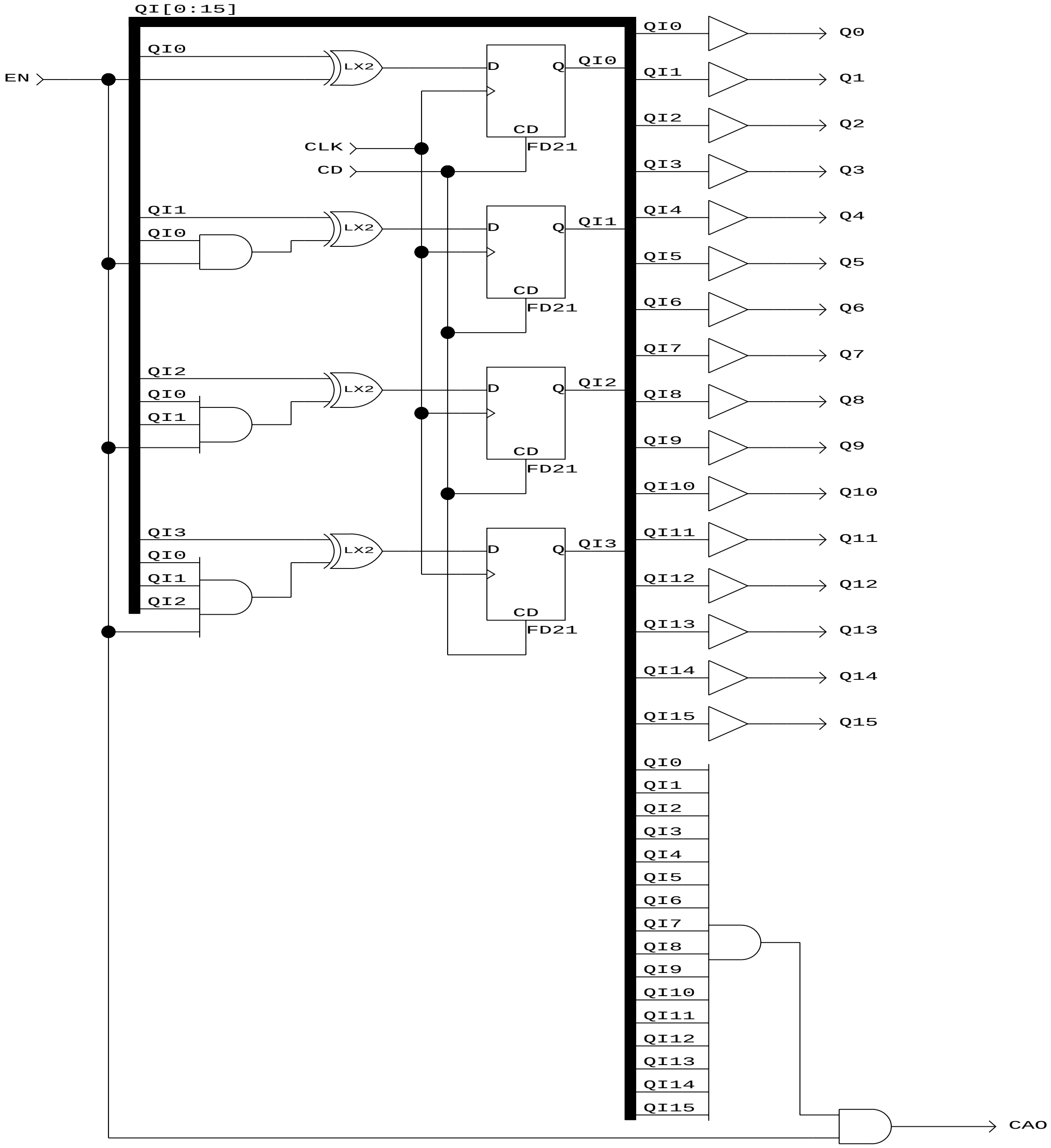
CBU516.3


EN
QI[0:15]
CLK CD
QI8
QI0
QI1
QI2
QI3
QI4
QI5
QI6
QI7
LX2
D
Q
CD
FD21
QI8
QI9
QI10
QI11

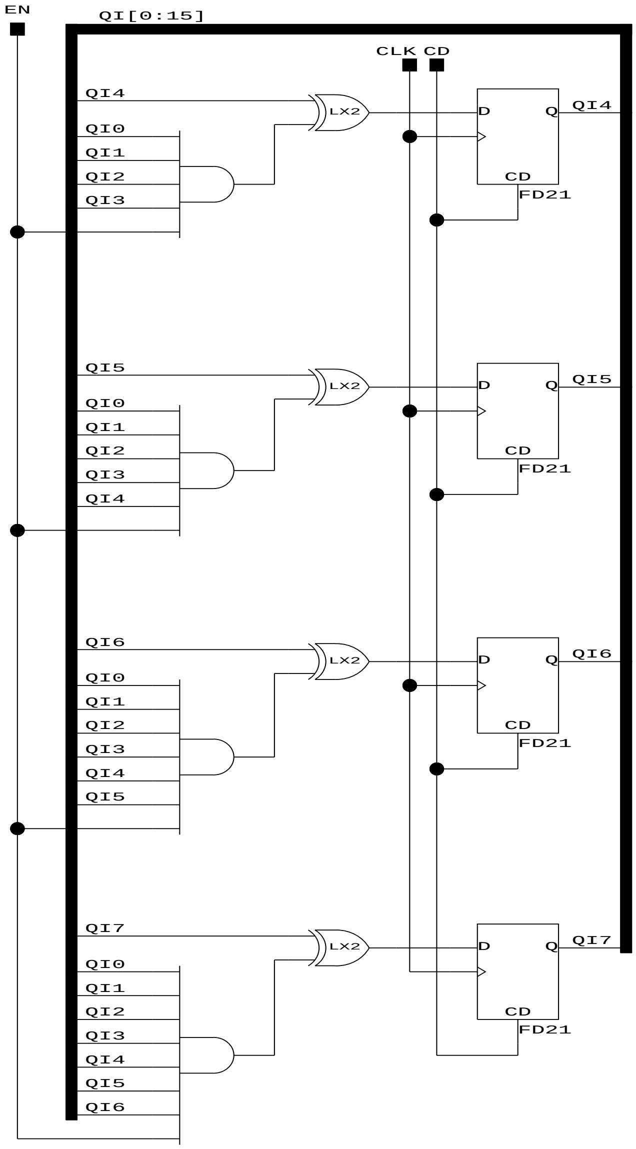
CBU516.4


CLK
CD
EN
QI[0:15]
QI12
QI0
QI1
QI2
QI3
QI4
QI5
QI6
QI7
QI8
QI9
QI10
QI11
LX2
D
Q
CD
FD21
QI12
QI13
QI13
QI14
QI14
QI15
QI15

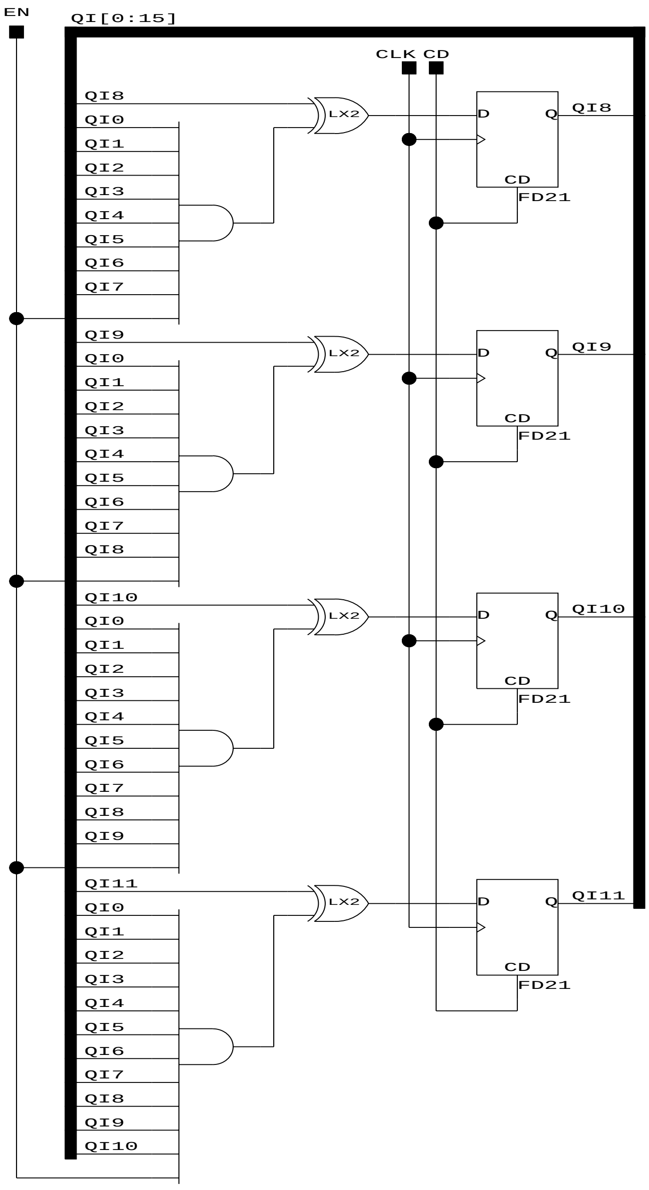
CBU616.1


QI[0:15]
EN
CLK
CD
QI0
QI1
QI2
QI3
LX2
D
Q
CD
FD21
QI0
QI1
QI2
QI3
QI4
QI5
QI6
QI7
QI8
QI9
QI10
QI11
QI12
QI13
QI14
QI15
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
CAO

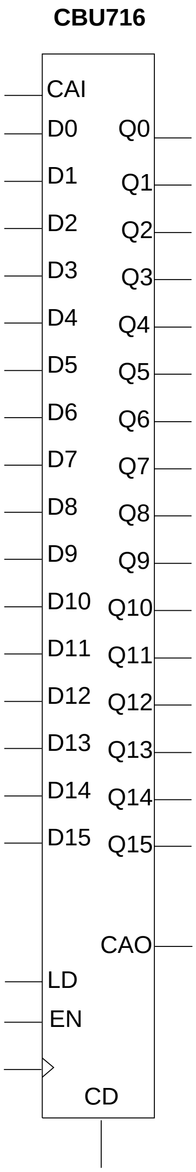
CBU616.3


EN
QI[0:15]
CLK
CD
QI4
QI0
QI1
QI2
QI3
LX2
D
Q
CD
FD21
QI4
QI5
QI0
QI1
QI2
QI3
QI4
LX2
D
Q
CD
FD21
QI5
QI6
QI0
QI1
QI2
QI3
QI4
QI5
LX2
D
Q
CD
FD21
QI6
QI7
QI0
QI1
QI2
QI3
QI4
QI5
QI6
LX2
D
Q
CD
FD21
QI7

CBU616.4


EN
QI[0:15]
CLK
CD
QI8
QI0
QI1
QI2
QI3
QI4
QI5
QI6
QI7
LX2
D
Q
QI8
CD
FD21
QI9
QI0
QI1
QI2
QI3
QI4
QI5
QI6
QI7
QI8
LX2
D
Q
QI9
CD
FD21
QI10
QI0
QI1
QI2
QI3
QI4
QI5
QI6
QI7
QI8
QI9
LX2
D
Q
QI10
CD
FD21
QI11
QI0
QI1
QI2
QI3
QI4
QI5
QI6
QI7
QI8
QI9
QI10
LX2
D
Q
QI11
CD
FD21

CBU716



Function:

16-bit up counter with asynchronous clear, enable, parallel data load and carry out.

Availability:

CBU716 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Schematics appear on the following pages.

Type: Soft

Macro Port Definition:

```
CBU716 ([Q0..Q15],CAO,CLK,EN,LD,CD,CAI,[D0..D15]);
  CBU716_1 ([Q0..Q3],[D0..D3],CAI,CLK,LD,EN,CD);
  CBU716_2 ([Q4..Q7],[Q0..Q3],[D4..D7],CAI,CLK,
               LD,EN,CD);
  CBU716_3 ([Q8..Q11],[Q0..Q7],[D8..D11],CAI,CLK,
               LD,EN,CD);
  CBU716_4 ([Q12..Q15],[Q0..Q11],[D12..D15],
               CAI,CLK,LD,EN,CD);
  CBU716_5 (CAO,[Q0..Q15],CAI,EN);
```

Counting Ranges:

0 - 65,535

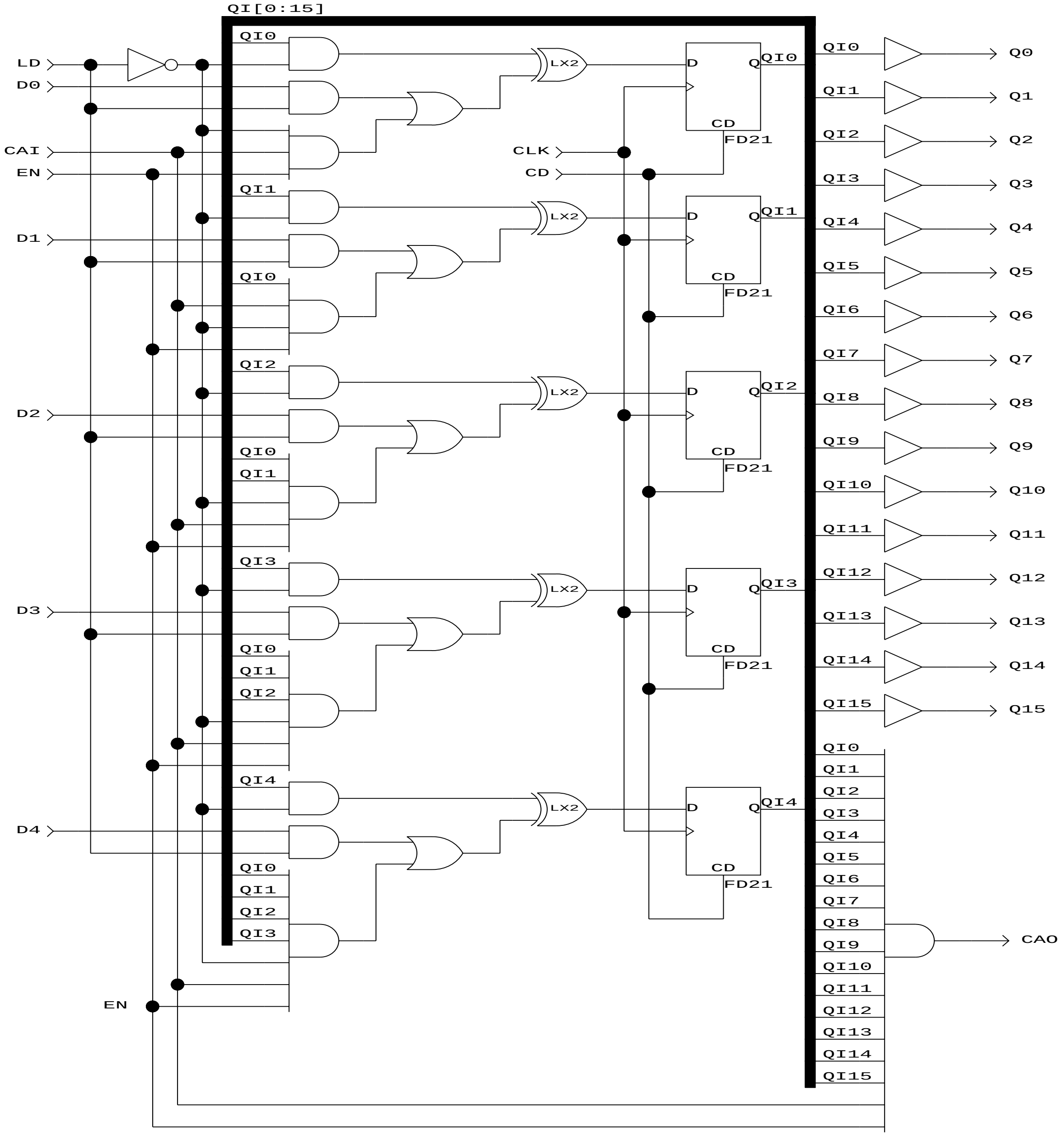
Truth Table:

Input						Output	
CD	LD	D	EN	CAI	CLK	Q	CAO
1	X	X	X	X	X	0	CAI • EN
0	1	d	X	X	↑	d	*
0	0	X	0	X	X	Q	0
0	0	X	X	0	X	Q	0
0	0	X	1	1	↑	count up	**

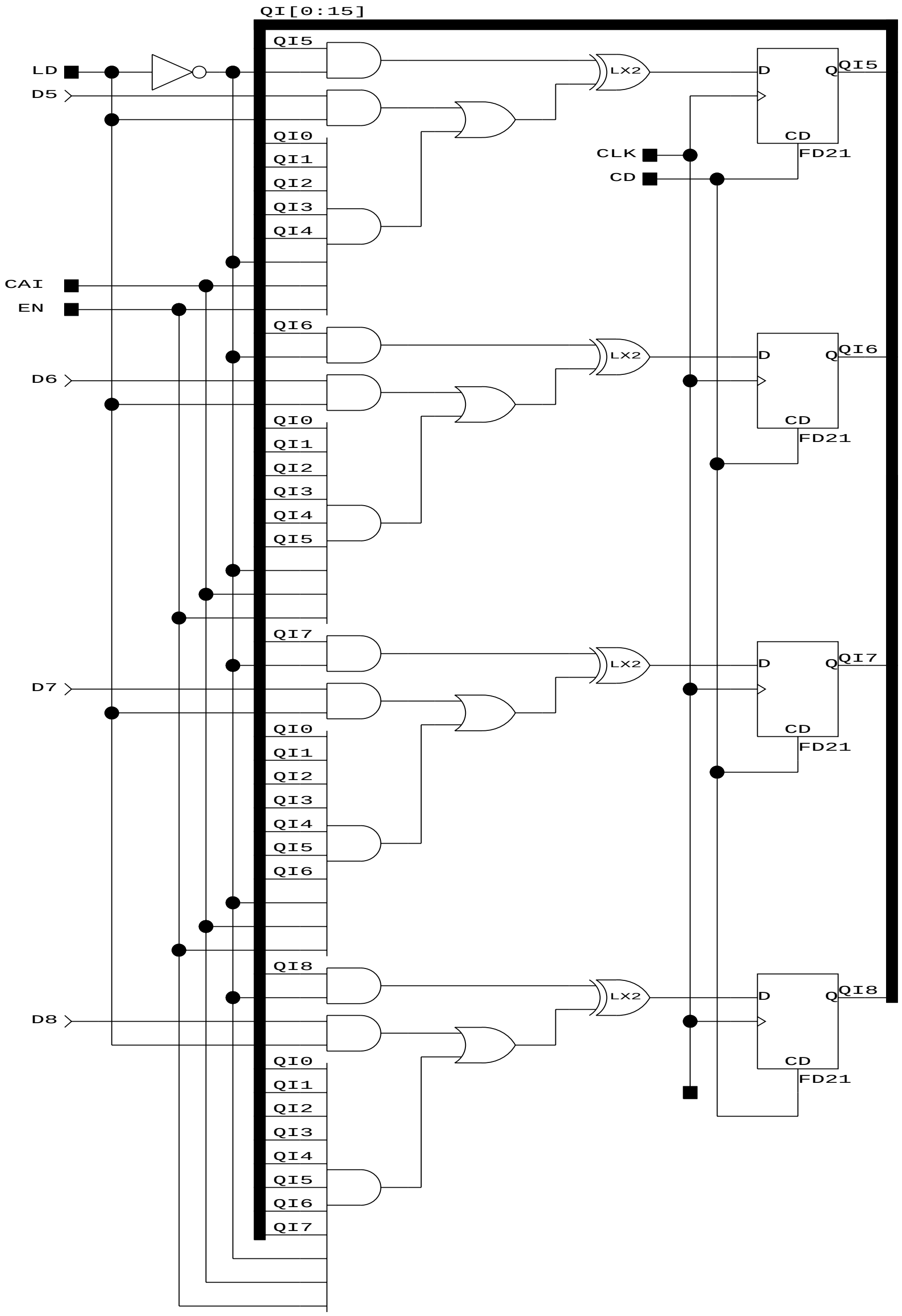
* CBU716: CAO = CAI, EN, D0, D1, D2, D3, D4, D5,
D6, D7, D8, D9, D10, D11, D12,
D13, D14, D15.

** CAO = 1 after terminal count, when CAI = 1 and EN = 1.
Q = output of flip-flop or latch, x = don’t care,
↑ = rising clock edge.

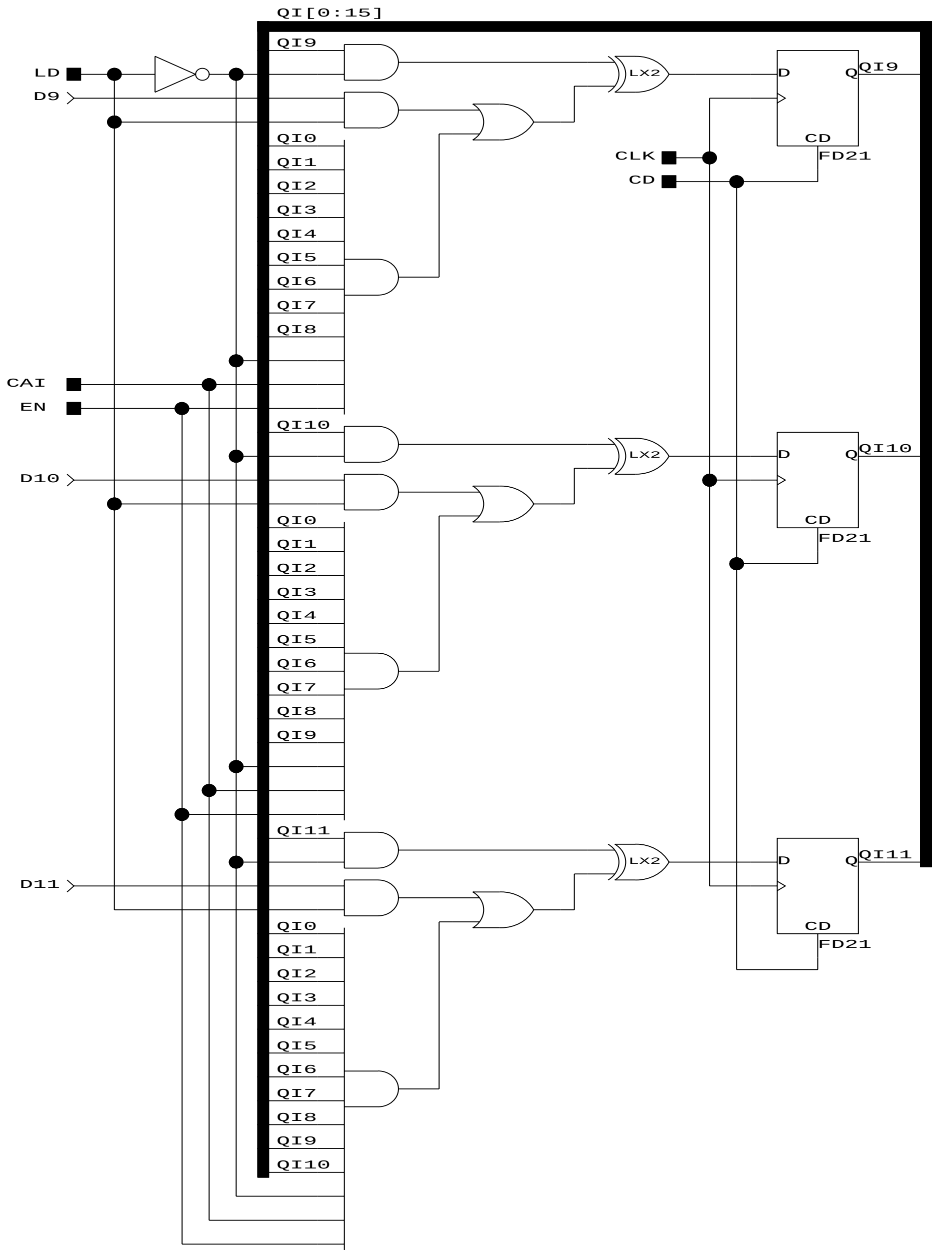
CBU716.1


QI[0:15]
LD
D0
CAI
EN
D1
D2
D3
D4
EN
CLK
CD
QI0
QI1
QI2
QI3
QI4
LX2
D
Q
CD
FD21
QI0
QI1
QI2
QI3
QI4
QI5
QI6
QI7
QI8
QI9
QI10
QI11
QI12
QI13
QI14
QI15
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
Q8
Q9
Q10
Q11
Q12
Q13
Q14
Q15
CAO

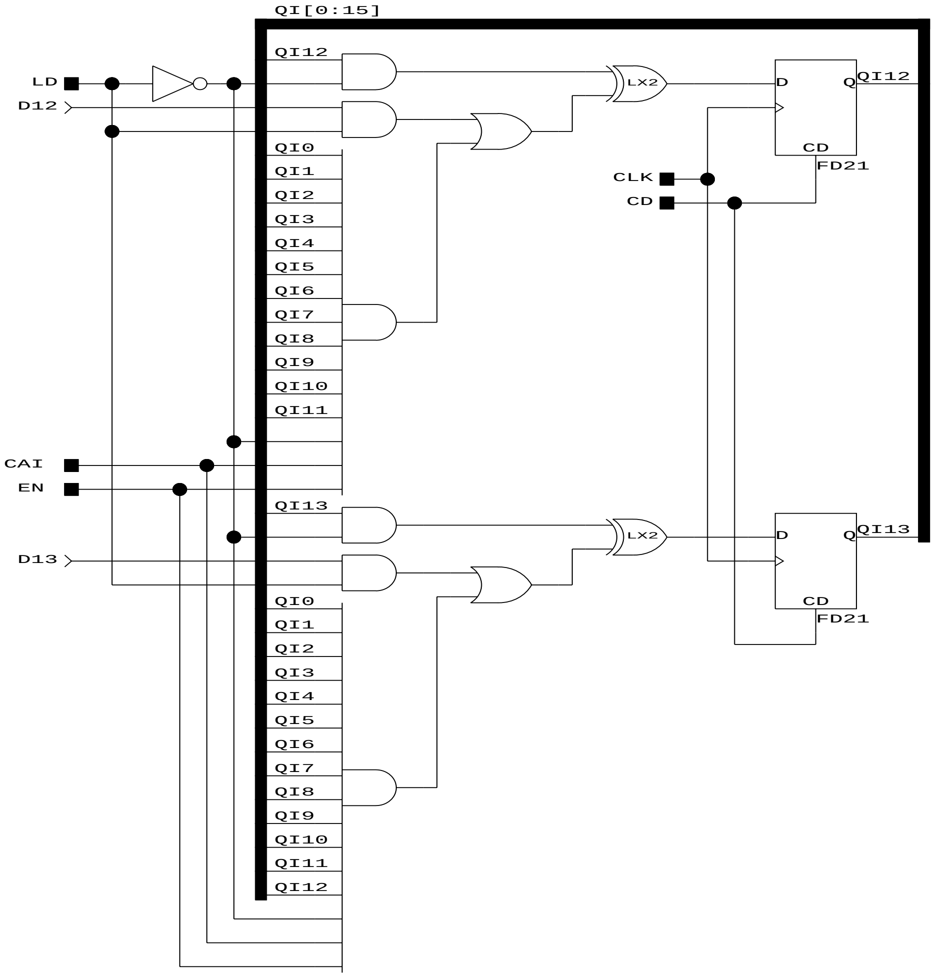
CBU716.2


QI[0:15]
LD
D5
CAI
EN
D6
D7
D8
CLK
CD
QI0
QI1
QI2
QI3
QI4
QI5
QI6
QI7
QI8
LX2
D
Q
CD
FD21

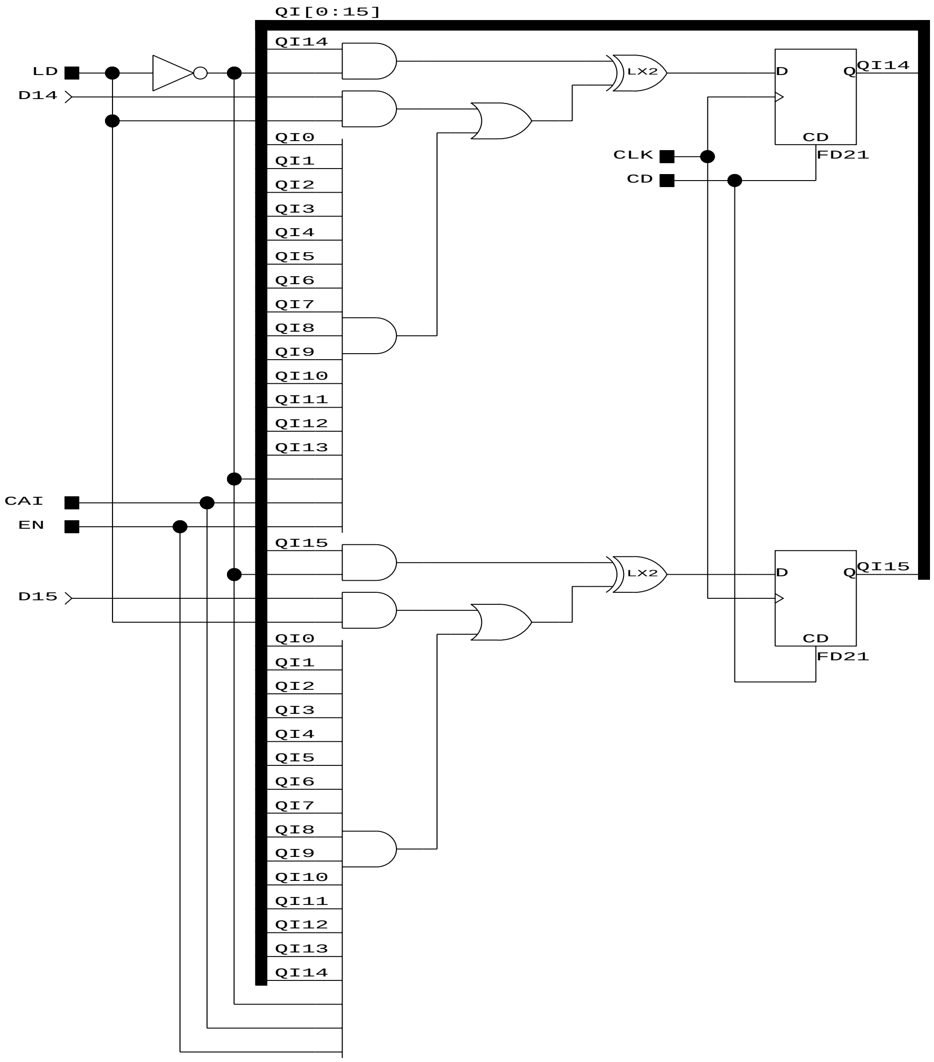
CBU716.3


QI[0:15]
QI9
LD
D9
QI0
QI1
QI2
QI3
QI4
QI5
QI6
QI7
QI8
CAI
EN
QI10
D10
QI9
QI11
D11
LX2
D
Q
CD
FD21
CLK
CD

CBU716.4

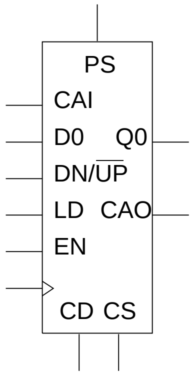

QI[0:15]
QI12
LD
D12
QI0
QI1
QI2
QI3
QI4
QI5
QI6
QI7
QI8
QI9
QI10
QI11
LX2
D
Q
QI12
CD
FD21
CLK
CD
CAI
EN
QI13
D13
QI0
QI1
QI2
QI3
QI4
QI5
QI6
QI7
QI8
QI9
QI10
QI11
QI12
LX2
D
Q
QI13
CD
FD21

CBU716.5

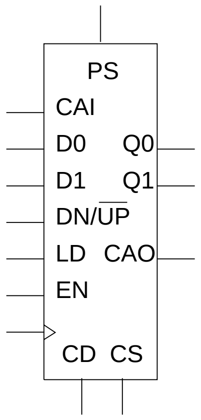

QI[0:15]
QI14
LD
D14
LX2
D
Q
QI14
CD
FD21
CLK
CD
QI0
QI1
QI2
QI3
QI4
QI5
QI6
QI7
QI8
QI9
QI10
QI11
QI12
QI13
CAI
EN
QI15
D15
LX2
D
Q
QI15
CD
FD21
QI0
QI1
QI2
QI3
QI4
QI5
QI6
QI7
QI8
QI9
QI10
QI11
QI12
QI13
QI14

CBUD1, CBUD2, CBUD4, and CBUD8

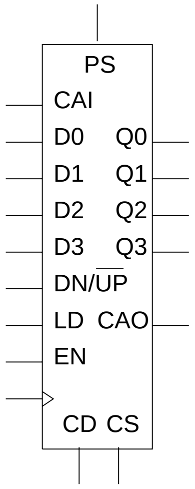
CBUD1



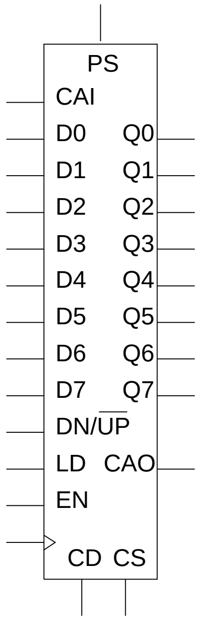
CBUD2



CBUD4



CBUD8



Function:

1-, 2-, 4-, and 8-bit up/down counters with asynchronous clear, synchronous clear, enable, parallel data load, synchronous preset, CAI, and CAO.

Availability:

CBUD1, CBUD2, CBUD4, and CBUD8 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Schematics appear on the following pages.

Type:

Soft: CBUD1 and CBUD2.
Hard: CBUD4 and CBUD8.

Logic Resources:

Macro	PT	GLB	Output	Level
CBUD4	*/out	2	5	1**
CBUD8	*/out	4	9	1**

* Q0: 4 PT. Q1-Q_{n-1}: 5 PT.
CAO: 2 PT.
CLK: 1 PT per GLB if Product Term Clock is used.
CD: 1 PT per GLB.

** (CAO is a 2-level output).

Macro Port Definition:

```
CBUD1 (Q0,CAO,D0,CAI,CLK,PS,LD,EN,DNUP,CD,CS);
CBUD2 (Q0,Q1,CAO,D0,D1,CAI,CLK,PS,LD,EN,DNUP,CD,CS);
CBUD4 ([Q0..Q3],CAO,[D0..D3],CAI,CLK,PS,LD,EN,DNUP,CD,CS);
  CBUD4_1 ([Q0..Q2],[D0..D2],CAI,CLK,PS,LD,EN,DNUP,CD,CS);
  CBUD4_2 (Q3,CAO,[Q0..Q2],D3,CAI,CLK,PS,LD,EN,DNUP,CD,CS);
CBUD8 ([Q0..Q7],CAO,[D0..D7],CAI,CLK,PS,LD,EN,DNUP,CD,CS);
  CBUD8_1 ([Q0..Q2],[D0..D2],CAI,CLK,PS,LD,EN,DNUP,CD,CS);
  CBUD8_2  [Q3..Q5],[Q0..Q2],[D3..D5],CAI,CLK,PS,LD,EN,DNUP,CD,CS);
  CBUD8_3 (Q6,Q7,CAO,[Q0..Q5],D6,D7,CAI,CLK,PS,LD,EN,DNUP,CD,CS);
```

Counting Ranges:

CBUD1: 0↔1. CBUD2: 0↔3. CBUD4: 0↔15. CBUD8: 0↔255.

Truth Table:

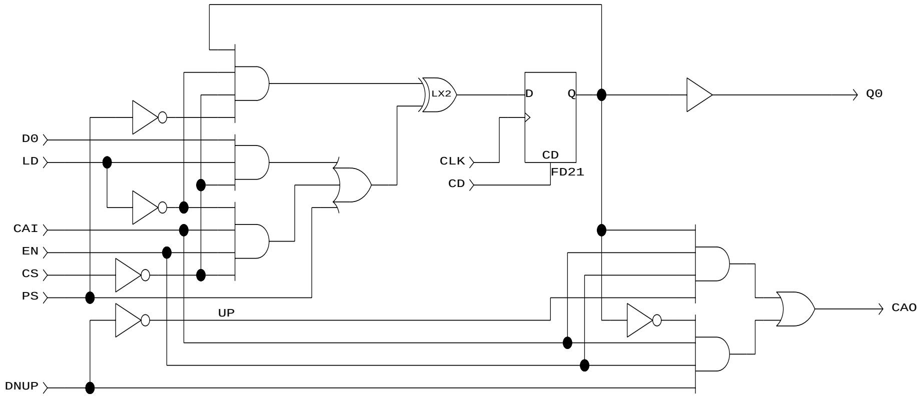
The truth table is the same for all CBUDs.

Input									Output	
CD	**PS**	**CS**	**LD**	**D**	**EN**	**CAI**	**DNUP**	**CLK**	**Q**	**CAO**
1	x	x	x	x	x	x	x	x	0	$\mathrm{CAI \cdot EN \cdot DNUP}$
0	1	x	x	x	x	x	x	↑	1	$\mathrm{CAI \cdot EN \cdot \overline{DNUP}}$
0	0	1	x	x	x	x	x	↑	0	$\mathrm{CAI \cdot EN \cdot DNUP}$
0	0	0	1	d	x	x	x	↑	d	*
0	0	0	0	x	0	x	x	x	Q	0
0	0	0	0	x	x	0	x	↑	Q	0
0	0	0	0	x	1	1	0	↑	count up	**
0	0	0	0	x	1	1	1	↑	count down	**

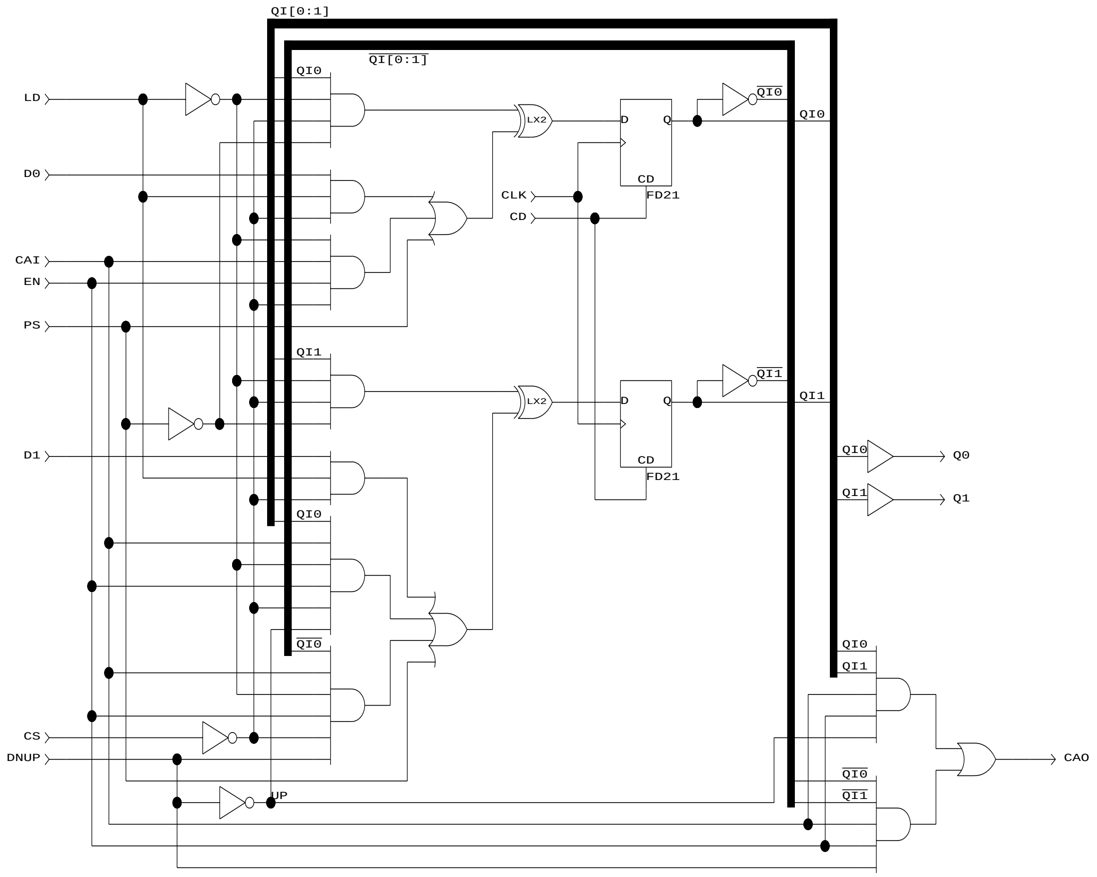
* CBUD1: $\mathrm{CAO = CAI \cdot EN \cdot (DNUP \cdot \overline{D0} + \overline{DNUP} \cdot D0)}$
CBUD2: $\mathrm{CAO = CAI \cdot EN \cdot (DNUP \cdot \overline{D0} \cdot \overline{D1} + \overline{DNUP} \cdot D0 \cdot D1)}$
CBUD4: $\mathrm{CAO = CAI \cdot EN \cdot (DNUP \cdot \overline{D0} \cdot \overline{D1} \cdot \overline{D2} \cdot \overline{D3} + \overline{DNUP} \cdot D0 \cdot D1 \cdot D2 \cdot D3)}$
CBUD8: $\mathrm{CAO = CAI \cdot EN \cdot (DNUP \cdot \overline{D0} \cdot \overline{D1} \cdot \overline{D2} \cdot \overline{D3} \cdot \overline{D4} \cdot \overline{D5} \cdot \overline{D6} \cdot \overline{D7} +}$
$\mathrm{\overline{DNUP} \cdot D0 \cdot D1 \cdot D2 \cdot D3 \cdot D4 \cdot D5 \cdot D6 \cdot D7)}$

** CAO = 1 after terminal count, when CAI = 1 and EN = 1.
CAI·EN = shift registers: serial input; counters: CAcadeIn, enable for multiplexors and counters,
d = any pattern of 1s and 0s on an input or set of inputs, Q = output of flip-flop or latch, ↑ = rising clock edge.

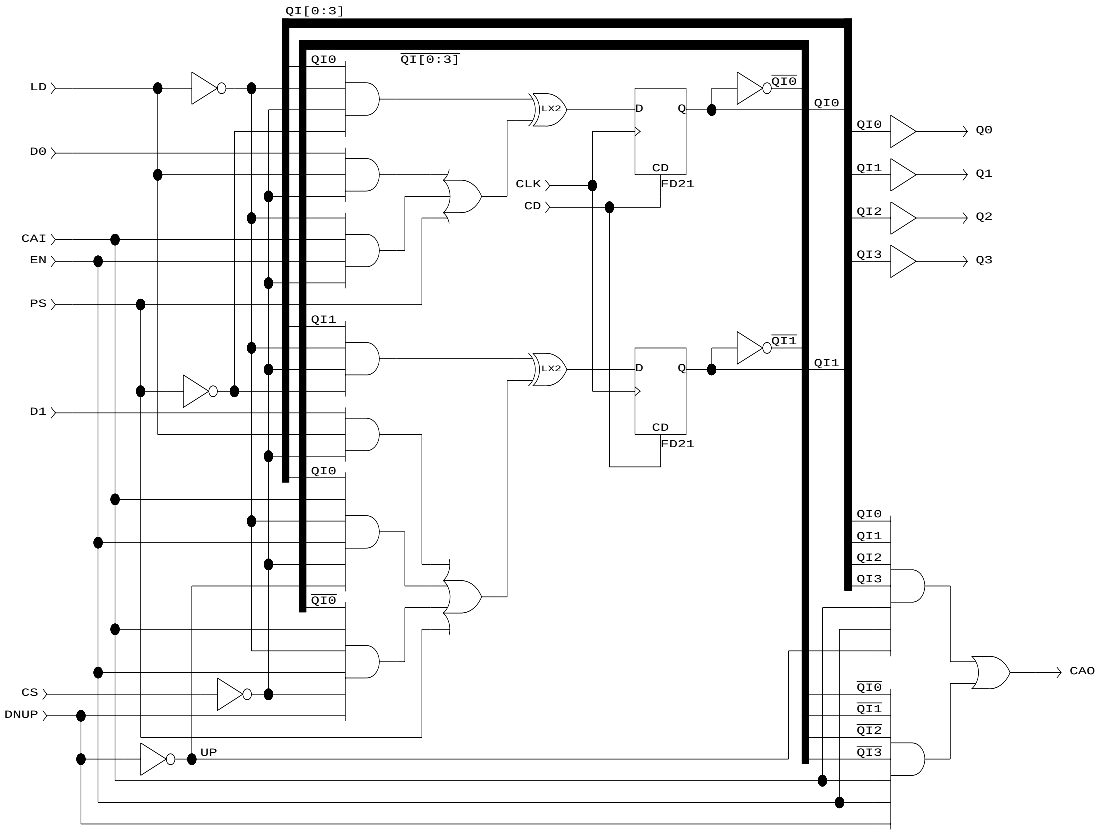
CBUD1



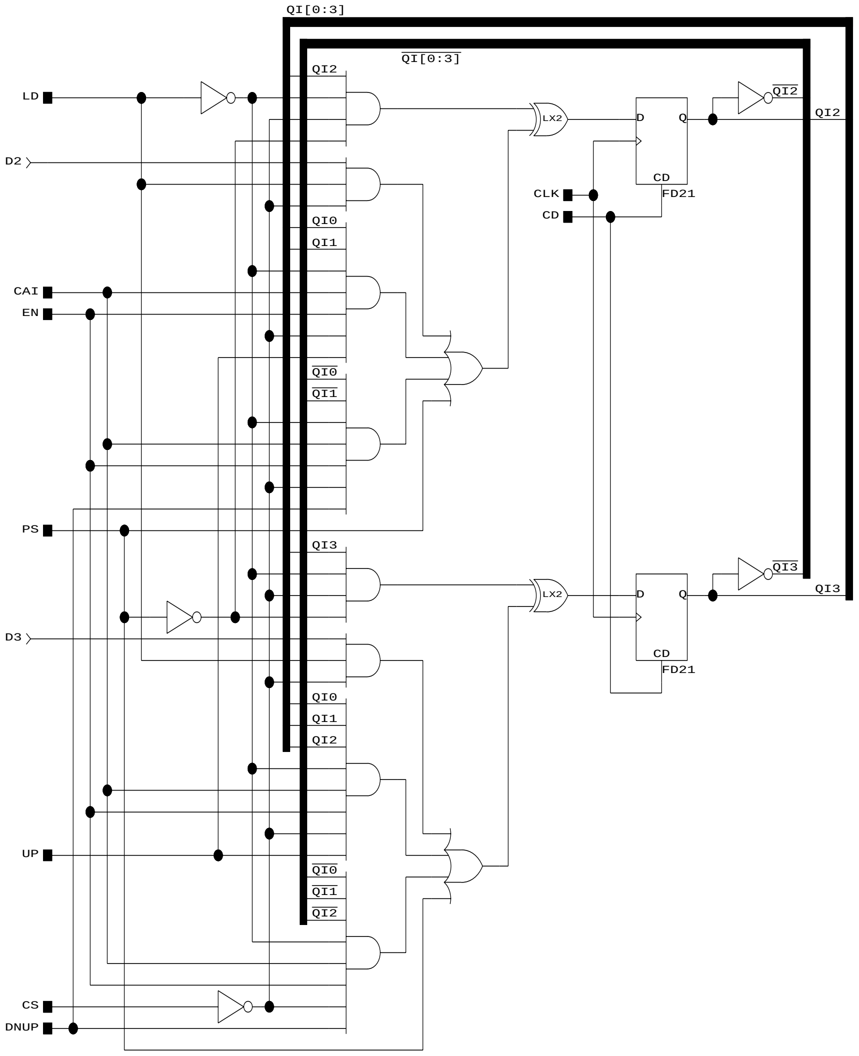
CBUD2


QI[0:1]
$\overline{QI[0:1]}$
QI0
LD
D0
CAI
EN
PS
QI1
D1
QI0
$\overline{QI0}$
CS
DNUP
UP
LX2
LX2
D
Q
CD
FD21
D
Q
CD
FD21
CLK
CD
$\overline{QI0}$
QI0
$\overline{QI1}$
QI1
QI0
Q0
QI1
Q1
QI0
QI1
$\overline{QI0}$
$\overline{QI1}$
CAO

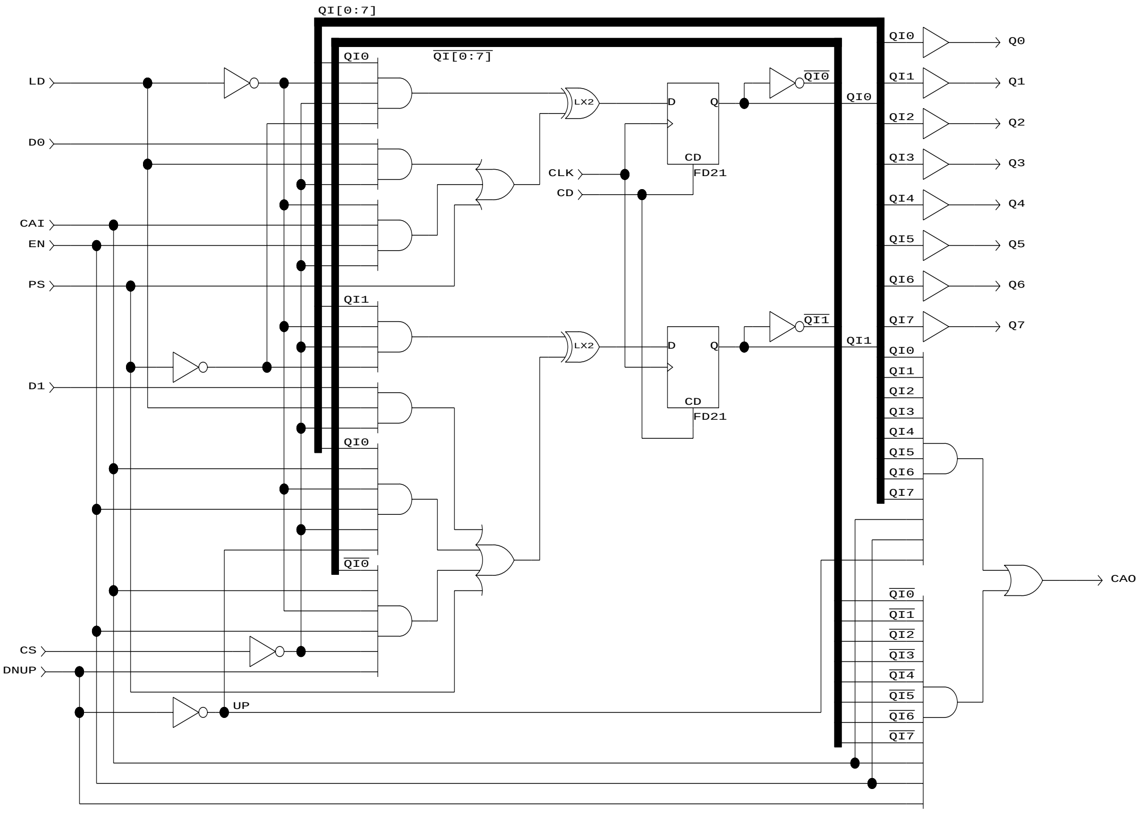
CBUD4.1


QI[0:3]
QI0
$\overline{QI[0:3]}$
LD
D0
CAI
EN
PS
D1
CS
DNUP
UP
QI1
QI0
$\overline{QI0}$
LX2
LX2
D
Q
CD
FD21
D
Q
CD
FD21
CLK
CD
$\overline{QI0}$
QI0
$\overline{QI1}$
QI1
QI0
QI1
QI2
QI3
Q0
Q1
Q2
Q3
QI0
QI1
QI2
QI3
$\overline{QI0}$
$\overline{QI1}$
$\overline{QI2}$
$\overline{QI3}$
CAO

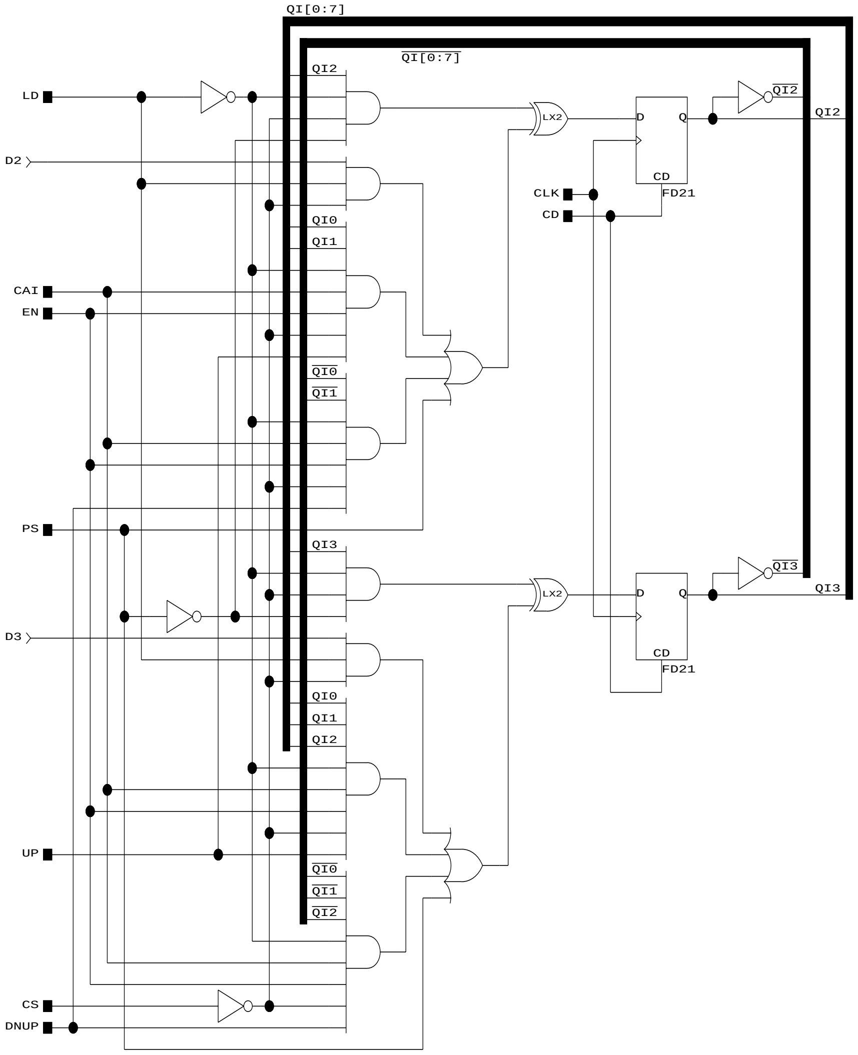
CBUD4.2


QI[0:3]
$\overline{QI[0:3]}$
QI2
LD
D2
QI0
QI1
CAI
EN
$\overline{QI0}$
$\overline{QI1}$
PS
QI3
D3
QI0
QI1
QI2
UP
$\overline{QI0}$
$\overline{QI1}$
$\overline{QI2}$
CS
DNUP
LX2
D
Q
CD
FD21
CLK
CD
$\overline{QI2}$
QI2
LX2
D
Q
CD
FD21
$\overline{QI3}$
QI3

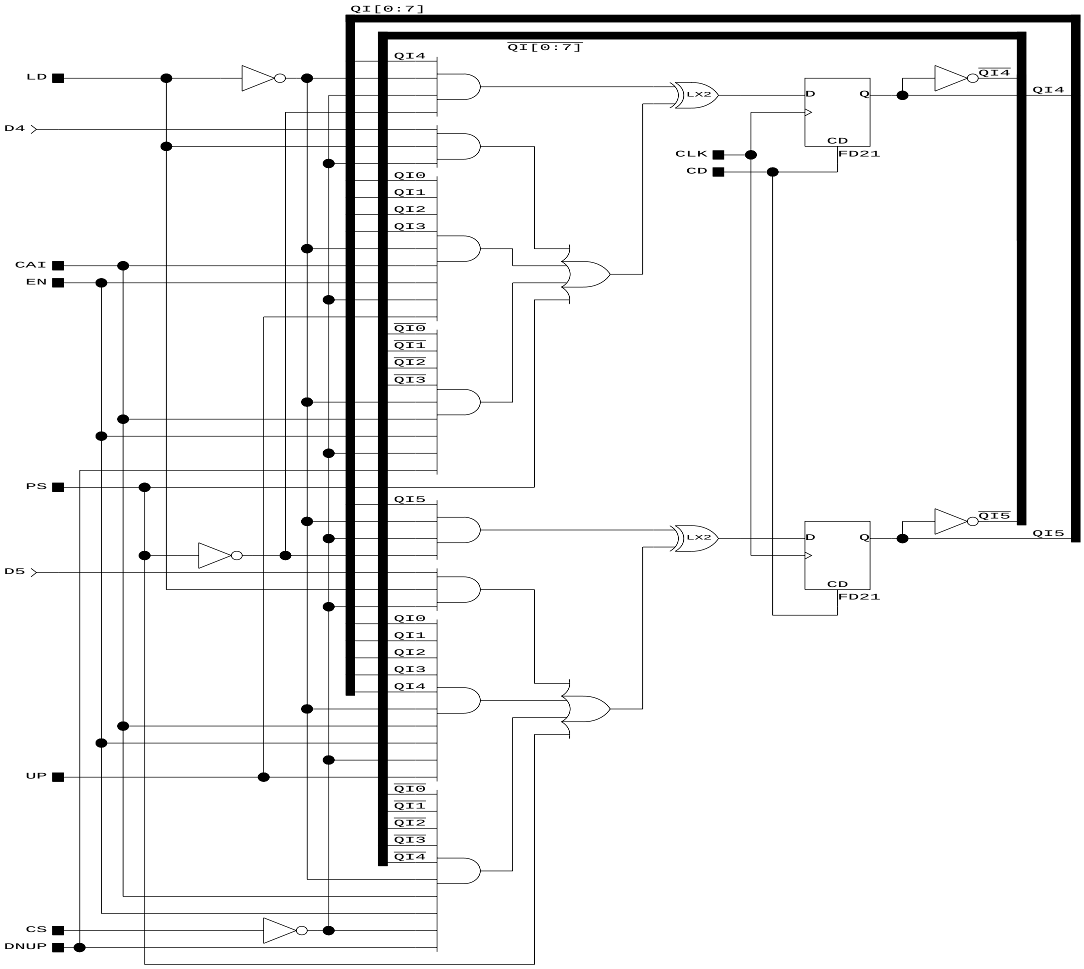
CBUD8.1


QI[0:7]
QI0
$\overline{QI[0:7]}$
LD
D0
CAI
EN
PS
QI1
D1
QI0
$\overline{QI0}$
CS
DNUP
UP
LX2
D
Q
CD
FD21
CLK
CD
$\overline{QI0}$
QI0
LX2
D
Q
CD
FD21
$\overline{QI1}$
QI1
QI0
QI1
QI2
QI3
QI4
QI5
QI6
QI7
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
QI0
QI1
QI2
QI3
QI4
QI5
QI6
QI7
CAO
$\overline{QI0}$
$\overline{QI1}$
$\overline{QI2}$
$\overline{QI3}$
$\overline{QI4}$
$\overline{QI5}$
$\overline{QI6}$
$\overline{QI7}$

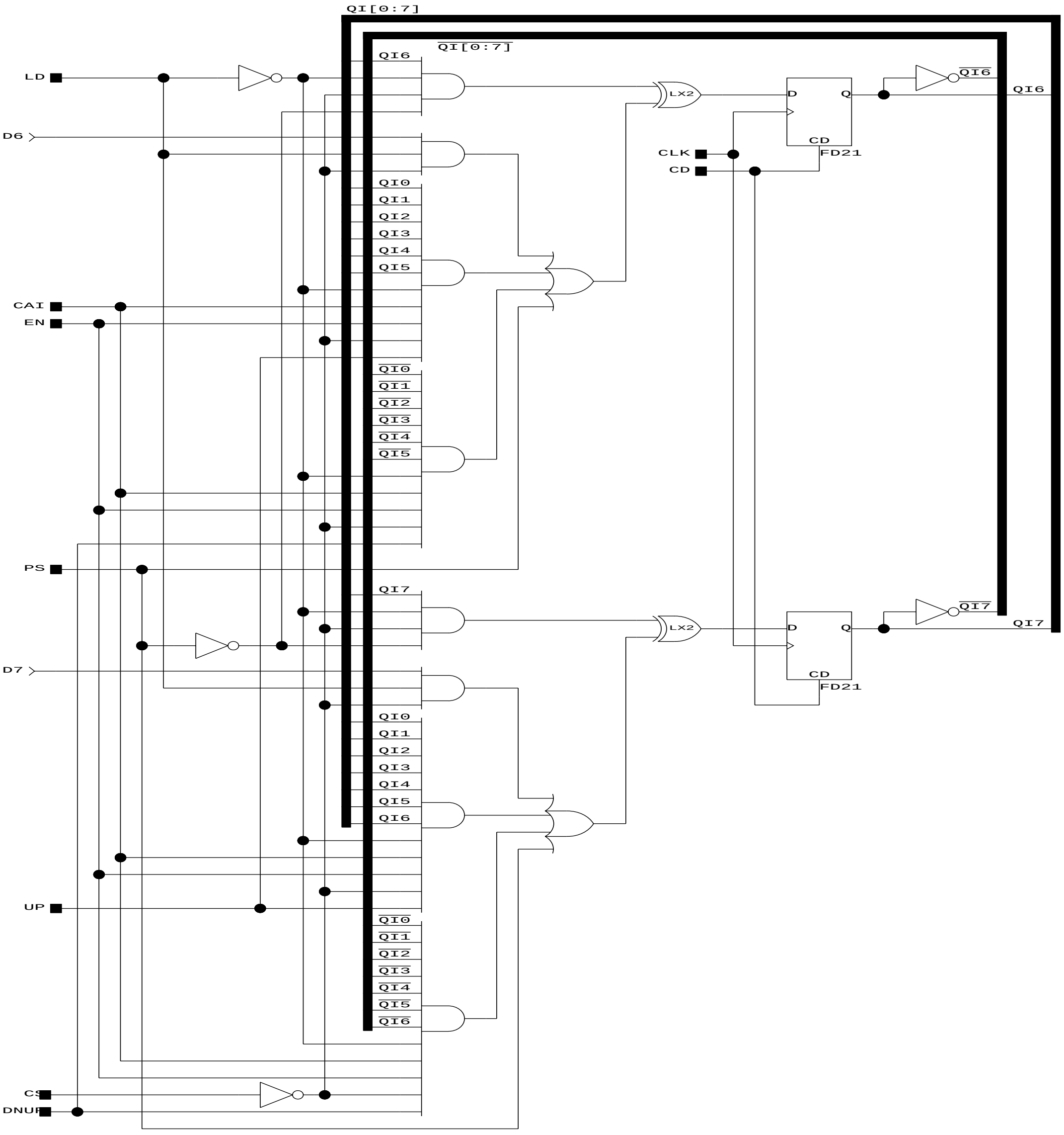
CBUD8.2


QI[0:7]
$\overline{QI[0:7]}$
QI2
LD
D2
QI0
QI1
CAI
EN
$\overline{QI0}$
$\overline{QI1}$
PS
QI3
D3
QI0
QI1
QI2
UP
$\overline{QI0}$
$\overline{QI1}$
$\overline{QI2}$
CS
DNUP
LX2
D
Q
CD
FD21
CLK
CD
$\overline{QI2}$
QI2
LX2
D
Q
CD
FD21
$\overline{QI3}$
QI3

CBUD8.3


QI[0:7]
QI[0:7]
LD
D4
CAI
EN
PS
D5
UP
CS
DNUP
QI4
QI0
QI1
QI2
QI3
QI5
LX2
D
Q
CD
FD21
CLK
CD
QI4
QI5

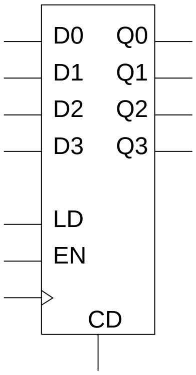
CBUD8.4


QI[0:7]
$\overline{QI[0:7]}$
QI6
LD
D6
LX2
D
Q
CD
FD21
$\overline{QI6}$
QI6
CLK
CD
QI0
QI1
QI2
QI3
QI4
QI5
CAI
EN
$\overline{QI0}$
$\overline{QI1}$
$\overline{QI2}$
$\overline{QI3}$
$\overline{QI4}$
$\overline{QI5}$
PS
QI7
D7
LX2
D
Q
CD
FD21
$\overline{QI7}$
QI7
QI0
QI1
QI2
QI3
QI4
QI5
QI6
UP
$\overline{QI0}$
$\overline{QI1}$
$\overline{QI2}$
$\overline{QI3}$
$\overline{QI4}$
$\overline{QI5}$
$\overline{QI6}$
CS
DNUP

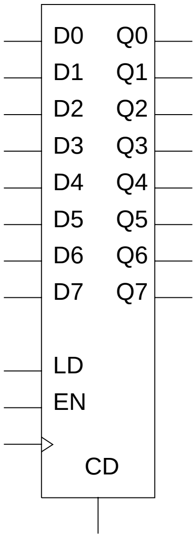
Decade Counters

CDD14 and CDD18

CDD14



CDD18



Function:

4- and 8-bit decade down counters with asynchronous clear, enable, and parallel data load.

Availability:

CDD14 and CDD18 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Schematics appear on the following pages.

Type: Hard

Logic Resources:

Macro	PT	GLB	Output	Level
CDD14	*	2	4	1
CDD18	**	4	8	1

* CLK: 1 PT per GLB if Product Term Clock is used.
CD: 1 PT per GLB.
Q0: 5 PT Q1: 6 PT Q2: 5 PT Q3: 5 PT

** CLK: 1 PT per GLB if Product Term Clock is used.
CD: 1 PT per GLB.
Q0: 5 PT Q1: 6 PT Q2: 5 PT Q3: 5 PT
Q4: 6 PT Q5: 6 PT Q6: 5 PT Q7: 5 PT

Macro Port Definition:

```
CDD14 ([Q0..Q3],[D0..D3],CLK,LD,EN,CD);
  CDD14_1 ([Q0..Q2],[D0..D2],Q3,CLK,LD,EN,CD);
  CDD14_2 (Q3,D3,[Q0..Q2],CLK,LD,EN,CD);
CDD18 ([Q0..Q7],[D0..D7],CLK,LD,EN,CD);
  CDD18_1 ([Q0..Q2],[D0..D2],Q3,CLK,LD,EN,CD);
  CDD18_2 ([Q3..Q5],[D3..D5],[Q0..Q2],Q6,Q7,CLK,LD,EN,CD);
  CDD18_3 (Q6,Q7,D6,D7,[Q0..Q5],CLK,LD,EN,CD);
```

Counting Ranges:

CDD14: 9-0. CDD18: 99-0.

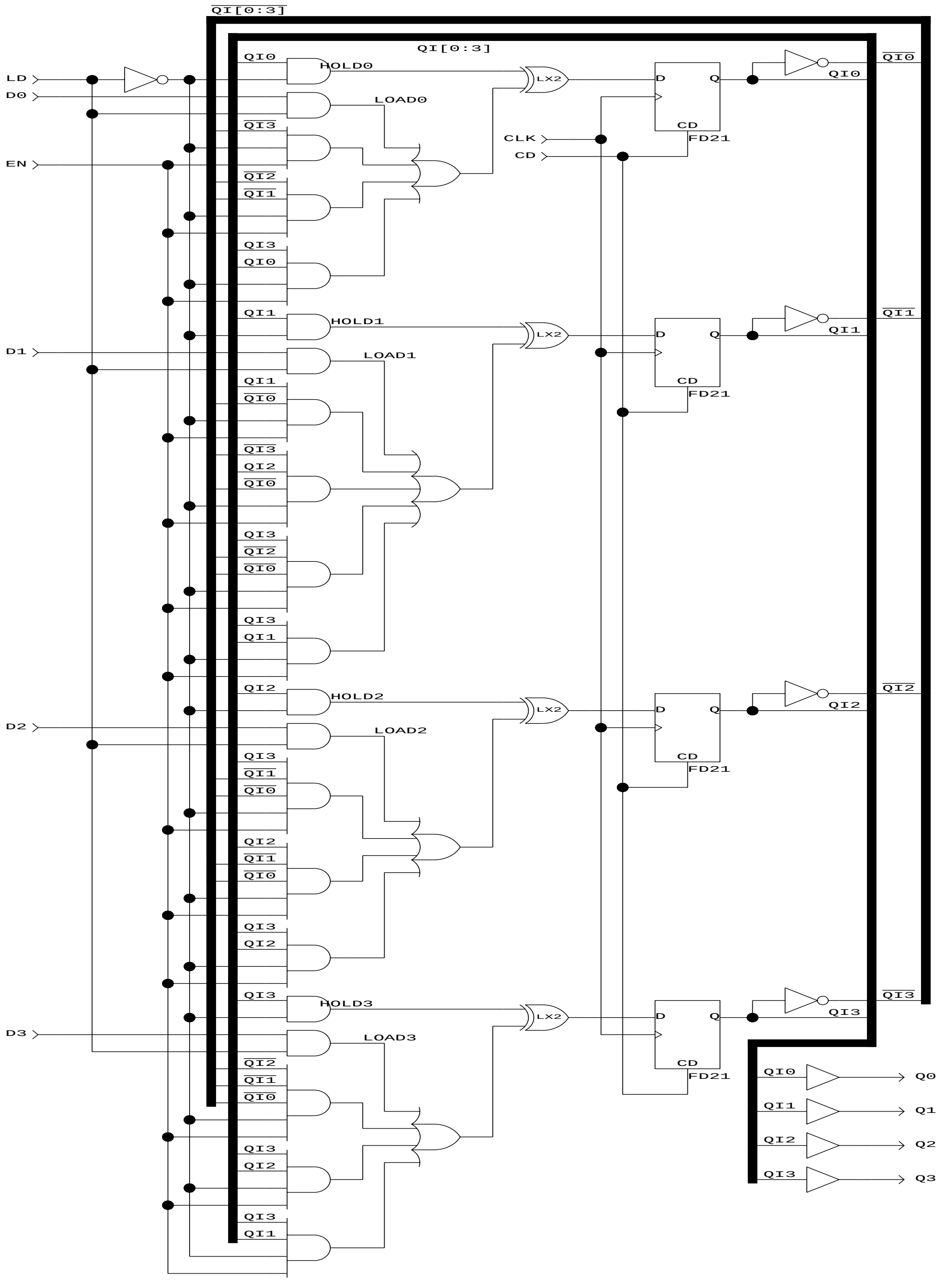
Truth Table:

The truth table is the same for both CDD1s.

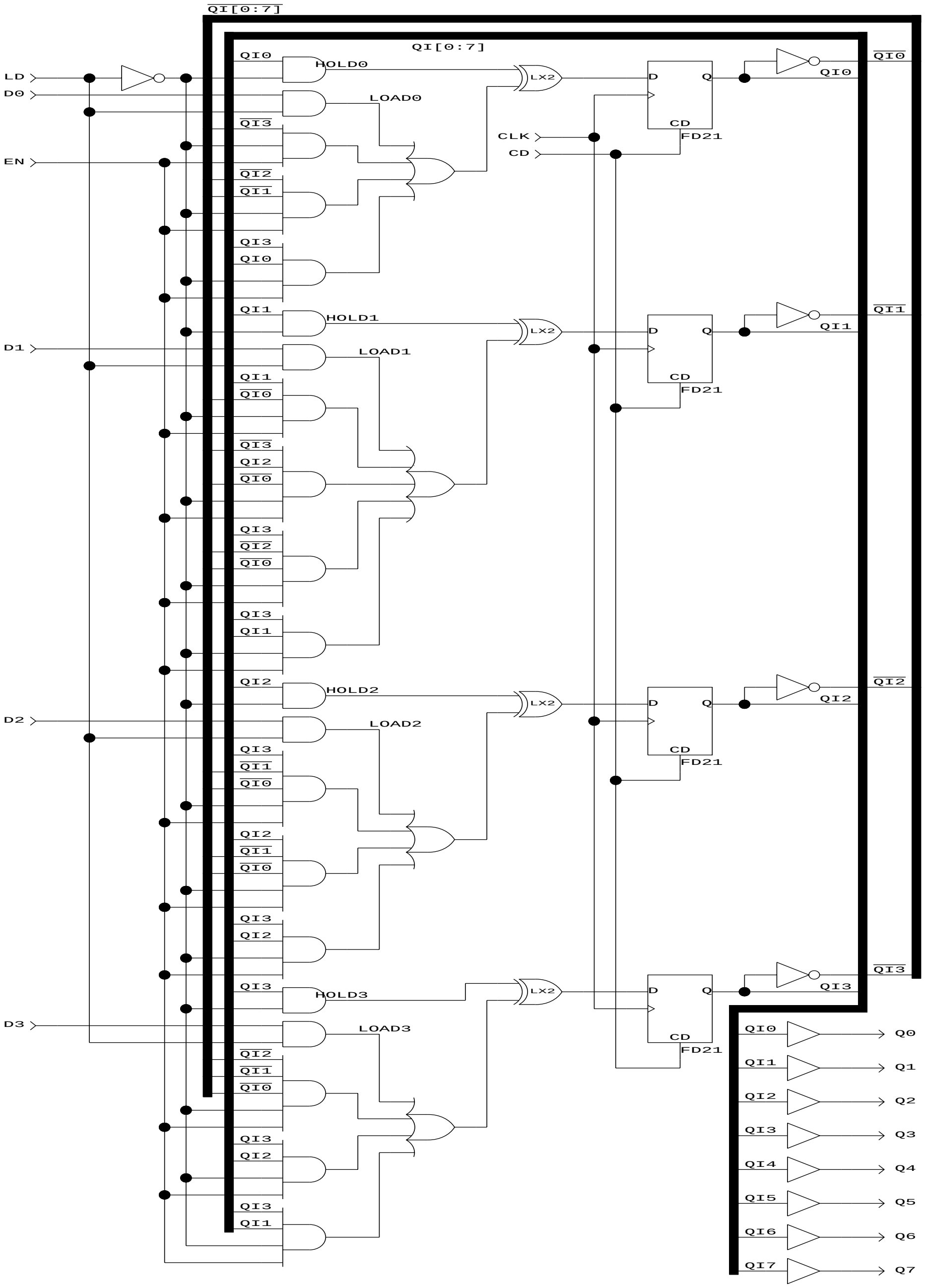
Input					Output
CD	**LD**	**D**	**EN**	**CLK**	**Q**
1	x	x	x	x	0
0	1	d	x	↑	d
0	0	x	0	x	Q
0	0	x	1	↑	count down

Valid states for each 4-bit digit are 0-9.
Loading higher hexadecimal input values (A-F)
clears that decimal output digit on the next clock pulse.
d = any pattern of 1s and 0s on an input or set of inputs,
Q = output of flip-flop or latch, x = don't care,
↑ = rising clock edge.

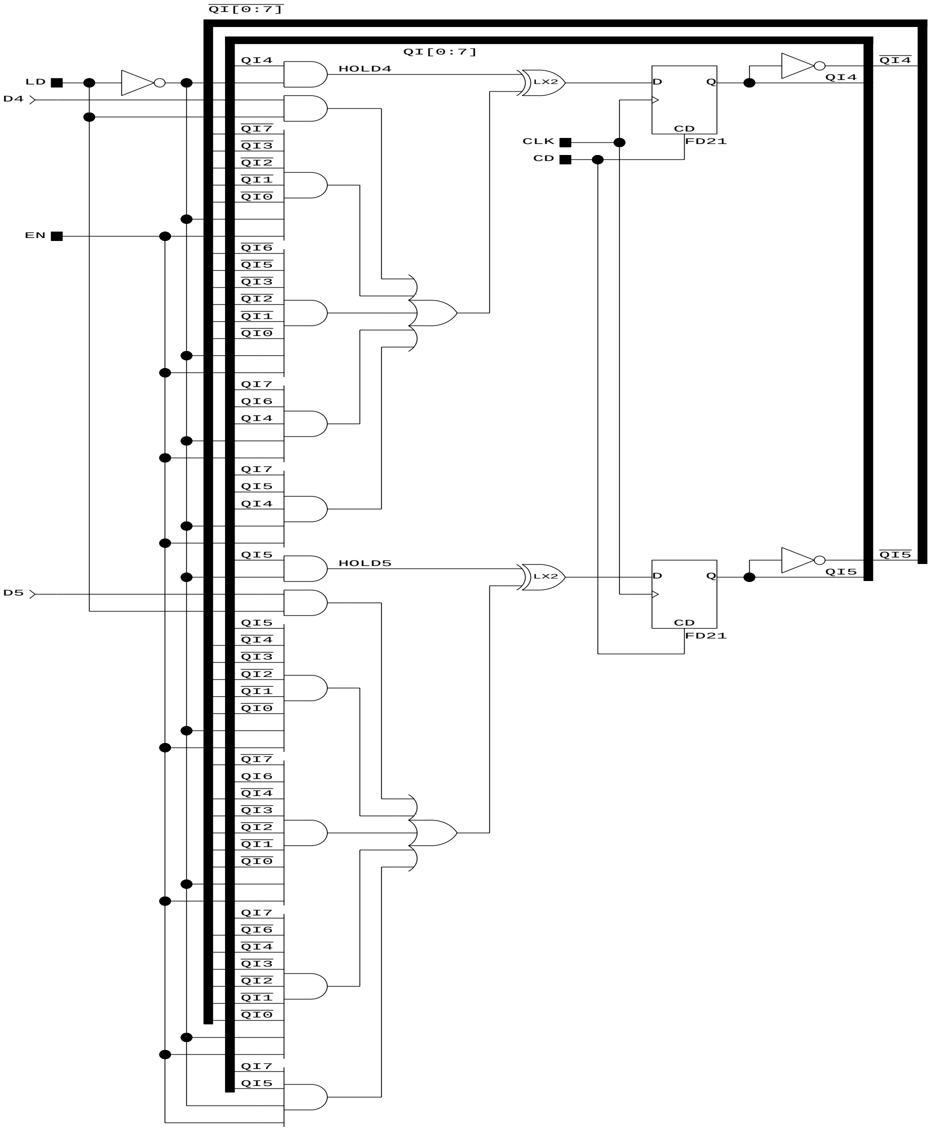
CDD14


$\overline{QI[0:3]}$
QI[0:3]
QI0
HOLD0
LX2
D
Q
$\overline{QI0}$
QI0
LD
D0
LOAD0
$\overline{QI3}$
CD
FD21
CLK
CD
EN
$\overline{QI2}$
$\overline{QI1}$
QI3
QI0
QI1
HOLD1
LX2
D
Q
$\overline{QI1}$
QI1
D1
LOAD1
CD
FD21
QI1
$\overline{QI0}$
$\overline{QI3}$
QI2
$\overline{QI0}$
QI3
$\overline{QI2}$
$\overline{QI0}$
QI3
QI1
QI2
HOLD2
LX2
D
Q
$\overline{QI2}$
QI2
D2
LOAD2
QI3
$\overline{QI1}$
$\overline{QI0}$
CD
FD21
QI2
$\overline{QI1}$
$\overline{QI0}$
QI3
QI2
QI3
HOLD3
LX2
D
Q
$\overline{QI3}$
QI3
D3
LOAD3
CD
FD21
$\overline{QI2}$
$\overline{QI1}$
$\overline{QI0}$
QI0
Q0
QI1
Q1
QI2
Q2
QI3
Q3
QI3
QI2
QI3
QI1

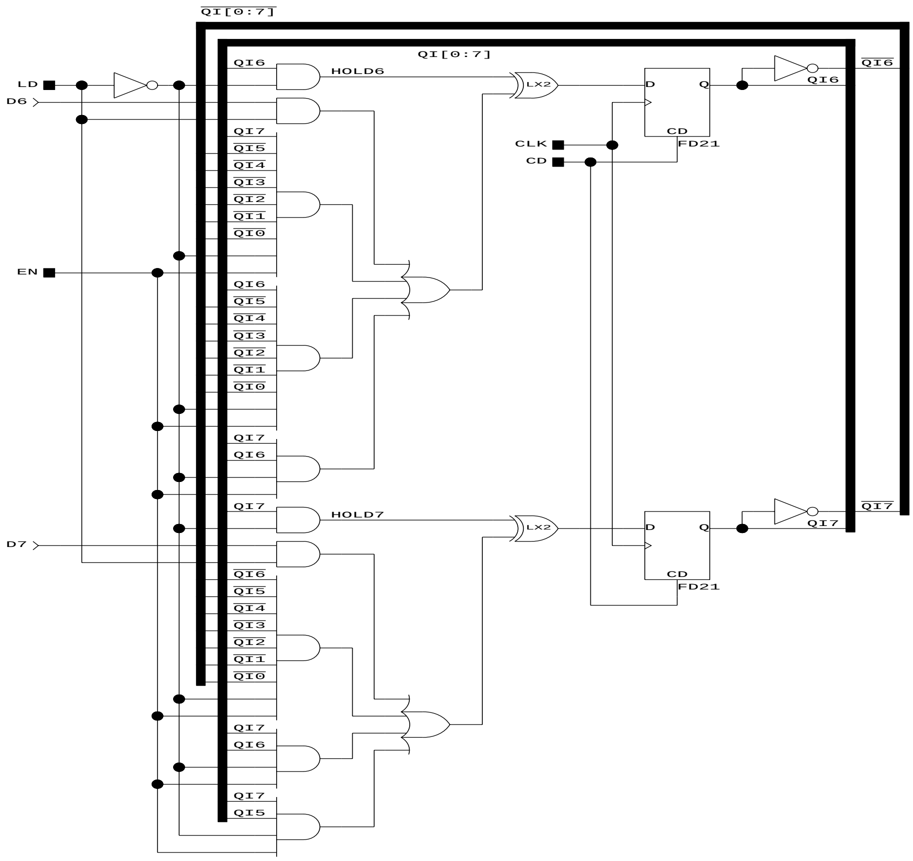
CDD18.1


QI[0:7]
QI[0:7]
LD
D0
EN
D1
D2
D3
CLK
CD
QI0
QI1
QI2
QI3
HOLD0
LOAD0
HOLD1
LOAD1
HOLD2
LOAD2
HOLD3
LOAD3
LX2
D
Q
CD
FD21
QI4
QI5
QI6
QI7
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7

CDD18.2

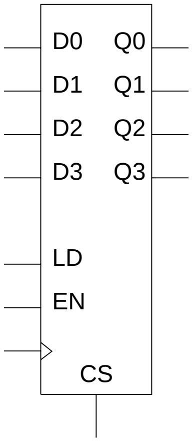

QI[0:7]
QI[0:7]
LD
D4
EN
D5
CLK
CD
HOLD4
HOLD5
LX2
LX2
D
Q
CD
FD21
D
Q
CD
FD21
QI4
QI4
QI5
QI5
QI4
QI7
QI3
QI2
QI1
QI0
QI6
QI5
QI3
QI2
QI1
QI0
QI7
QI6
QI4
QI7
QI5
QI4
QI5
QI5
QI4
QI3
QI2
QI1
QI0
QI7
QI6
QI4
QI3
QI2
QI1
QI0
QI7
QI6
QI4
QI3
QI2
QI1
QI0
QI7
QI5

CDD18.3

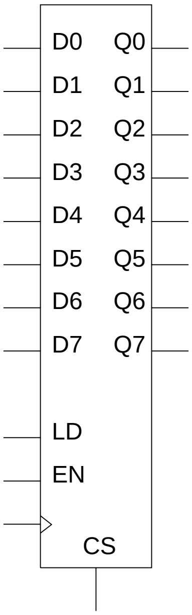

QI[0:7]
QI[0:7]
QI6
HOLD6
LX2
D
Q
CD
FD21
QI6
QI6
LD
D6
CLK
CD
QI7
QI5
QI4
QI3
QI2
QI1
QI0
EN
QI6
QI5
QI4
QI3
QI2
QI1
QI0
QI7
QI6
QI7
HOLD7
LX2
D
Q
CD
FD21
QI7
QI7
D7
QI6
QI5
QI4
QI3
QI2
QI1
QI0
QI7
QI6
QI7
QI5

CDD24 and CDD28

CDD24



CDD28



Function:

4- and 8-bit decade down counters with synchronous clear, enable, and parallel data load.

Availability:

CDD24 and CDD28 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Schematics appear on the following pages.

Type: Hard

Logic Resources:

Macro	PT	GLB	Output	Level
CDD24	*	2	4	1
CDD28	**	3	8	1

* CLK: 1 PT per GLB if Product Term Clock is used.
Q0: 5 PT Q1: 6 PT Q2: 5 PT Q3: 5 PT
** CLK: 1 PT per GLB if Product Term Clock is used.
Q0: 5 PT Q1: 6 PT Q2: 5 PT Q3: 5 PT
Q4: 6 PT Q5: 6 PT Q6: 5 PT Q7: 5 PT

Macro Port Definition:

```
CDD24 ([Q0..Q3],[D0..D3],CLK,LD,EN,CS);
  CDD24_1 ([Q0..Q2],[D0..D2],Q3,CLK,LD,EN,CS);
  CDD24_2 (Q3,D3,[Q0..Q2],CLK,LD,EN,CS);
CDD28 ([Q0..Q7],[D0..D7],CLK,LD,EN,CS);
  CDD28_1 ([Q0..Q2],[D0..D2],Q3,CLK,LD,EN,CS);
  CDD28_2 ([Q3..Q5],[D3..D5],[Q0..Q2],Q6,Q7,CLK,LD,EN,CS);
  CDD28_3 (Q6,Q7,D6,D7,[Q0..Q5],CLK,LD,EN,CS);
```

Counting Ranges:

CDD24: 9-0. CDD28: 99-0.

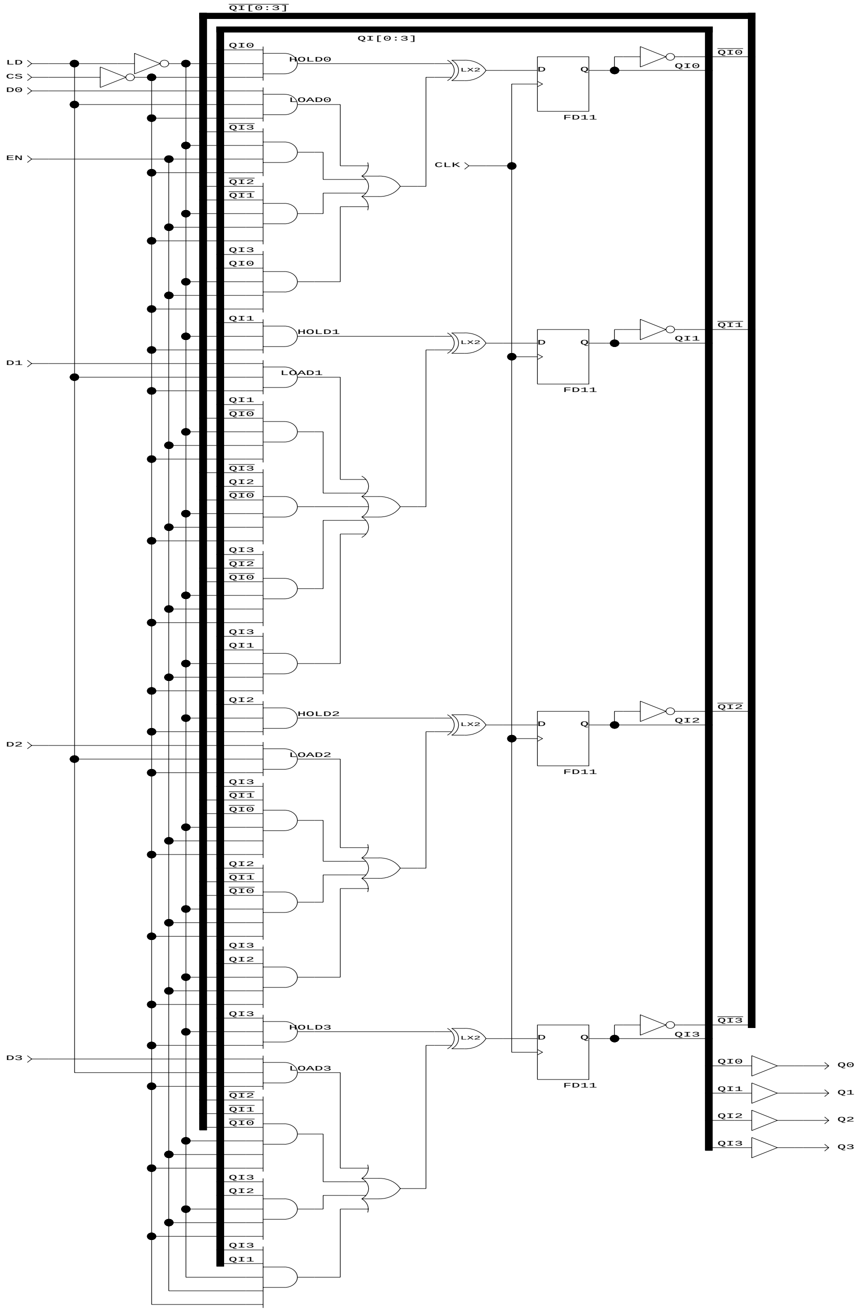
Truth Table:

The truth table is the same for both CDD2s.

Input					Output
CS	**LD**	**D**	**EN**	**CLK**	**Q**
1	x	x	x	↑	0
0	1	d	x	↑	d
0	0	x	0	x	Q
0	0	x	1	↑	count down

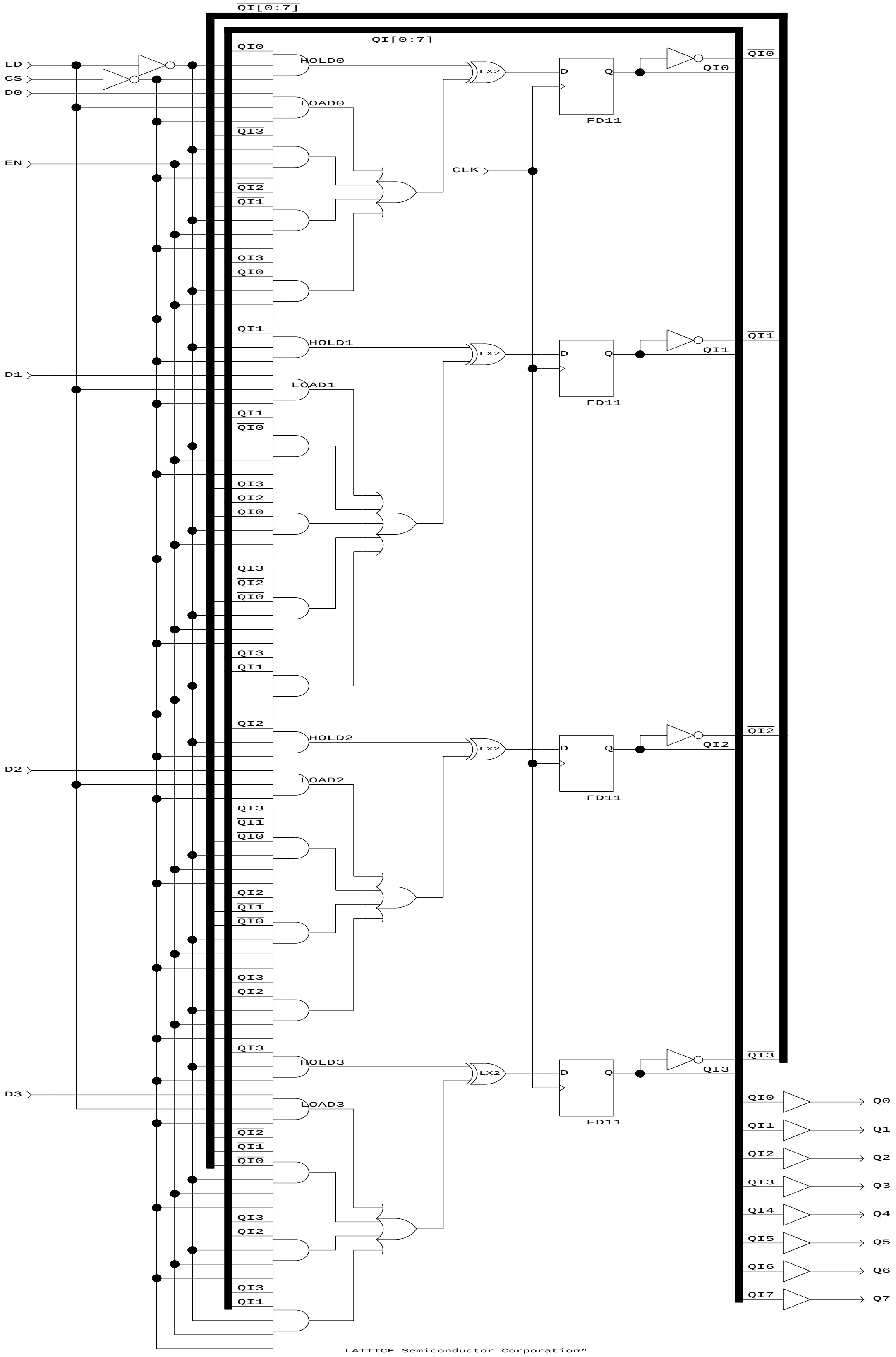
Valid states for each 4-bit digit are 0-9.
Loading higher hexadecimal input values (A-F)
clears that decimal output digit on the next clock pulse.
d = any pattern of 1s and 0s on an input or set of inputs,
Q = output of flip-flop or latch, x = don’t care,
↑ = rising clock edge.

CDD24

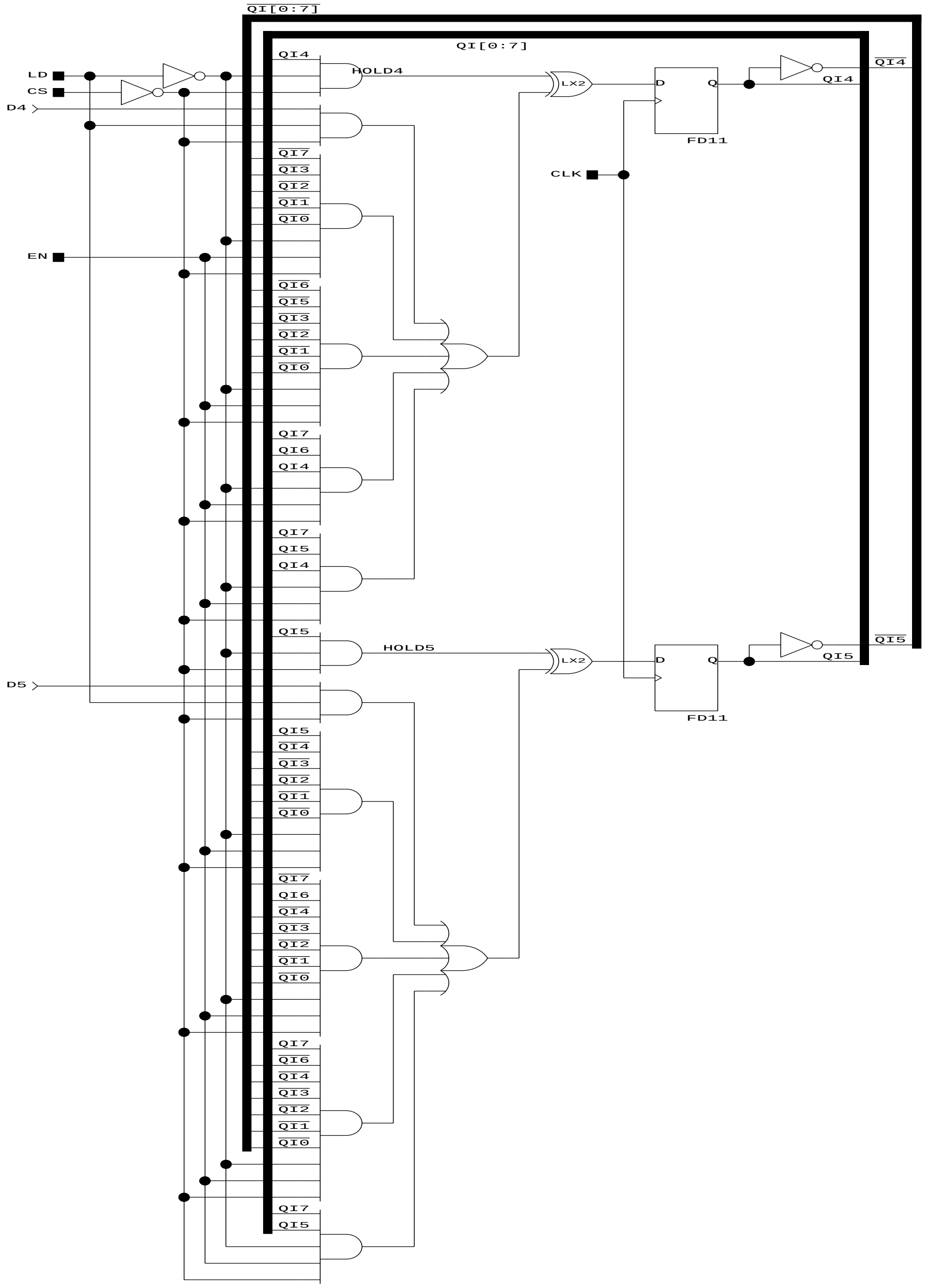


$\overline{QI[0:3]}$
QI[0:3]
LD
CS
D0
EN
CLK
D1
D2
D3
HOLD0
LOAD0
HOLD1
LOAD1
HOLD2
LOAD2
HOLD3
LOAD3
LX2
D
Q
FD11
$\overline{QI0}$
QI0
$\overline{QI1}$
QI1
$\overline{QI2}$
QI2
$\overline{QI3}$
QI3
Q0
Q1
Q2
Q3

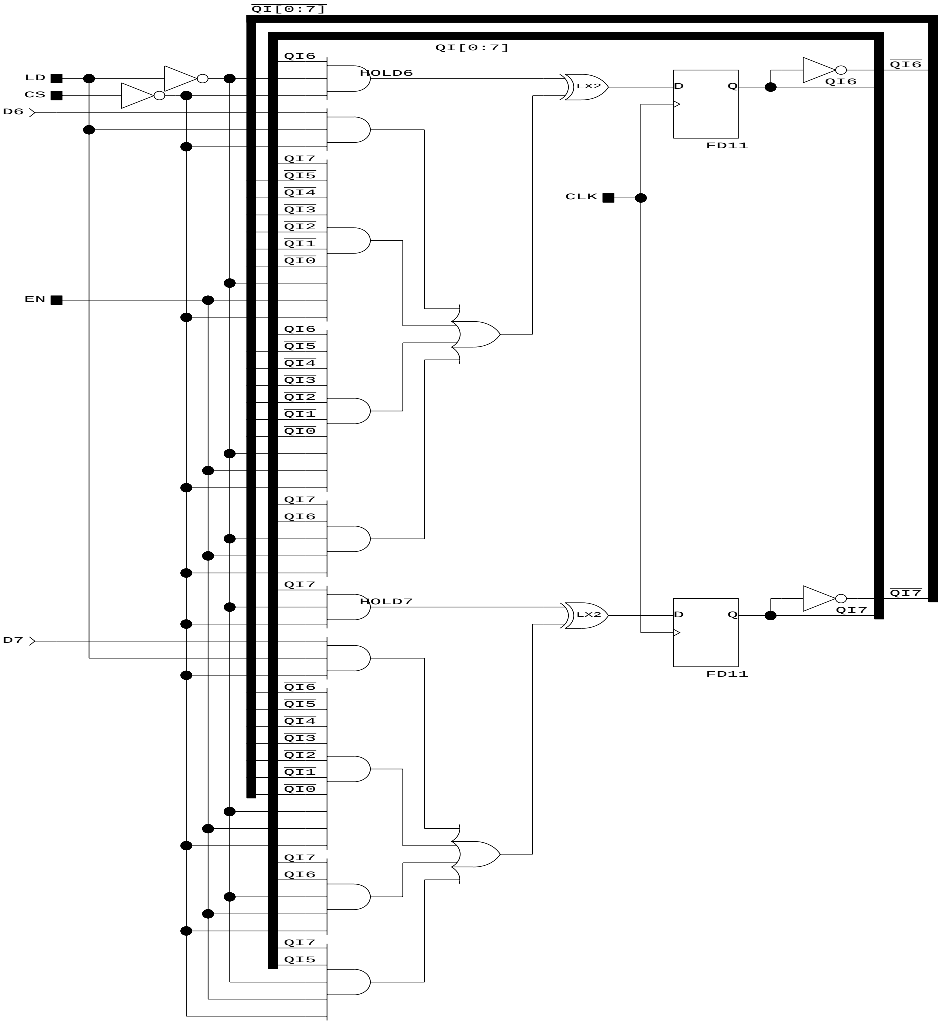
CDD28.1


QI[0:7]
QI[0:7]
LD
CS
D0
EN
D1
D2
D3
CLK
QI0
QI1
QI2
QI3
HOLD0
LOAD0
HOLD1
LOAD1
HOLD2
LOAD2
HOLD3
LOAD3
LX2
D
Q
FD11
QI0
QI1
QI2
QI3
QI4
QI5
QI6
QI7
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
LATTICE Semiconductor Corporation™

CDD28.2

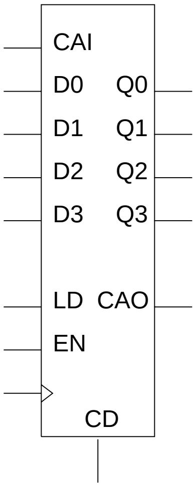

QI[0:7]
QI[0:7]
LD
CS
D4
QI4
HOLD4
LX2
D
Q
FD11
QI4
QI4
CLK
QI7
QI3
QI2
QI1
QI0
EN
QI6
QI5
QI3
QI2
QI1
QI0
QI7
QI6
QI4
QI7
QI5
QI4
QI5
HOLD5
LX2
D
Q
FD11
QI5
QI5
D5
QI5
QI4
QI3
QI2
QI1
QI0
QI7
QI6
QI4
QI3
QI2
QI1
QI0
QI7
QI6
QI4
QI3
QI2
QI1
QI0
QI7
QI5

CDD28.3

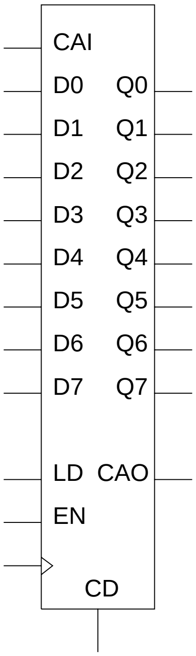

$\overline{QI[0:7]}$
QI[0:7]
LD
CS
D6
QI6
HOLD6
LX2
D
Q
FD11
$\overline{QI6}$
QI6
CLK
QI7
$\overline{QI5}$
$\overline{QI4}$
$\overline{QI3}$
$\overline{QI2}$
$\overline{QI1}$
$\overline{QI0}$
EN
QI6
$\overline{QI5}$
$\overline{QI4}$
$\overline{QI3}$
$\overline{QI2}$
$\overline{QI1}$
$\overline{QI0}$
$\overline{QI7}$
QI6
QI7
HOLD7
LX2
D
Q
FD11
$\overline{QI7}$
QI7
D7
$\overline{QI6}$
$\overline{QI5}$
$\overline{QI4}$
$\overline{QI3}$
$\overline{QI2}$
$\overline{QI1}$
$\overline{QI0}$
QI7
QI6
$\overline{QI7}$
QI5

CDD34 and CDD38

CDD34



CDD38



Function:

4- and 8-bit decade down counters with asynchronous clear, enable, parallel data load, CAI, and CAO.

Availability:

CDD34 and CDD38 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Schematics appear on the following pages.

Type: Hard

Logic Resources:

Macro	PT	GLB	Output	Level
CDD34	*	2	5	1***
CDD38	**	4	9	1***

* CLK: 1 PT per GLB if Product Term Clock is used.
CAO: 1 PT CD: 1 PT per GLB.
Q0: 5 PT Q1: 6 PT
Q2: 5 PT Q3: 5 PT

** CLK: 1 PT per GLB if Product Term Clock is used.
CAO: 1 PT CD: 1 PT per GLB.
Q0: 5 PT Q1: 6 PT Q2: 5 PT
Q3: 5 PT Q4: 6 PT Q5: 6 PT
Q6: 5 PT Q7: 5 PT

* (CAO is a 2-level output).

Macro Port Definition:

```
CDD34 ([Q0..Q3],CAO,[D0..D3],CAI,CLK,LD,EN,CD);
  CDD34_1 ([Q0..Q2],[D0..D2],Q3,CAI,CLK,LD,EN,CD);
  CDD34_2 (Q3,CAO,D3,[Q0..Q2],CAI,CLK,LD,EN,CD);
CDD38 ([Q0..Q7],CAO,[D0..D7],CAI,CLK,LD,EN,CD);
  CDD38_1 ([Q0..Q2],[D0..D2],Q3,CAI,CLK,LD,EN,CD);
  CDD38_2 ([Q3..Q5],[D3..D5],[Q0..Q2],Q6,Q7,CAI,CLK,LD,EN,CD);
  CDD38_3 (Q6,Q7,CAO,D6,D7,[Q0..Q5],CAI,CLK,LD,EN,CD);
```

Counting Ranges:

CDD34: 9-0. 38: 99-0.

Truth Table:

The truth table is the same for both CDD3s.

Input						Output	
CD	**LD**	**D**	**EN**	**CAI**	**CLK**	**Q**	**CAO**
1	x	x	x	x	x	0	CAI·EN
0	1	d	x	x	↑	d	*
0	0	x	0	x	x	Q	0
0	0	x	x	0	x	Q	0
0	0	x	1	1	↑	count down	**

* CAO = CAI·EN·terminal count.

** CAO = 1 after terminal count when CAI = 1 and EN = 1.

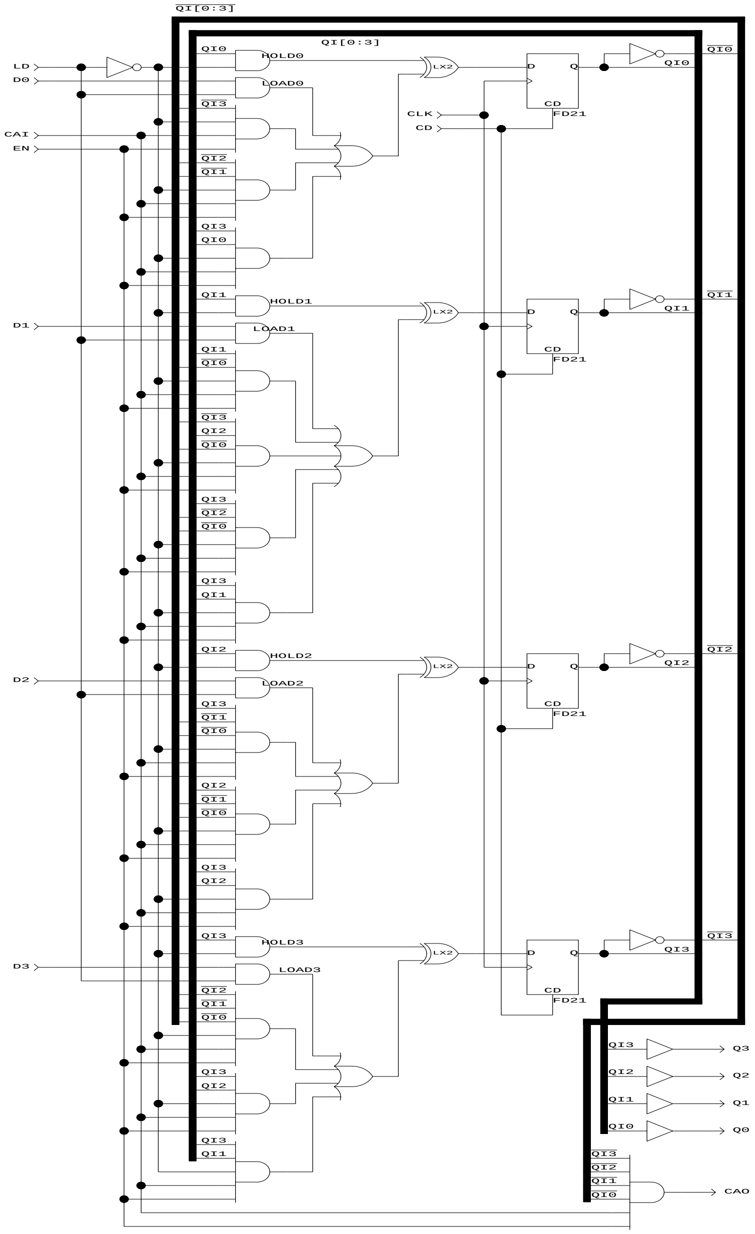
Valid states for each 4-bit digit are 0~9. Loading higher hexadecimal input values (A-F) clears that decimal output digit on the next clock pulse.

d = any pattern of 1s and 0s on an input or set of inputs,

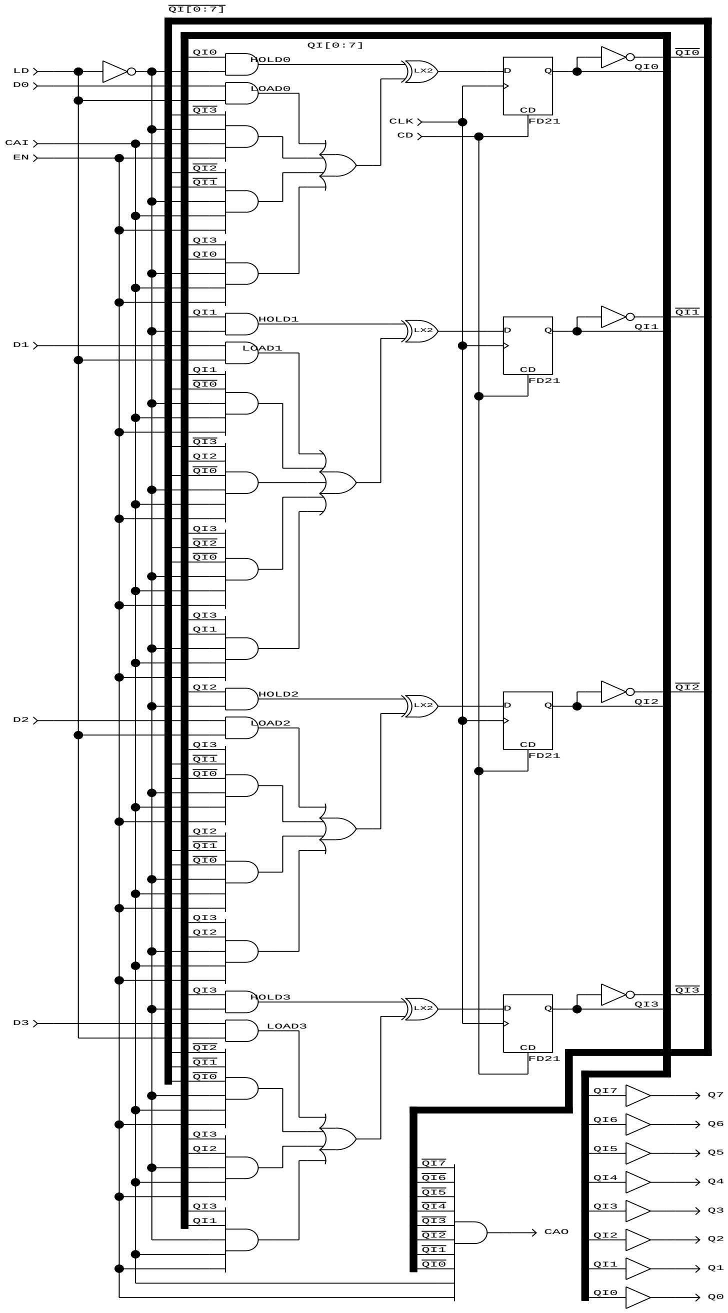
Q = output of flip-flop or latch, x = don't care,

↑ = rising clock edge.

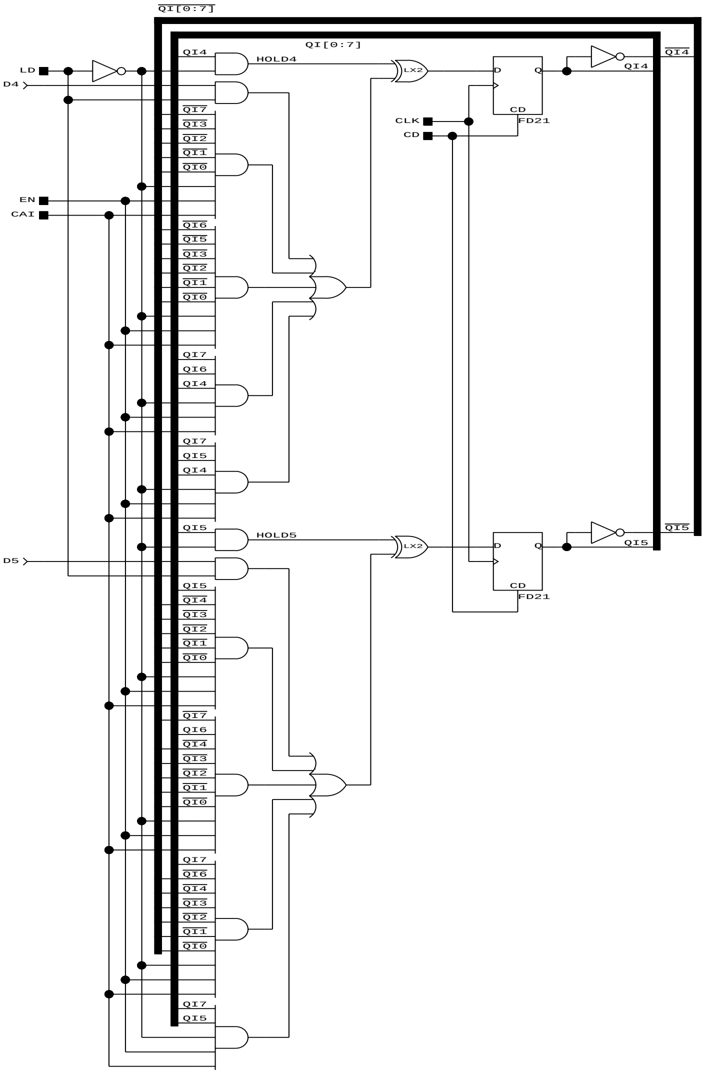
CDD34


QI[0:3]
QI[0:3]
LD
D0
CAI
EN
D1
D2
D3
CLK
CD
QI0
QI1
QI2
QI3
HOLD0
LOAD0
HOLD1
LOAD1
HOLD2
LOAD2
HOLD3
LOAD3
LX2
D
Q
CD
FD21
Q3
Q2
Q1
Q0
CA0

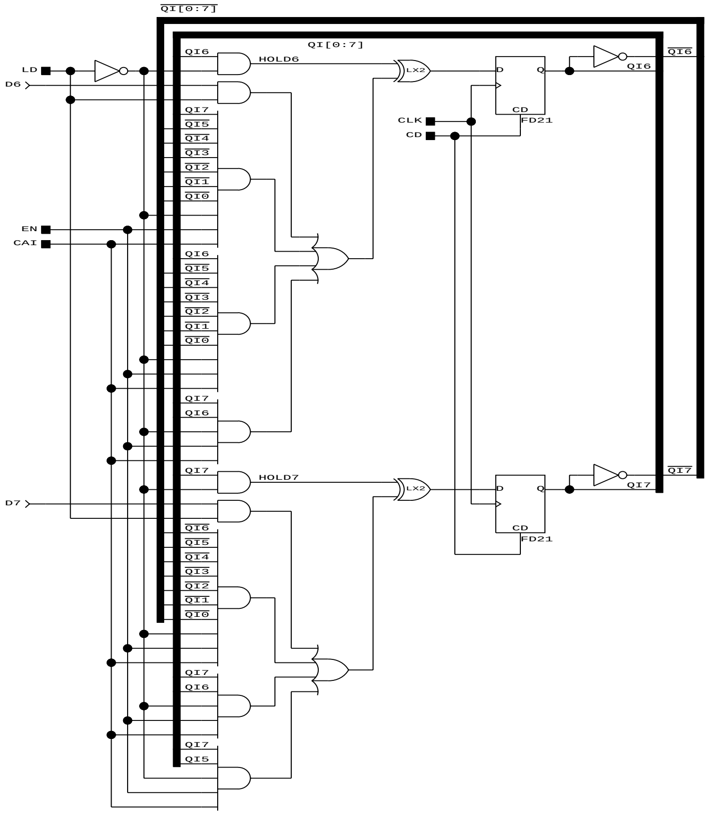
CDD38.1


QI[0:7]
QI[0:7]
LD
D0
CAI
EN
D1
D2
D3
CLK
CD
HOLD0
LOAD0
HOLD1
LOAD1
HOLD2
LOAD2
HOLD3
LOAD3
LX2
D
Q
CD
FD21
QI0
QI1
QI2
QI3
QI4
QI5
QI6
QI7
CAO
Q7
Q6
Q5
Q4
Q3
Q2
Q1
Q0

CDD38.2

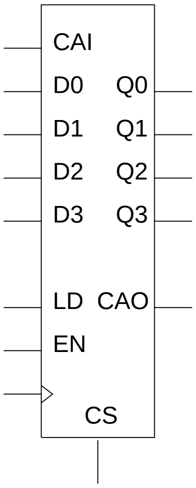

$\overline{QI[0:7]}$
QI[0:7]
LD
D4
EN
CAI
D5
HOLD4
HOLD5
LX2
D
Q
CD
FD21
CLK
CD
QI4
$\overline{QI4}$
QI5
$\overline{QI5}$
$\overline{QI7}$
$\overline{QI6}$
$\overline{QI5}$
$\overline{QI4}$
$\overline{QI3}$
$\overline{QI2}$
$\overline{QI1}$
$\overline{QI0}$
QI7
QI6
QI5
QI4

CDD38.3

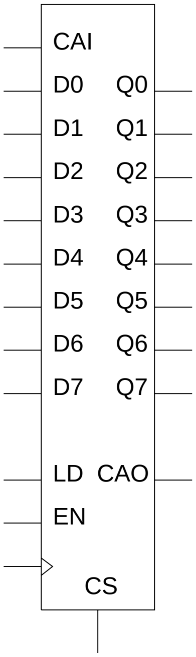

$\overline{QI[0:7]}$
QI[0:7]
LD
D6
EN
CAI
D7
QI6
HOLD6
QI7
$\overline{QI5}$
$\overline{QI4}$
$\overline{QI3}$
$\overline{QI2}$
$\overline{QI1}$
$\overline{QI0}$
QI6
$\overline{QI5}$
$\overline{QI4}$
$\overline{QI3}$
$\overline{QI2}$
$\overline{QI1}$
$\overline{QI0}$
QI7
QI6
QI7
HOLD7
$\overline{QI6}$
$\overline{QI5}$
$\overline{QI4}$
$\overline{QI3}$
$\overline{QI2}$
$\overline{QI1}$
$\overline{QI0}$
QI7
QI6
QI7
QI5
LX2
LX2
D
Q
CD
FD21
D
Q
CD
FD21
CLK
CD
$\overline{QI6}$
QI6
$\overline{QI7}$
QI7

CDD44 and CDD48

CDD44



CDD48



Function:

4- and 8-bit decade down counters with synchronous clear, enable, parallel data load, CAI, and CAO.

Availability:

CDD44 and CDD48 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Schematics appear on the following pages.

Type: Hard

Logic Resources:

Macro	PT	GLB	Output	Level
CDD44	*	2	5	1***
CDD48	**	3	9	1***

*   CLK: 1 PT per GLB if Product Term Clock is used.
CAO: 1 PT   Q0: 5 PT
Q1: 6 PT   Q2: 5 PT   Q3: 5 PT

**   CLK: 1 PT per GLB if Product Term Clock is used.
CAO: 1 PT   Q0: 5 PT
Q1: 6 PT   Q2: 5 PT   Q3: 5 PT
Q4: 6 PT   Q5: 6 PT   Q6: 5 PT   Q7: 5 PT

***   (CAO is a 2-level output).

Macro Port Definition:

```
CDD44 ([Q0..Q3],CAO,[D0..D3],CAI,CLK,LD,EN,CS);
  CDD44_1 ([Q0..Q2],[D0..D2],Q3,CAI,CLK,LD,EN,CS);
  CDD44_2 (Q3,CAO,D3,[Q0..Q2],CAI,CLK,LD,EN,CS);
CDD48 ([Q0..Q7],CAO,[D0..D7],CAI,CLK,LD,EN,CS);
  CDD48_1 ([Q0..Q2],[D0..D2],Q3,CAI,CLK,LD,EN,CS);
  CDD48_2 ([Q3..Q5],[D3..D5],[Q0..Q2],Q6,Q7,CAI,CLK,LD,
             EN,CS);
  CDD48_3 (Q6,Q7,CAO,D6,D7,[Q0..Q5],CAI,CLK,LD,EN,CS);
```

Counting Ranges:

CDD44: 9-0. 48: 99-0.

Truth Table:

The truth table is the same for both CDD4s..

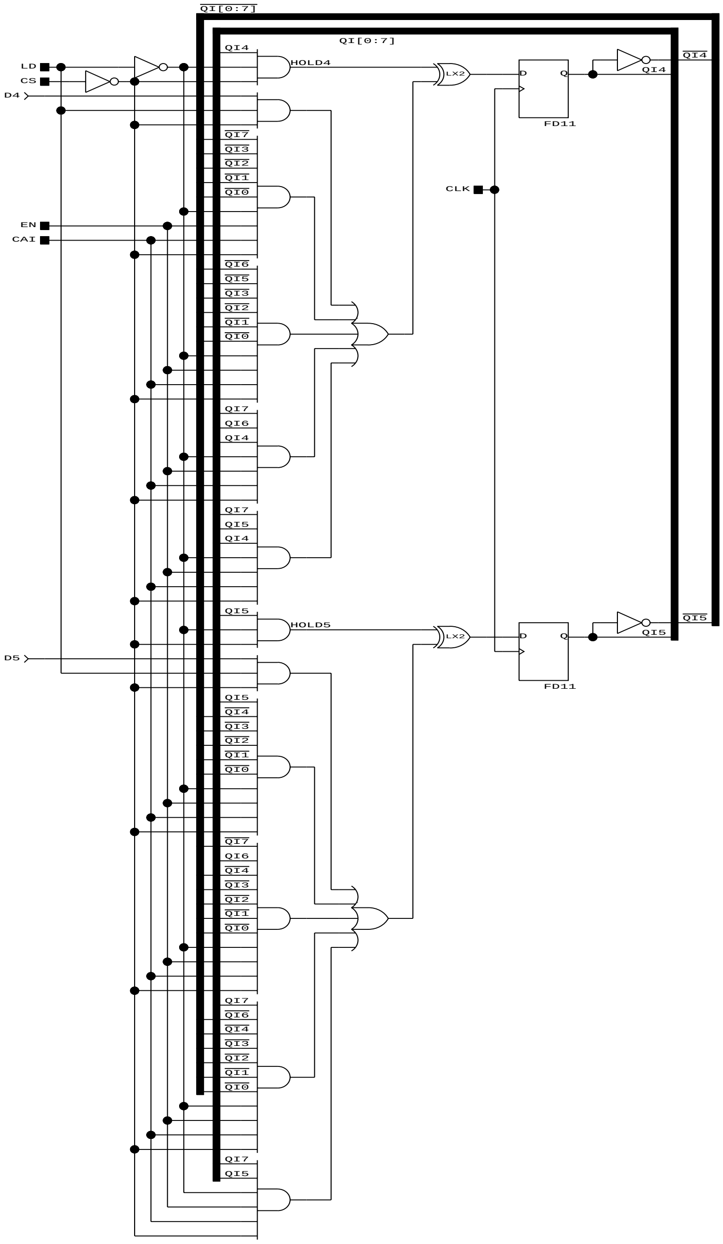
Input						Output	
CS	**LD**	**D**	**EN**	**CAI**	**CLK**	**Q**	**CAO**
1	x	x	x	x	↑	0	0
0	1	d	x	x	↑	d	*
0	0	x	0	x	x	Q	0
0	0	x	x	0	x	Q	0
0	0	x	1	1	↑	count down	**

* CAO = CAI·EN·terminal count.

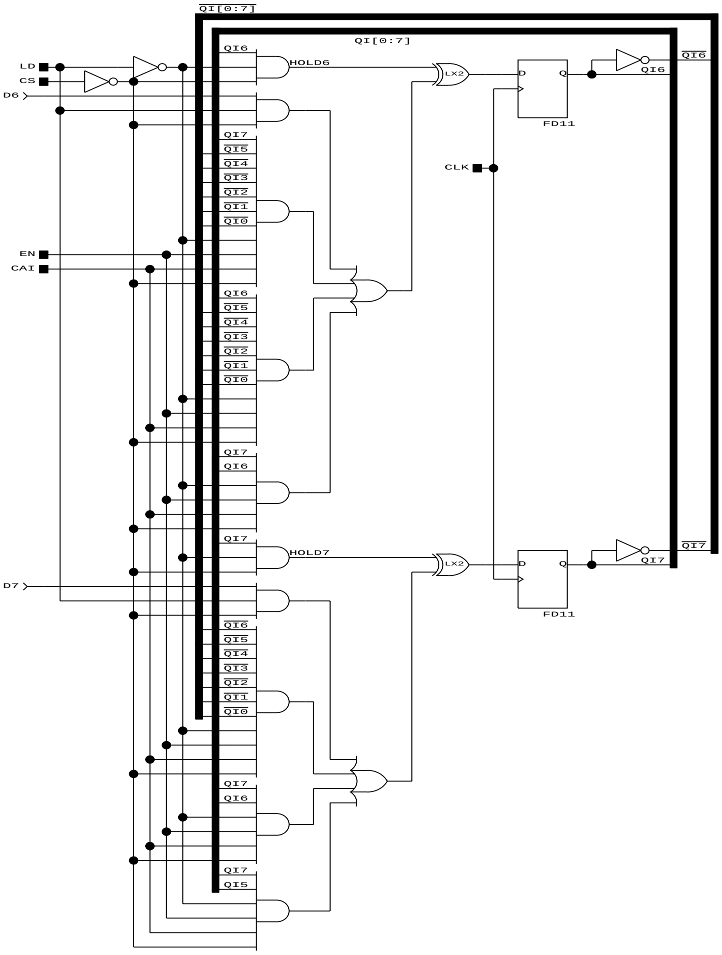
** CAO = 1 after terminal count when CAI = 1 and EN = 1.

Valid states for each 4-bit digit are 0~9. Loading higher hexadecimal input values (A-F) clears that decimal output digit on the next clock pulse.
d = any pattern of 1s and 0s on an input or set of inputs,
Q = output of flip-flop or latch, x = don’t care,
↑ = rising clock edge.

CDD48.2

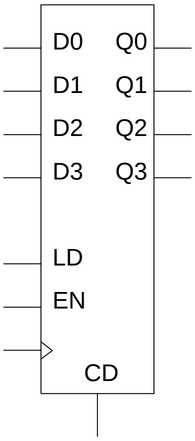

QI[0:7]
QI[0:7]
QI4
HOLD4
LD
CS
D4
LX2
D
Q
FD11
QI4
QI4
CLK
QI7
QI3
QI2
QI1
QI0
EN
CAI
QI6
QI5
QI3
QI2
QI1
QI0
QI7
QI6
QI4
QI7
QI5
QI4
QI5
HOLD5
D5
LX2
D
Q
FD11
QI5
QI5
QI5
QI4
QI3
QI2
QI1
QI0
QI7
QI6
QI4
QI3
QI2
QI1
QI0
QI7
QI6
QI4
QI3
QI2
QI1
QI0
QI7
QI5

CDD48.3

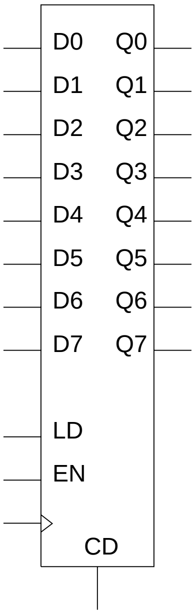

$\overline{QI[0:7]}$
QI[0:7]
LD
CS
D6
QI6
HOLD6
LX2
D
Q
FD11
$\overline{QI6}$
QI6
CLK
QI7
$\overline{QI5}$
$\overline{QI4}$
$\overline{QI3}$
$\overline{QI2}$
$\overline{QI1}$
$\overline{QI0}$
EN
CAI
QI6
$\overline{QI5}$
$\overline{QI4}$
$\overline{QI3}$
$\overline{QI2}$
$\overline{QI1}$
$\overline{QI0}$
QI7
QI6
QI7
HOLD7
LX2
D
Q
FD11
$\overline{QI7}$
QI7
D7
$\overline{QI6}$
$\overline{QI5}$
$\overline{QI4}$
$\overline{QI3}$
$\overline{QI2}$
$\overline{QI1}$
$\overline{QI0}$
QI7
QI6
QI7
QI5

CDU14 and CDU18

CDU14



CDU18



Function:

4- and 8-bit decade up counters with asynchronous clear, enable, and parallel data load.

Availability:

CDU14 and CDU18 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Schematics appear on the following pages.

Type: Hard

Logic Resources:

Macro	PT	GLB	Output	Level
CDU14	*	2	4	1
CDU18	**	3	8	1

* CLK: 1 PT per GLB if Product Term Clock is used.
CD: 1 PT per GLB.
Q0: 5 PT Q1: 4 PT Q2: 4 PT Q3: 6 PT

** CLK: 1 PT per GLB if Product Term Clock is used.
CD: 1 PT per GLB.
Q0: 5 PT Q1: 4 PT Q2: 4 PT
Q3: 6 PT Q4: 6 PT Q5: 4 PT
Q6: 4 PT Q7: 6 PT

Macro Port Definition:

```
CDU14 ([Q0..Q3],[D0..D3],CLK,LD,EN,CD);
CDU18 ([Q0..Q7],[D0..D7],CLK,LD,EN,CD);
  CDU18_1 ([Q0..Q3],[D0..D3],CLK,LD,EN,CD);
  CDU18_2 ([Q4..Q6],[D4..D6],[Q0..Q3],Q7,CLK,LD,EN,CD);
  CDU18_3 (Q7,D7,[Q0..Q6],CLK,LD,EN,CD);
```

Counting Ranges:

CDU14: 0-9. 18: 0-99.

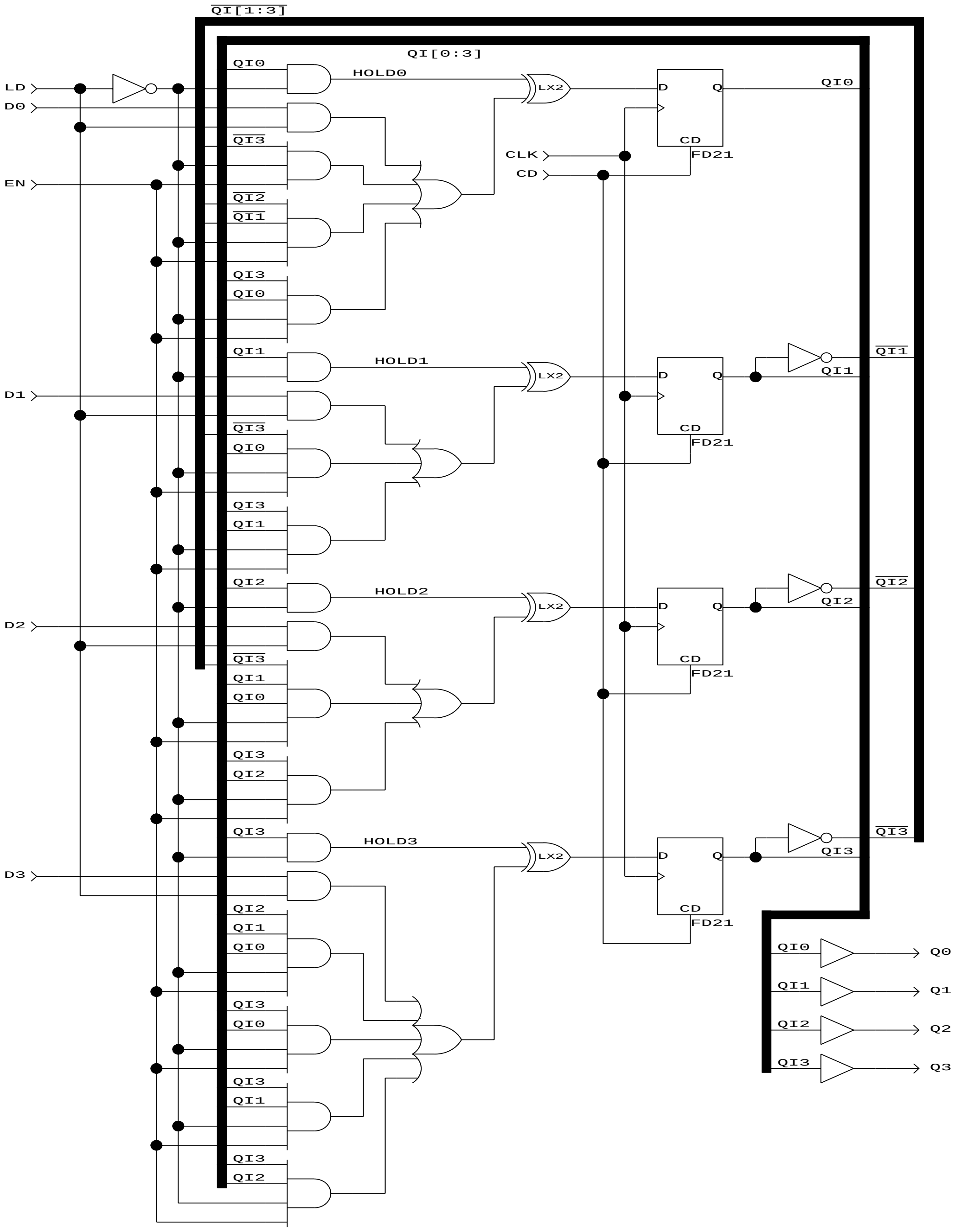
Truth Table:

The truth table is the same for both CDU1s.

Input					Output
CD	**LD**	**D**	**EN**	**CLK**	**Q**
1	x	x	x	x	0
0	1	d	x	↑	d
0	0	x	0	x	Q
0	0	x	1	↑	count up

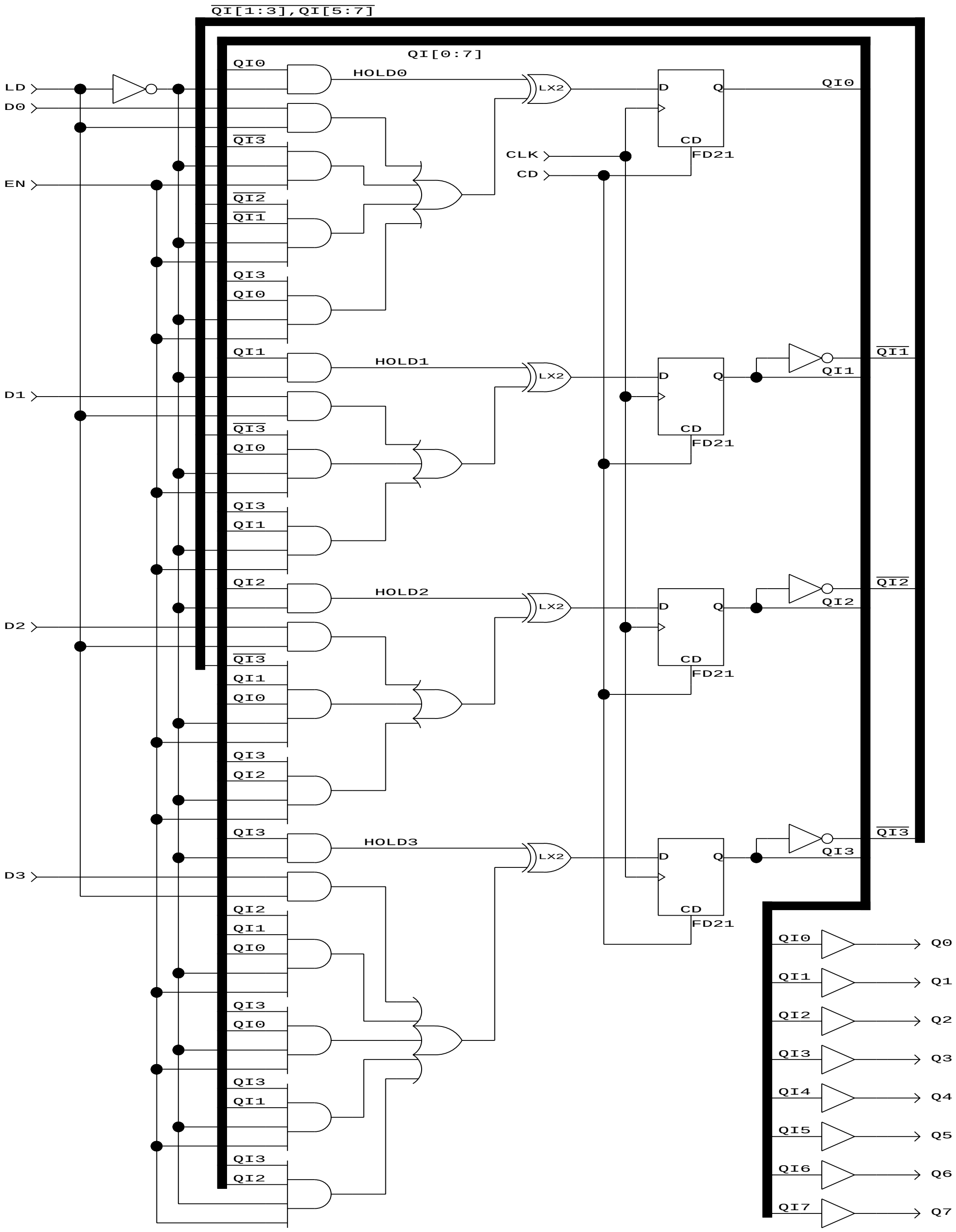
Valid states for each 4-bit digit are 0-9.
Loading higher hexadecimal input values (A-F)
clears that decimal output digit on the next clock pulse.
d = any pattern of 1s and 0s on an input or set of inputs,
Q = output of flip-flop or latch, x = don’t care,
↑ = rising clock edge.

CDU14

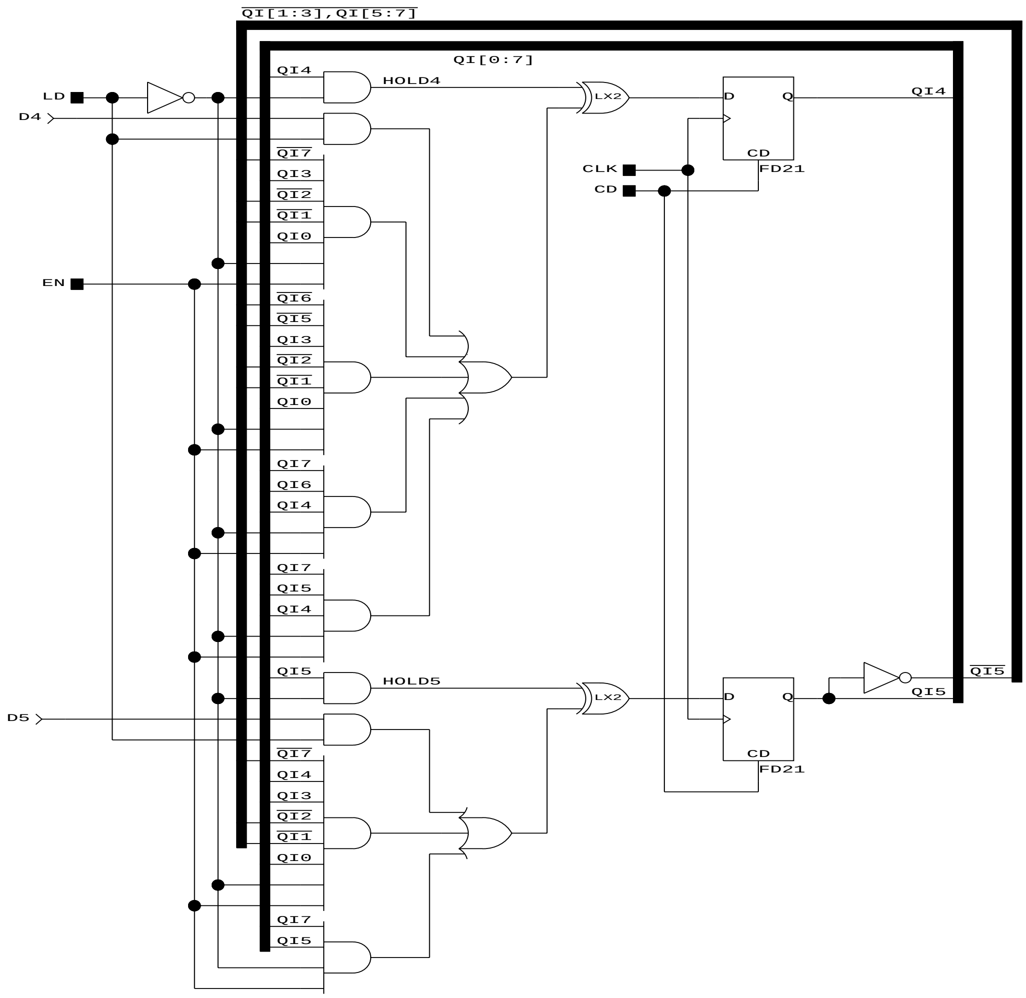


$\overline{QI[1:3]}$
QI[0:3]
LD
D0
EN
D1
D2
D3
QI0
$\overline{QI3}$
$\overline{QI2}$
$\overline{QI1}$
QI3
QI1
QI2
HOLD0
HOLD1
HOLD2
HOLD3
LX2
D
Q
CD
FD21
CLK
CD
QI0
QI1
QI2
QI3
$\overline{QI1}$
$\overline{QI2}$
$\overline{QI3}$
Q0
Q1
Q2
Q3

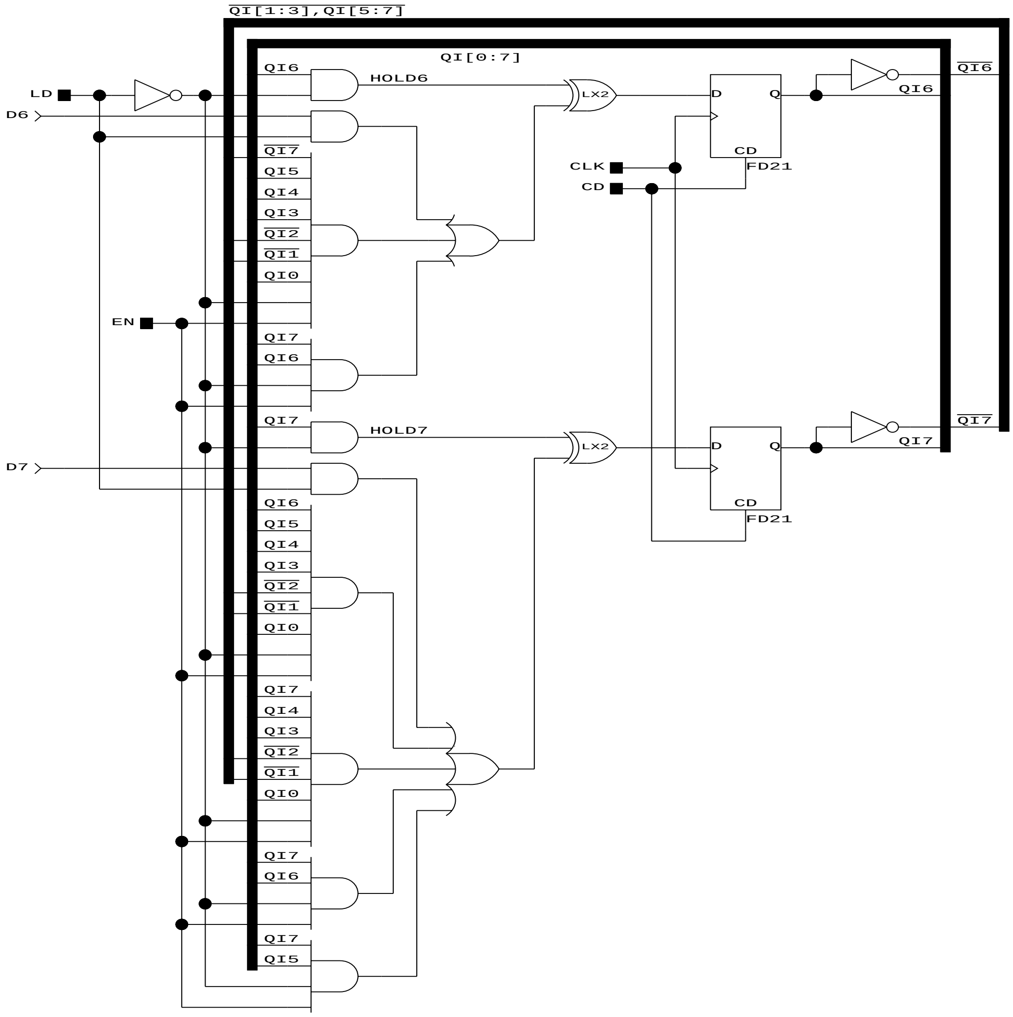
CDU18.1


QI[1:3],QI[5:7]
QI[0:7]
LD
D0
EN
D1
D2
D3
CLK
CD
QI0
QI1
QI2
QI3
HOLD0
HOLD1
HOLD2
HOLD3
LX2
D
Q
CD
FD21
QI0
QI1
QI2
QI3
QI4
QI5
QI6
QI7
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7

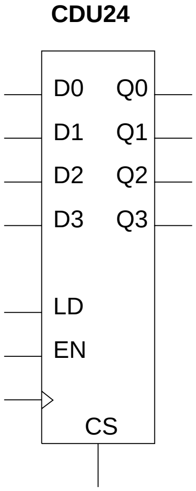
CDU18.2


$\overline{QI[1:3],QI[5:7]}$
QI[0:7]
QI4
HOLD4
LD
D4
$\overline{QI7}$
QI3
$\overline{QI2}$
$\overline{QI1}$
QI0
EN
$\overline{QI6}$
$\overline{QI5}$
QI3
$\overline{QI2}$
$\overline{QI1}$
QI0
QI7
QI6
QI4
QI7
QI5
QI4
LX2
D
Q
CD
FD21
CLK
CD
QI4
QI5
HOLD5
D5
$\overline{QI7}$
QI4
QI3
$\overline{QI2}$
$\overline{QI1}$
QI0
QI7
QI5
LX2
D
Q
CD
FD21
$\overline{QI5}$
QI5

CDU18.3


$\overline{\text{QI[1:3],QI[5:7]}}$
QI[0:7]
QI6
HOLD6
LD
D6
LX2
D
Q
$\overline{\text{QI6}}$
QI6
CD
FD21
CLK
CD
$\overline{\text{QI7}}$
QI5
QI4
QI3
$\overline{\text{QI2}}$
$\overline{\text{QI1}}$
QI0
EN
QI7
QI6
QI7
HOLD7
D7
LX2
D
Q
$\overline{\text{QI7}}$
QI7
CD
FD21
QI6
QI5
QI4
QI3
$\overline{\text{QI2}}$
$\overline{\text{QI1}}$
QI0
QI7
QI4
QI3
$\overline{\text{QI2}}$
$\overline{\text{QI1}}$
QI0
QI7
QI6
QI7
QI5

CDU24 and CDU28



Function:

4- and 8-bit decade up counters with synchronous clear, enable, and parallel data load.

Availability:

CDU24 and CDU28 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

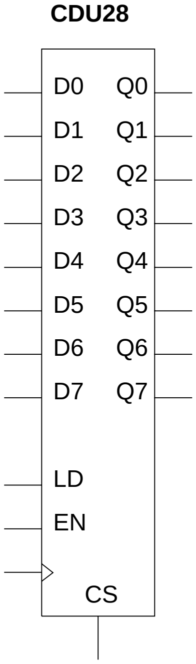
Schematics appear on the following pages.

Type: Hard

Logic Resources:

Macro	PT	GLB	Output	Level
CDU24	*	1	4	1
CDU28	**	3	8	1

```
*     CLK: 1 PT per GLB if Product Term Clock is used.
      Q0: 5 PT    Q1: 4 PT
      Q2: 4 PT    Q3: 6 PT
**    CLK: 1 PT per GLB if Product Term Clock is used.
      Q0: 5 PT    Q1: 4 PT
      Q2: 4 PT    Q3: 6 PT    Q4: 6 PT
      Q5: 4 PT    Q6: 4 PT    Q7: 6 PT
```



Macro Port Definition:

```
CDU24 ([Q0..Q3],[D0..D3],CLK,LD,EN,CS);
CDU28 ([Q0..Q7],[D0..D7],CLK,LD,EN,CS);
  CDU28_1 ([Q0..Q3],[D0..D3],CLK,LD,EN,CS);
  CDU28_2 ([Q4..Q6],[D4..D6],[Q0..Q3],Q7,CLK,LD,EN,CS);
  CDU28_3 (Q7,D7,[Q0..Q6],CLK,LD,EN,CS);
```

Counting Ranges:

CDU24: 0-9. CDU28: 0-99.

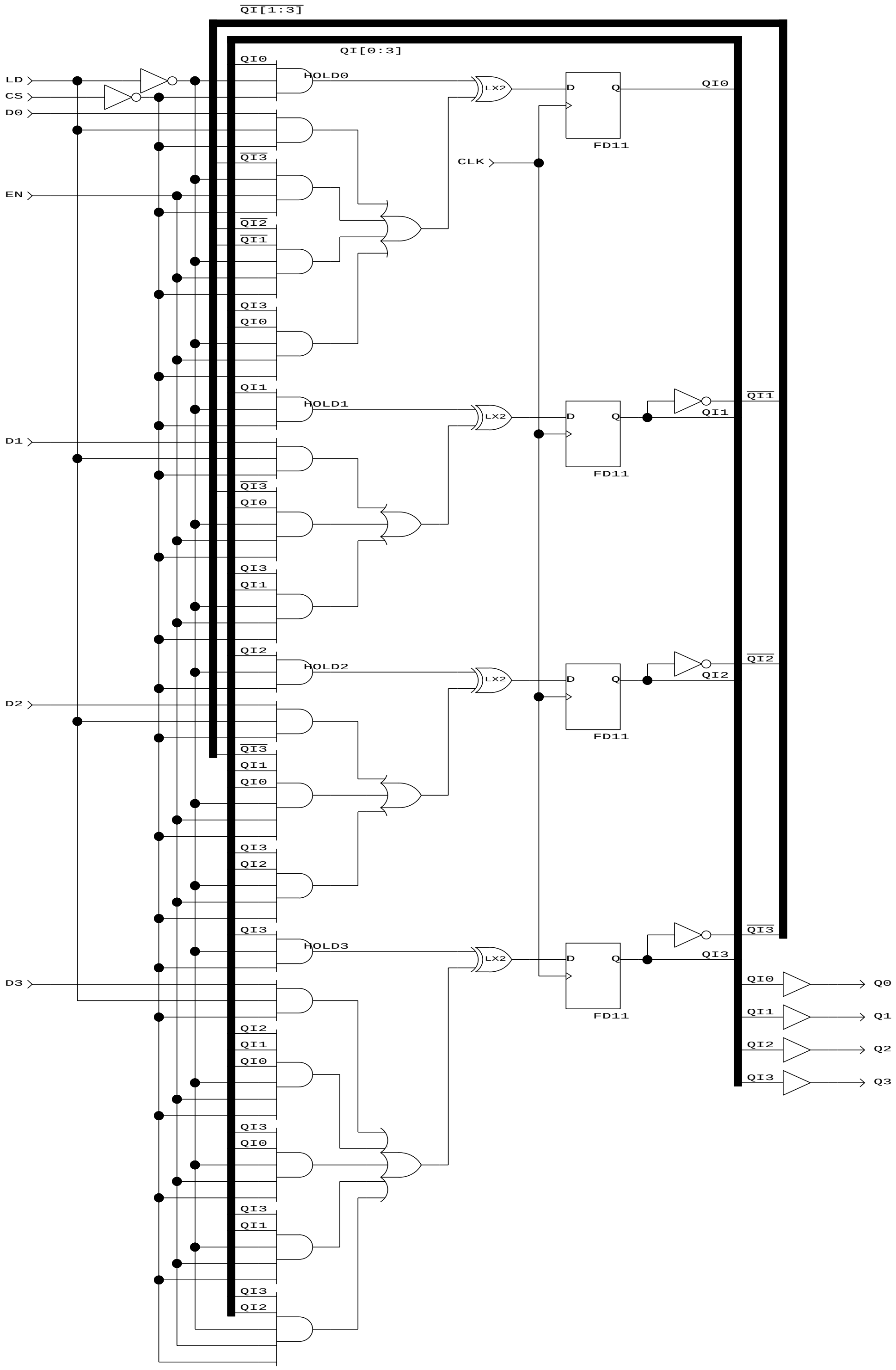
Truth Table:

The truth table is the same for both CDU2s.

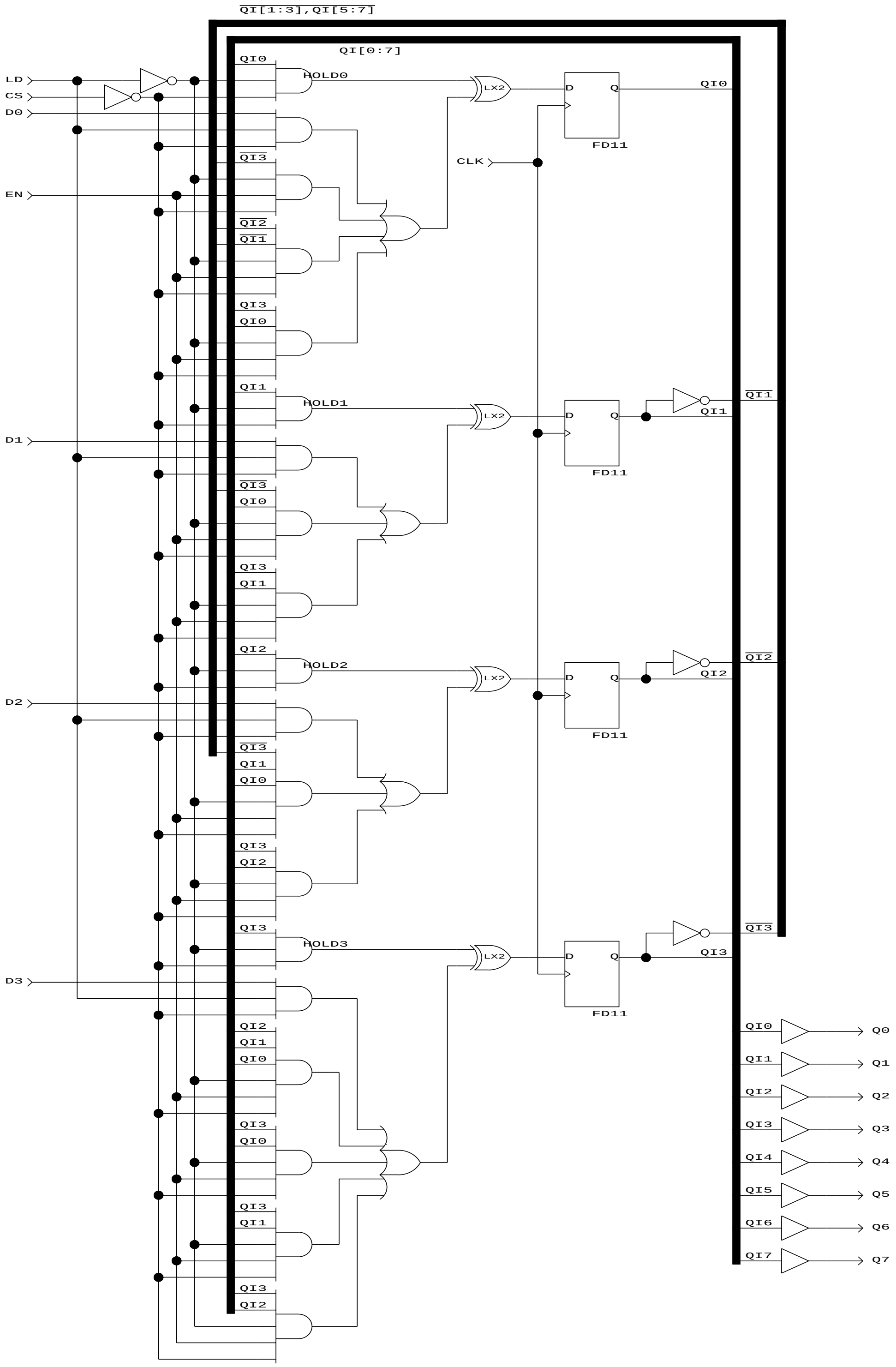
Input					Output
CS	**LD**	**D**	**EN**	**CLK**	**Q**
1	x	x	x	↑	0
0	1	d	x	↑	d
0	0	x	0	x	Q
0	0	x	1	↑	count up

Valid states for each 4-bit digit are 0~9.
Loading higher hexadecimal input values (A-F)
clears that decimal output digit on the next clock pulse.
d = any pattern of 1s and 0s on an input or set of inputs,
Q = output of flip-flop or latch,
x = don’t care, ↑ = rising clock edge.

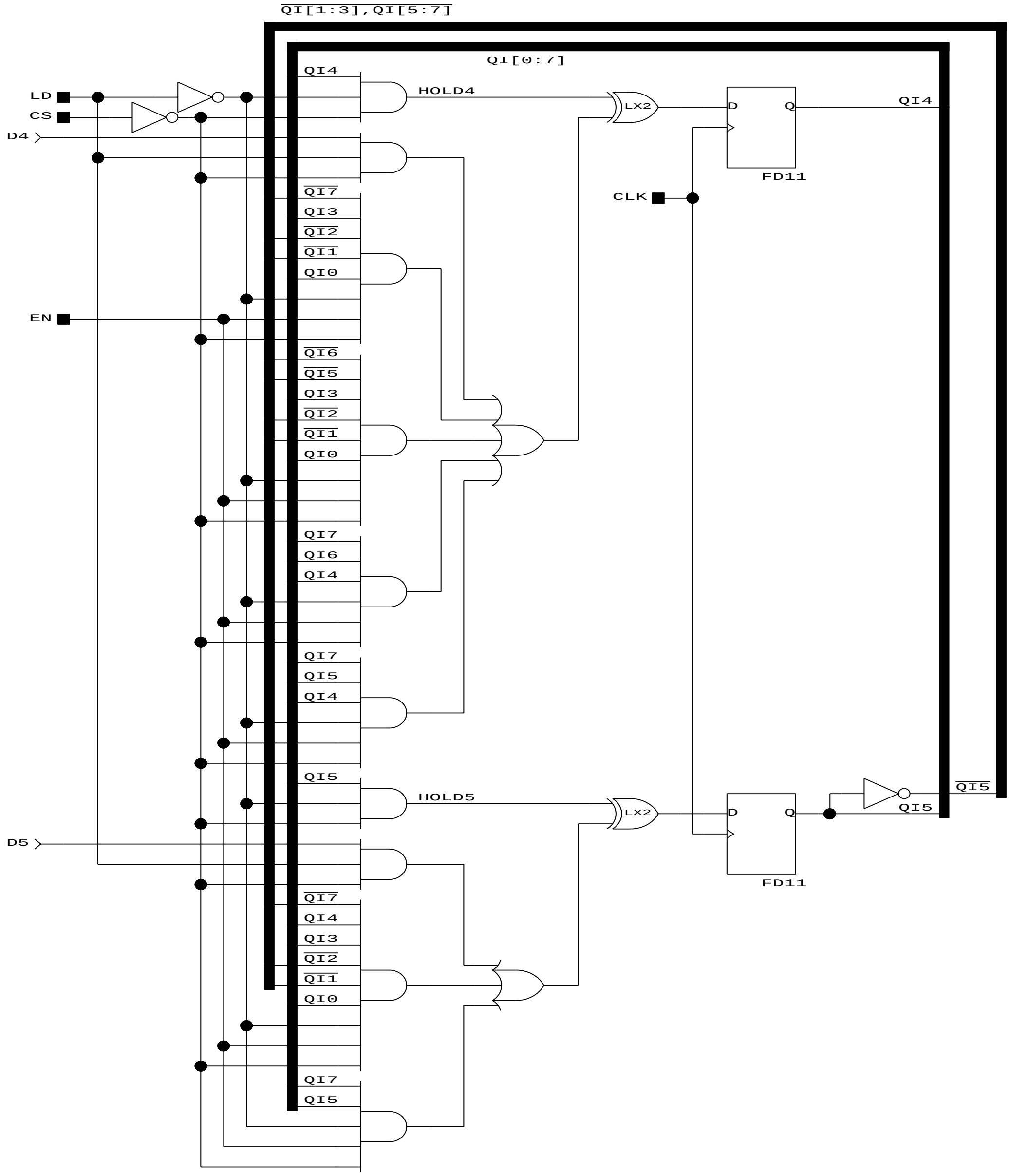
CDU24


$\overline{QI[1:3]}$
QI[0:3]
LD
CS
D0
EN
D1
D2
D3
CLK
HOLD0
HOLD1
HOLD2
HOLD3
LX2
D
Q
FD11
QI0
QI1
QI2
QI3
$\overline{QI1}$
$\overline{QI2}$
$\overline{QI3}$
Q0
Q1
Q2
Q3

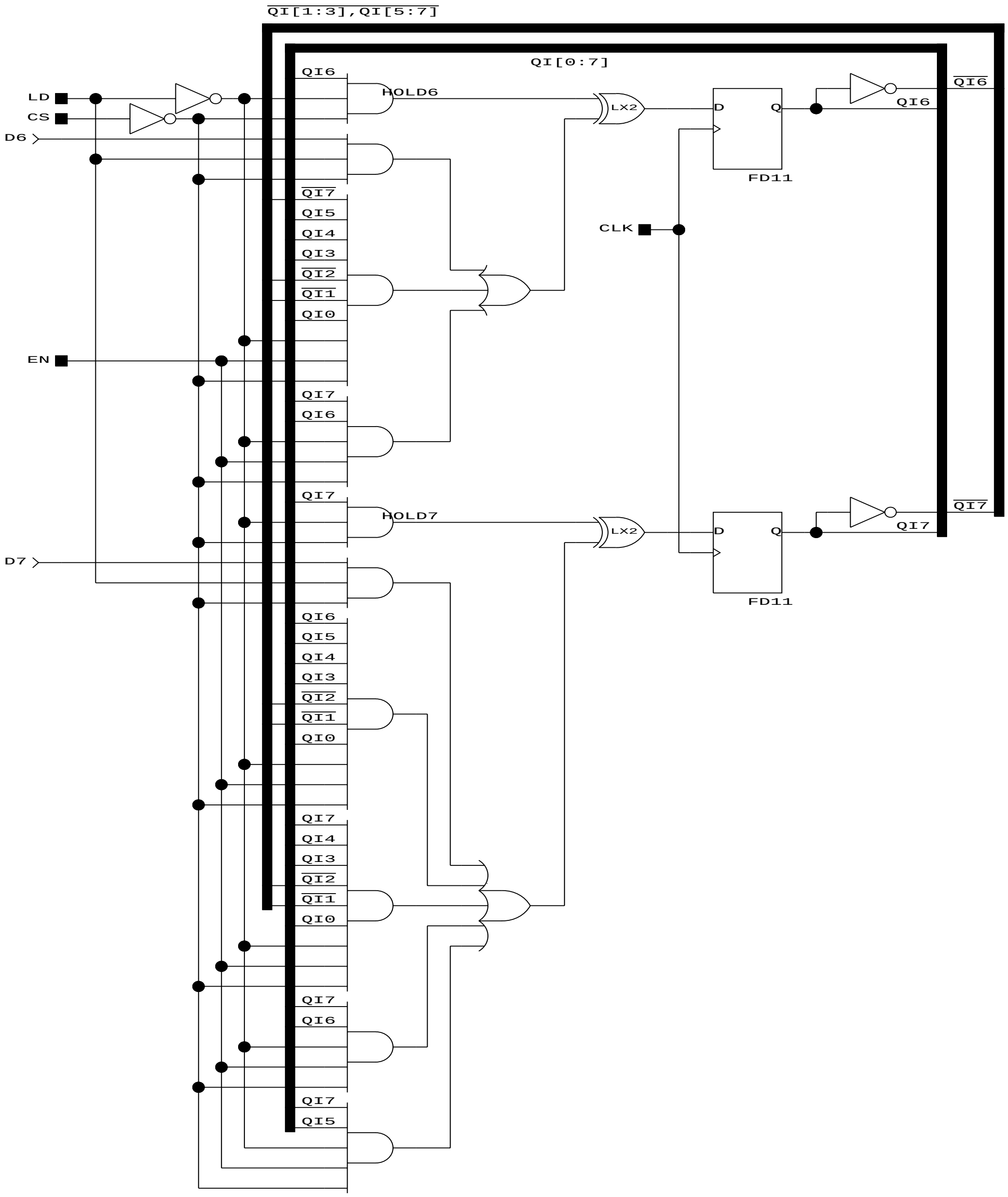
CDU28.1


QI[1:3],QI[5:7]
QI[0:7]
LD
CS
D0
EN
D1
D2
D3
CLK
QI0
QI3
QI2
QI1
HOLD0
HOLD1
HOLD2
HOLD3
LX2
D
Q
FD11
QI0
QI1
QI2
QI3
QI4
QI5
QI6
QI7
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7

CDU28.2

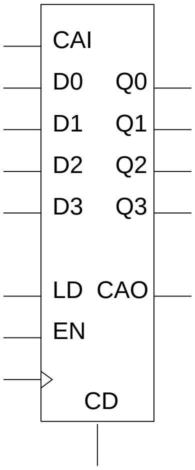

$\overline{QI[1:3],QI[5:7]}$
QI[0:7]
LD
CS
D4
EN
D5
CLK
QI4
HOLD4
LX2
D
Q
FD11
QI4
$\overline{QI7}$
QI3
$\overline{QI2}$
$\overline{QI1}$
QI0
$\overline{QI6}$
$\overline{QI5}$
QI3
$\overline{QI2}$
$\overline{QI1}$
QI0
QI7
QI6
QI4
QI7
QI5
QI4
QI5
HOLD5
LX2
D
Q
FD11
$\overline{QI5}$
QI5
$\overline{QI7}$
QI4
QI3
$\overline{QI2}$
$\overline{QI1}$
QI0
QI7
QI5

CDU28.3


$\overline{QI[1:3],QI[5:7]}$
QI[0:7]
LD
CS
D6
EN
D7
CLK
QI6
HOLD6
$\overline{QI7}$
QI5
QI4
QI3
$\overline{QI2}$
$\overline{QI1}$
QI0
QI7
QI6
QI7
HOLD7
QI6
QI5
QI4
QI3
$\overline{QI2}$
$\overline{QI1}$
QI0
QI7
QI4
QI3
$\overline{QI2}$
$\overline{QI1}$
QI0
QI7
QI6
QI7
QI5
LX2
D
Q
FD11
$\overline{QI6}$
QI6
LX2
D
Q
FD11
$\overline{QI7}$
QI7

CDU34 and CDU38

CDU34



Function:

4- and 8-bit decade up counters with asynchronous clear, enable, parallel data load, CAI, and CAO.

Availability:

CDU34 and CDU38 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Schematics appear on the following pages.

Type: Hard

Logic Resources:

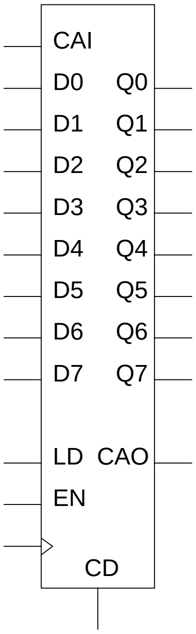
Macro	PT	GLB	Output	Level
CDU34	*	2	5	1***
CDU38	**	3	9	1***

* CLK: 1 PT per GLB if Product Term Clock is used.
CD: 1 PT per GLB.
Q0: 5 PT Q1: 4 PT
Q2: 4 PT Q3: 6 PT CAO: 1 PT

** CLK: 1 PT per GLB if Product Term Clock is used.
CD: 1 PT per GLB.
Q0: 5 PT Q1: 4 PT Q2: 4 PT Q3: 6 PT
Q4: 6 PT Q5: 4 PT Q6: 4 PT Q7: 6 PT
CAO: 1 PT

*** (CAO is a 2-level output).

CDU38



Macro Port Definition:

```
CDU34 ([Q0..Q3],CAO,[D0..D3],CAI,CLK,LD,EN,CD);
  CDU34_1 ([Q0..Q3],[D0..D3],CAI,CLK,LD,EN,CD);
  CDU34_2 (CAO,[Q0..Q3],CAI,EN);
CDU38 ([Q0..Q7],CAO,[D0..D7],CAI,CLK,LD,EN,CD);
  CDU38_1 ([Q0..Q3],[D0..D3],CAI,CLK,LD,EN,CD);
  CDU38_2 ([Q4..Q6],CAO,[D4..D6],[Q0..Q3],Q7,CAI,CLK,
               LD,EN,CD);
  CDU38_3 (Q7,D7,[Q0..Q6],CAI,CLK,LD,EN,CD);
```

Counting Ranges:

CDU34: 0-9. CDU38: 0-99.

Truth Table:

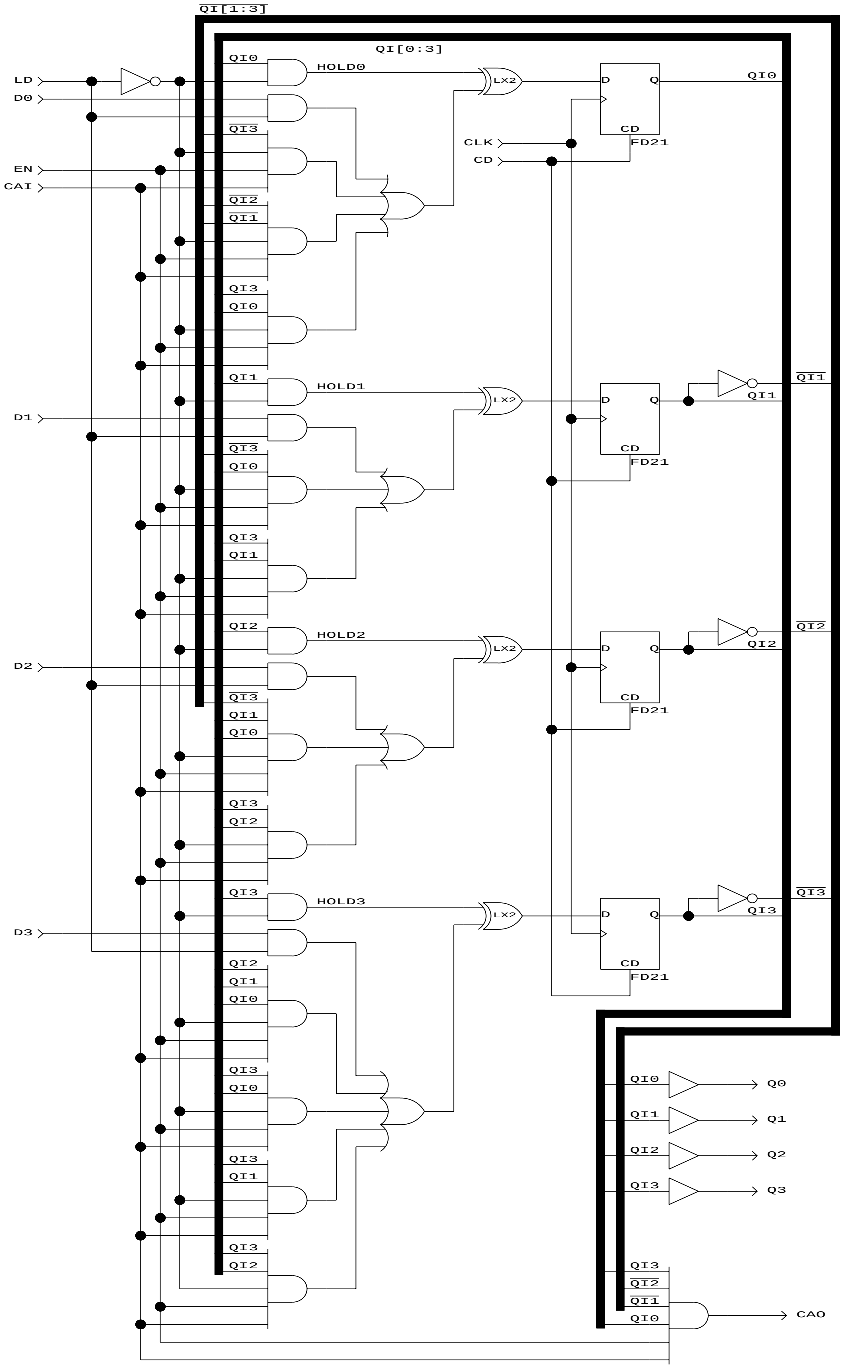
The truth table is the same for both CDU3s.

Input						Output	
CD	**LD**	**D**	**EN**	**CAI**	**CLK**	**Q**	**CAO**
1	x	x	x	x	x	0	0
0	1	d	x	x	↑	d	*
0	0	x	0	x	x	Q	0
0	0	x	x	0	x	Q	0
0	0	x	1	1	↑	count up	**

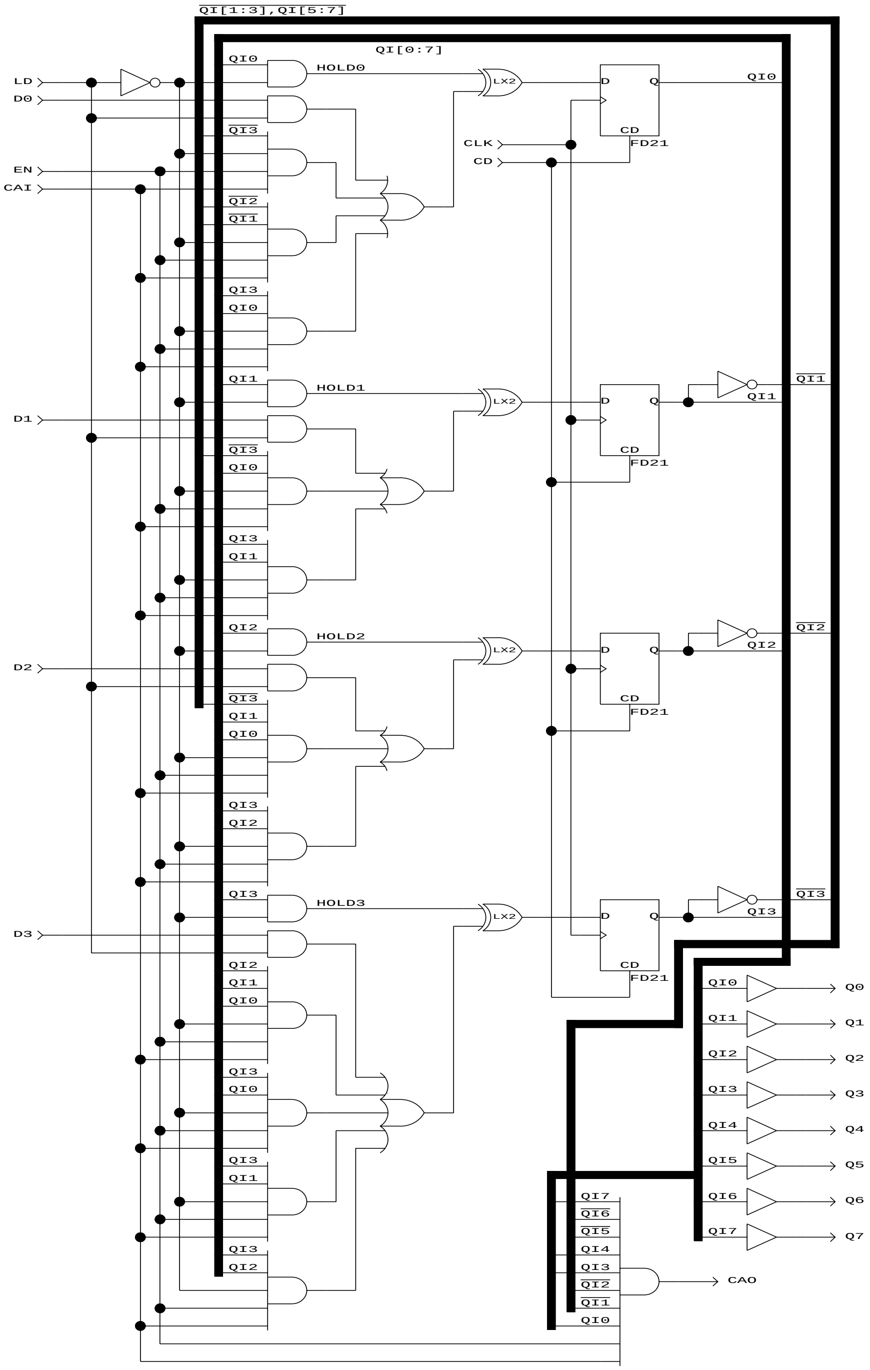
* CAO = CAI·EN·terminal count.

** CAO = 1 after terminal count (9 or 99) when CAI = 1 and EN = 1.
Valid states for each 4-bit digit are 0~9.
Loading higher hexadecimal input values (A-F)
clears that decimal output digit on the next clock pulse.
d = any pattern of 1s and 0s on an input or set of inputs,
Q = output of flip-flop or latch, x = don’t care, ↑ = rising clock edge.

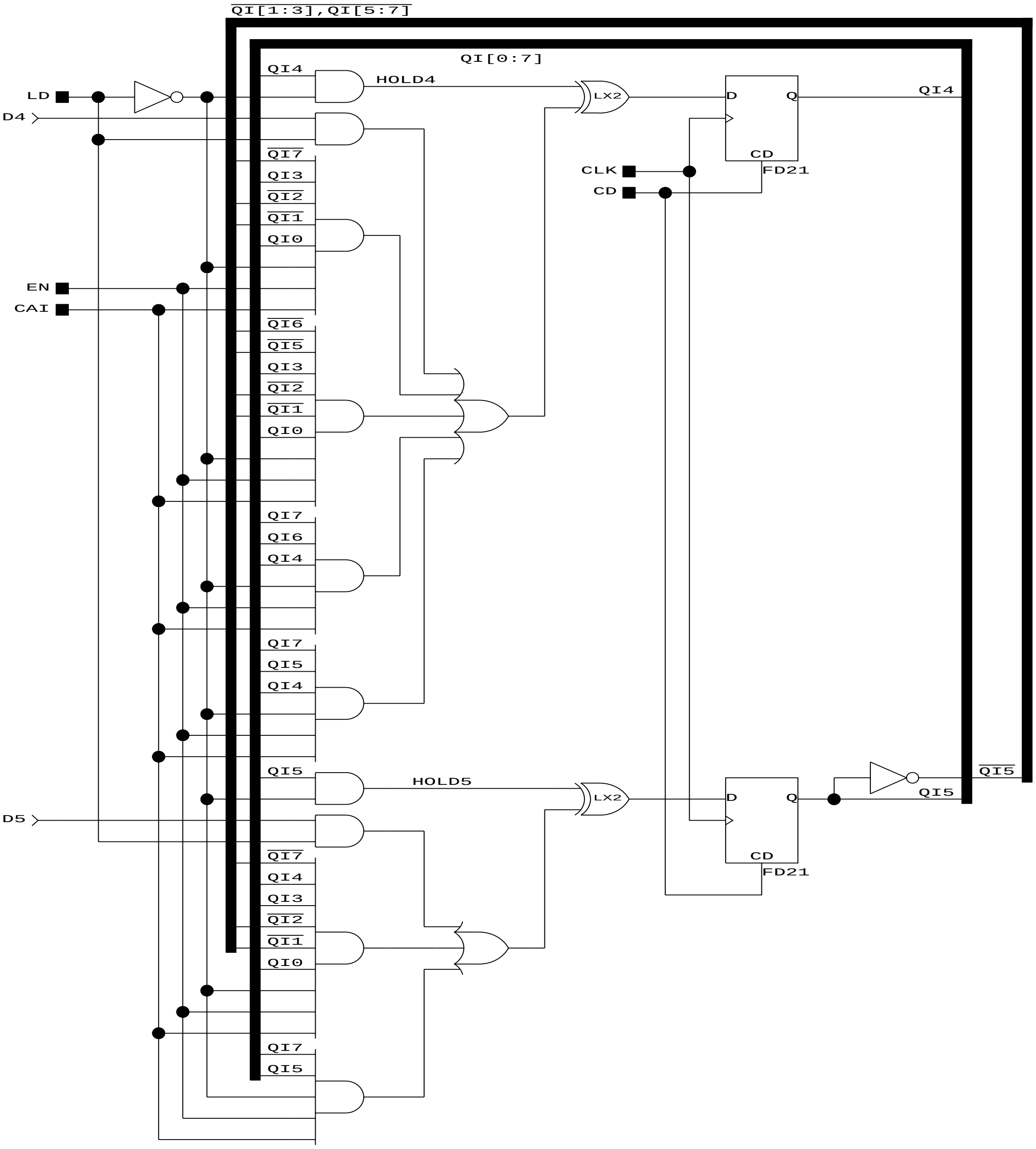
CDU34


QI[1:3]
QI[0:3]
LD
D0
EN
CAI
CLK
CD
D1
D2
D3
QI0
QI1
QI2
QI3
HOLD0
HOLD1
HOLD2
HOLD3
LX2
D
Q
CD
FD21
Q0
Q1
Q2
Q3
CAO

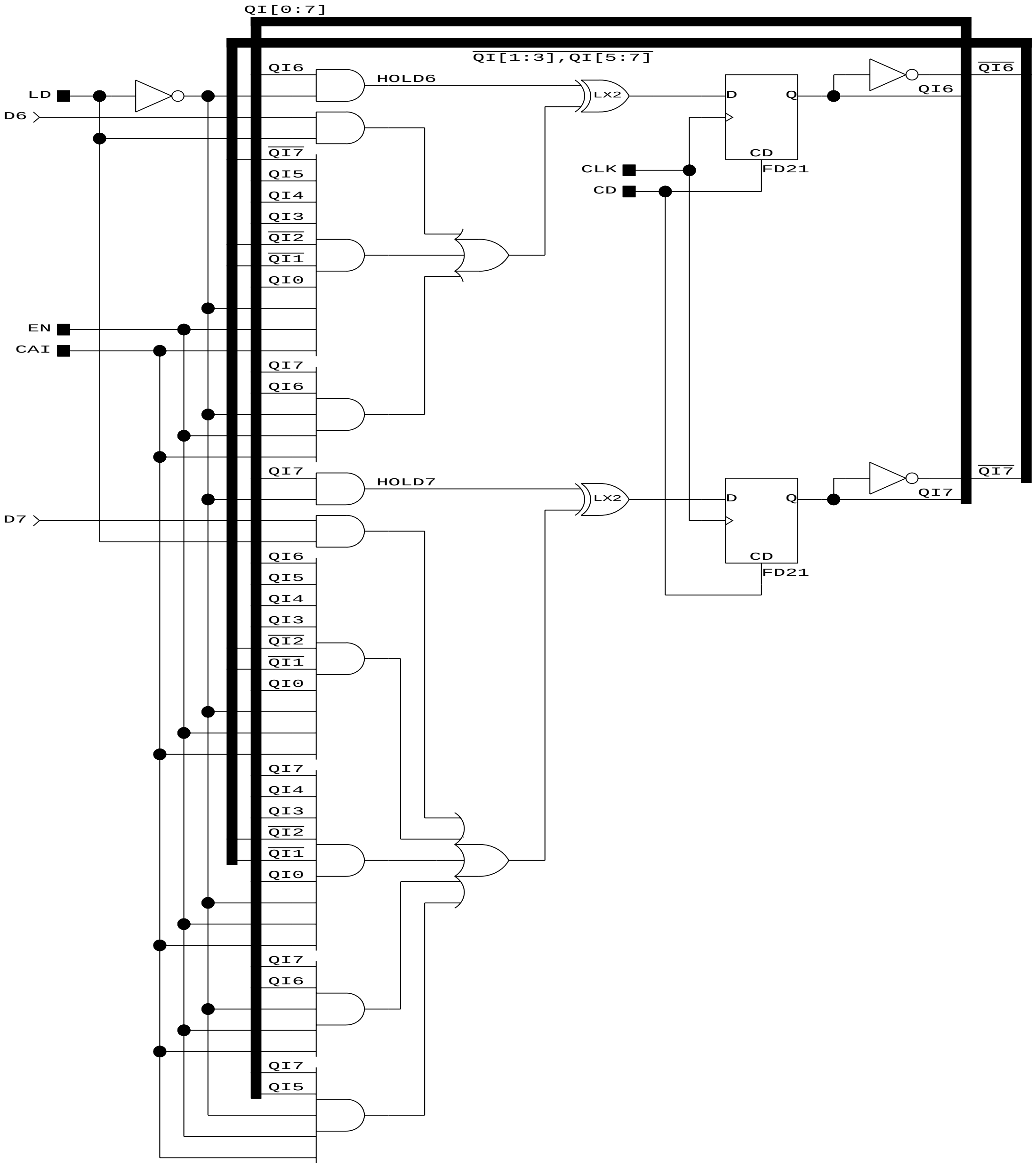
CDU38.1


QI[1:3],QI[5:7]
QI[0:7]
LD
D0
EN
CAI
D1
D2
D3
CLK
CD
HOLD0
HOLD1
HOLD2
HOLD3
LX2
D
Q
CD
FD21
QI0
QI1
QI2
QI3
QI4
QI5
QI6
QI7
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
CA0

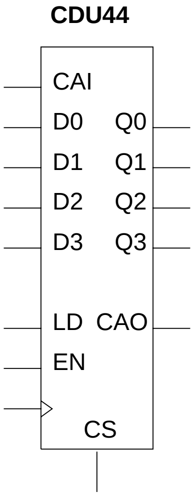
CDU38.2

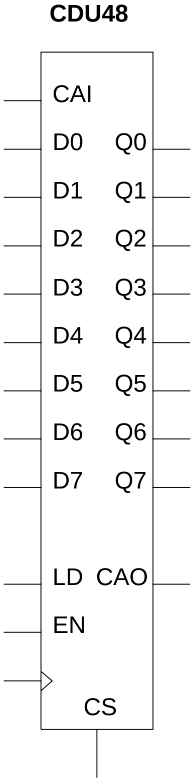

$\overline{QI[1:3],QI[5:7]}$
QI[0:7]
LD
D4
EN
CAI
D5
QI4
HOLD4
$\overline{QI7}$
QI3
$\overline{QI2}$
$\overline{QI1}$
QI0
$\overline{QI6}$
$\overline{QI5}$
QI3
$\overline{QI2}$
$\overline{QI1}$
QI0
QI7
QI6
QI4
QI7
QI5
QI4
QI5
HOLD5
$\overline{QI7}$
QI4
QI3
$\overline{QI2}$
$\overline{QI1}$
QI0
QI7
QI5
LX2
LX2
D
Q
CD
FD21
CLK
CD
D
Q
CD
FD21
QI4
$\overline{QI5}$
QI5

CDU38.3


QI[0:7]
$\overline{\text{QI[1:3],QI[5:7]}}$
QI6
HOLD6
LD
D6
LX2
D
Q
$\overline{\text{QI6}}$
QI6
CD
FD21
CLK
CD
$\overline{\text{QI7}}$
QI5
QI4
QI3
$\overline{\text{QI2}}$
$\overline{\text{QI1}}$
QI0
EN
CAI
QI7
QI6
QI7
HOLD7
D7
LX2
D
Q
$\overline{\text{QI7}}$
QI7
CD
FD21
QI6
QI5
QI4
QI3
$\overline{\text{QI2}}$
$\overline{\text{QI1}}$
QI0
QI7
QI4
QI3
$\overline{\text{QI2}}$
$\overline{\text{QI1}}$
QI0
QI7
QI6
QI7
QI5

CDU44 and CDU48





Function:

4- and 8-bit decade up counters with synchronous clear, enable, parallel data load, CAI, and CAO.

Availability:

CDU44 and CDU48 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Schematics appear on the following pages.

Type: Hard

Logic Resources:

Macro	PT	GLB	Output	Level
CDU44	*	2	5	1***
CDU48	**	3	9	1***

* CLK: 1 PT per GLB if Product Term Clock is used.
CAO: 1 PT
Q0: 5 PT Q1: 4 PT
Q2: 4 PT Q3: 6 PT

** CLK: 1 PT per GLB if Product Term Clock is used.
CAO: 1 PT
Q0: 5 PT Q1: 4 PT
Q2: 4 PT Q3: 6 PT Q4: 6 PT
Q5: 4 PT Q6: 4 PT Q7: 6 PT

*** (CAO is a 2-level output).

Macro Port Definition:

```
CDU44 ([Q0..Q3],CAO,[D0..D3],CAI,CLK,LD,EN,CS);
  CDU44_1 ([Q0..Q3],[D0..D3],CAI,CLK,LD,EN,CS);
  CDU44_2 (CAO,[Q0..Q3],CAI,EN);
CDU48 ([Q0..Q7],CAO,[D0..D7],CAI,CLK,LD,EN,CS);
  CDU48_1 ([Q0..Q3],[D0..D3],CAI,CLK,LD,EN,CS);
  CDU48_2 ([Q4..Q6],CAO,[D4..D6],[Q0..Q3],Q7,CAI,CLK,
             LD,EN,CS);
  CDU48_3 (Q7,D7,[Q0..Q6],CAI,CLK,LD,EN,CS);
```

Counting Ranges:

CDU44: 0-9. CDU48: 0-99.

Truth Table:

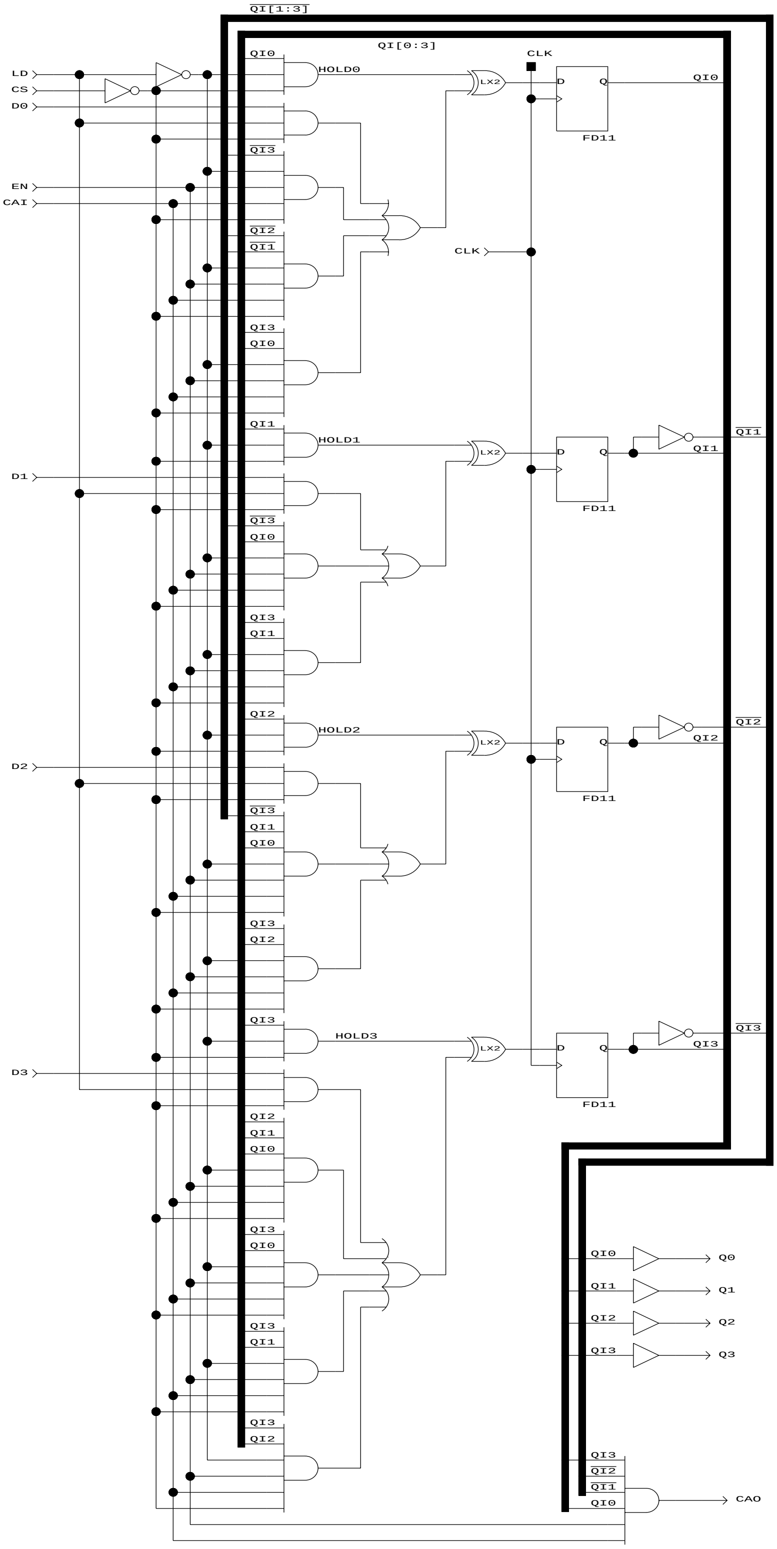
The truth table is the same for both CDU4s.

Input						Output	
CS	**LD**	**D**	**EN**	**CAI**	**CLK**	**Q**	**CAO**
1	x	x	x	x	↑	0	0
0	1	d	x	x	↑	d	*
0	0	x	0	x	x	Q	0
0	0	x	x	0	x	Q	0
0	0	x	1	1	↑	count up	**

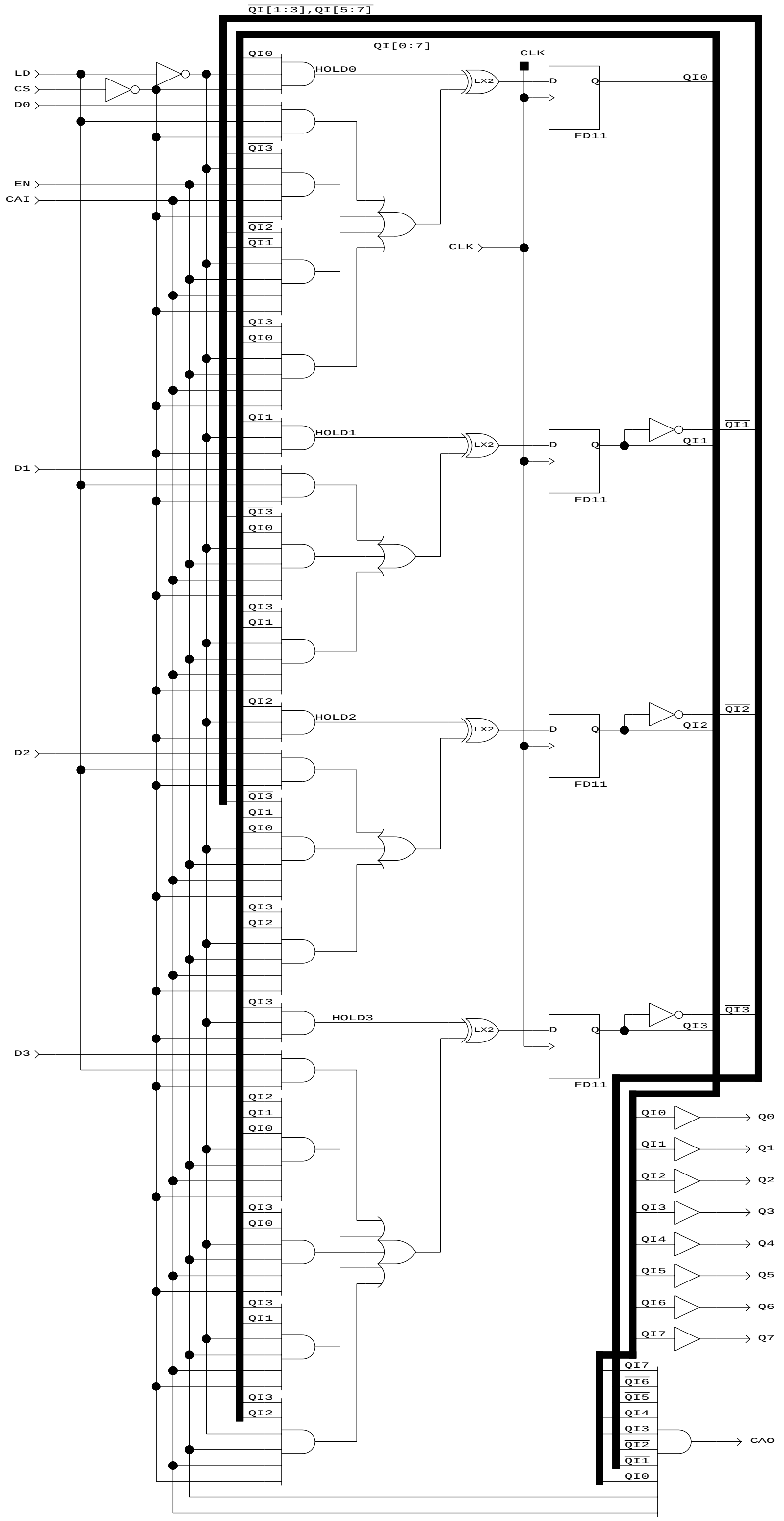
* CAO = CAI·EN·terminal count.

** CAO = 1 after terminal count (9 or 99) when CAI =1 and EN =1.
Valid states for each 4-bit digit are 0~9.
Loading higher hexadecimal input values (A-F)
clears that decimal output digit on the next clock pulse.
d = any pattern of 1s and 0s on an input or set of inputs,
Q = output of flip-flop or latch, x = don't care, ↑ = rising clock edge.

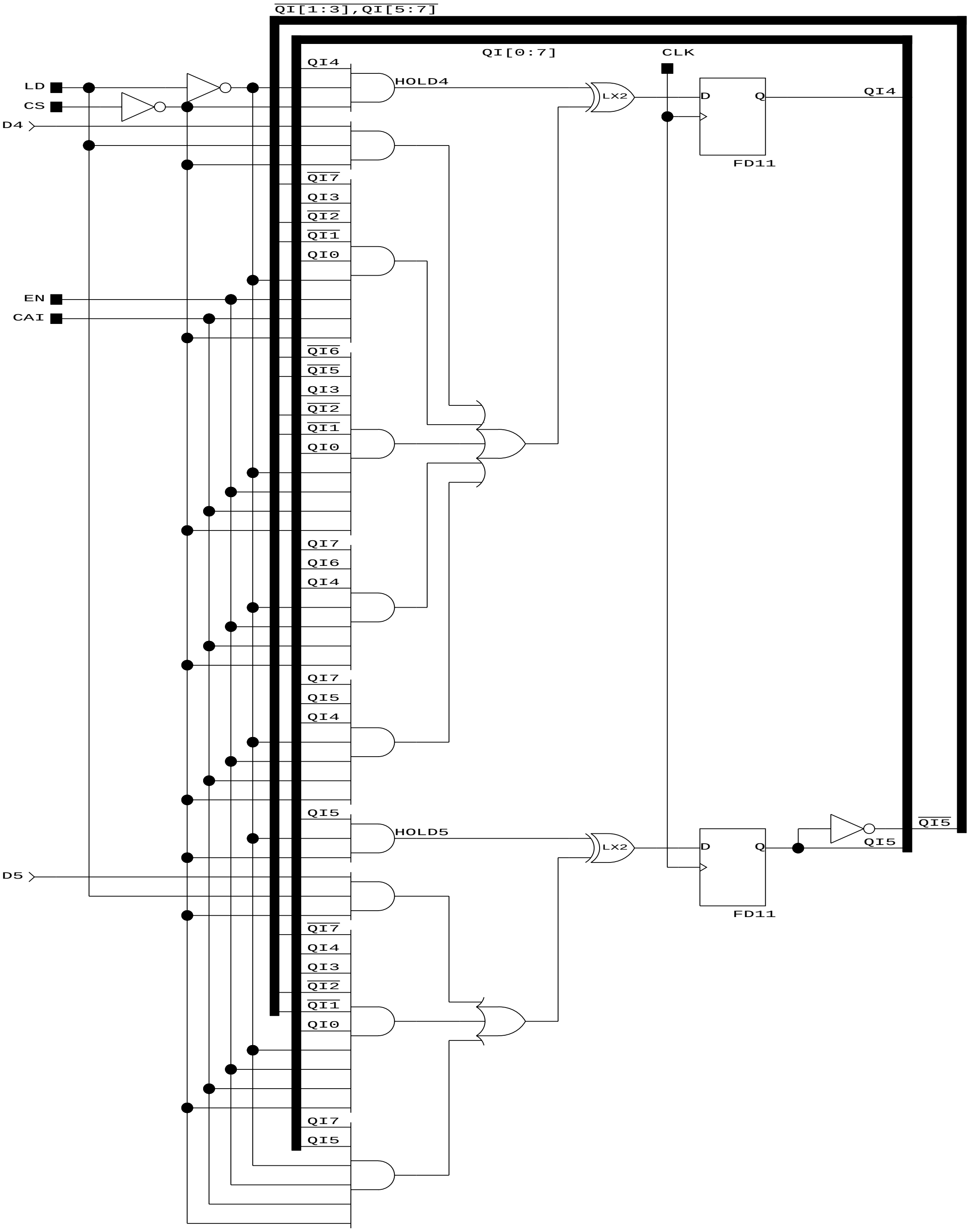
CDU44


QI[1:3]
QI[0:3]
CLK
LD
CS
D0
EN
CAI
D1
D2
D3
HOLD0
HOLD1
HOLD2
HOLD3
LX2
D
Q
FD11
QI0
QI1
QI2
QI3
Q0
Q1
Q2
Q3
CA0

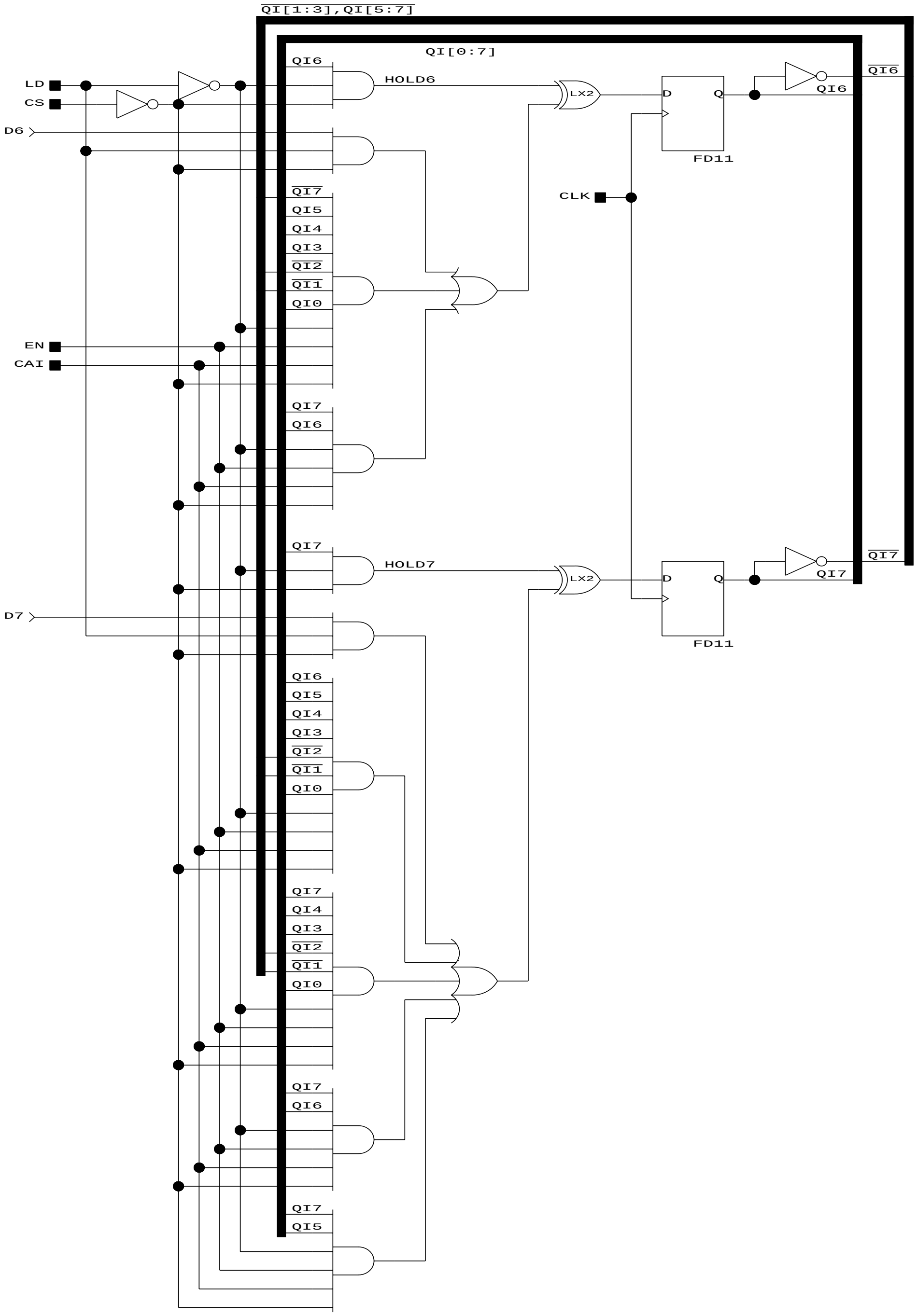
CDU48.1


$\overline{QI[1:3]},QI[5:7]$
QI[0:7]
LD
CS
D0
EN
CAI
D1
D2
D3
CLK
CLK
HOLD0
HOLD1
HOLD2
HOLD3
LX2
D
Q
FD11
QI0
$\overline{QI1}$
QI1
$\overline{QI2}$
QI2
$\overline{QI3}$
QI3
Q0
Q1
Q2
Q3
Q4
Q5
Q6
Q7
QI4
QI5
QI6
QI7
CA0

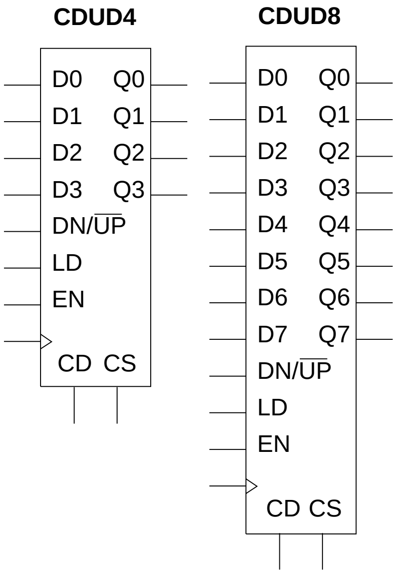
CDU48.2


QI[1:3],QI[5:7]
QI[0:7]
CLK
LD
CS
D4
EN
CAI
D5
QI4
HOLD4
LX2
D
Q
FD11
QI7
QI3
QI2
QI1
QI0
QI6
QI5
QI4
HOLD5
QI5
QI5

CDU48.3


$\overline{QI[1:3],QI[5:7]}$
QI[0:7]
LD
CS
D6
QI6
HOLD6
LX2
D
Q
FD11
$\overline{QI6}$
QI6
CLK
$\overline{QI7}$
QI5
QI4
QI3
$\overline{QI2}$
$\overline{QI1}$
QI0
EN
CAI
QI7
QI6
QI7
HOLD7
LX2
D
Q
FD11
$\overline{QI7}$
QI7
D7
QI6
QI5
QI4
QI3
$\overline{QI2}$
$\overline{QI1}$
QI0
QI7
QI4
QI3
$\overline{QI2}$
$\overline{QI1}$
QI0
QI7
QI6
QI7
QI5

CDUD4 and CDUD8



Function:

4- and 8-bit decade up/down counters with asynchronous clear, synchronous clear, enable, and parallel data load.

Availability:

CDUD4 and CDUD8 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Schematics appear on the following pages.

Type: Hard

Logic Resources:

Macro	PT	GLB	Output	Level
CDUD4	*	2	4	1
CDUD8	**	4	8	1

* CLK: 1 PT per GLB if Product Term Clock is used.
CD: 1 PT per GLB.
Q0: 5 PT Q1: 7 PT
Q2: 6 PT Q3: 7 PT

** CLK: 1 PT per GLB if Product Term Clock is used.
CD: 1 PT per GLB.
Q0: 5 PT Q1: 7 PT Q2: 6 PT
Q3: 7 PT Q4: 8 PT Q5: 7 PT
Q6: 6 PT Q7: 7 PT

Macro Port Definition:

```
CDUD4 ([Q0..Q3],[D0..D3],CLK,LD,EN,DNUP,CD,CS);
  CDUD4_1 ([Q0..Q2],[D0..D2],Q3,CLK,LD,EN,DNUP,CD,CS);
  CDUD4_2 (Q3,D3,[Q0..Q2],CLK,LD,EN,DNUP,CD,CS);
CDUD8 ([Q0..Q7],[D0..D7],CLK,LD,EN,DNUP,CD,CS);
  CDUD8_1 ([Q0..Q2],[D0..D2],Q3,CLK,LD,EN,DNUP,CD,CS);
  CDUD8_2 (Q3,Q4,D3,D4,[Q0..Q2],[Q5..Q7],CLK,LD,EN,DNUP,CD,CS);
  CDUD8_3 (Q5,Q6,D5,D6,[Q0..Q4],Q7,CLK,LD,EN,DNUP,CD,CS);
  CDUD8_4 (Q7,D7,[Q0..Q6],CLK,LD,EN,DNUP,CD,CS);
```

Counting Ranges:

CDUD4: 0↔9. 8: 0↔99.

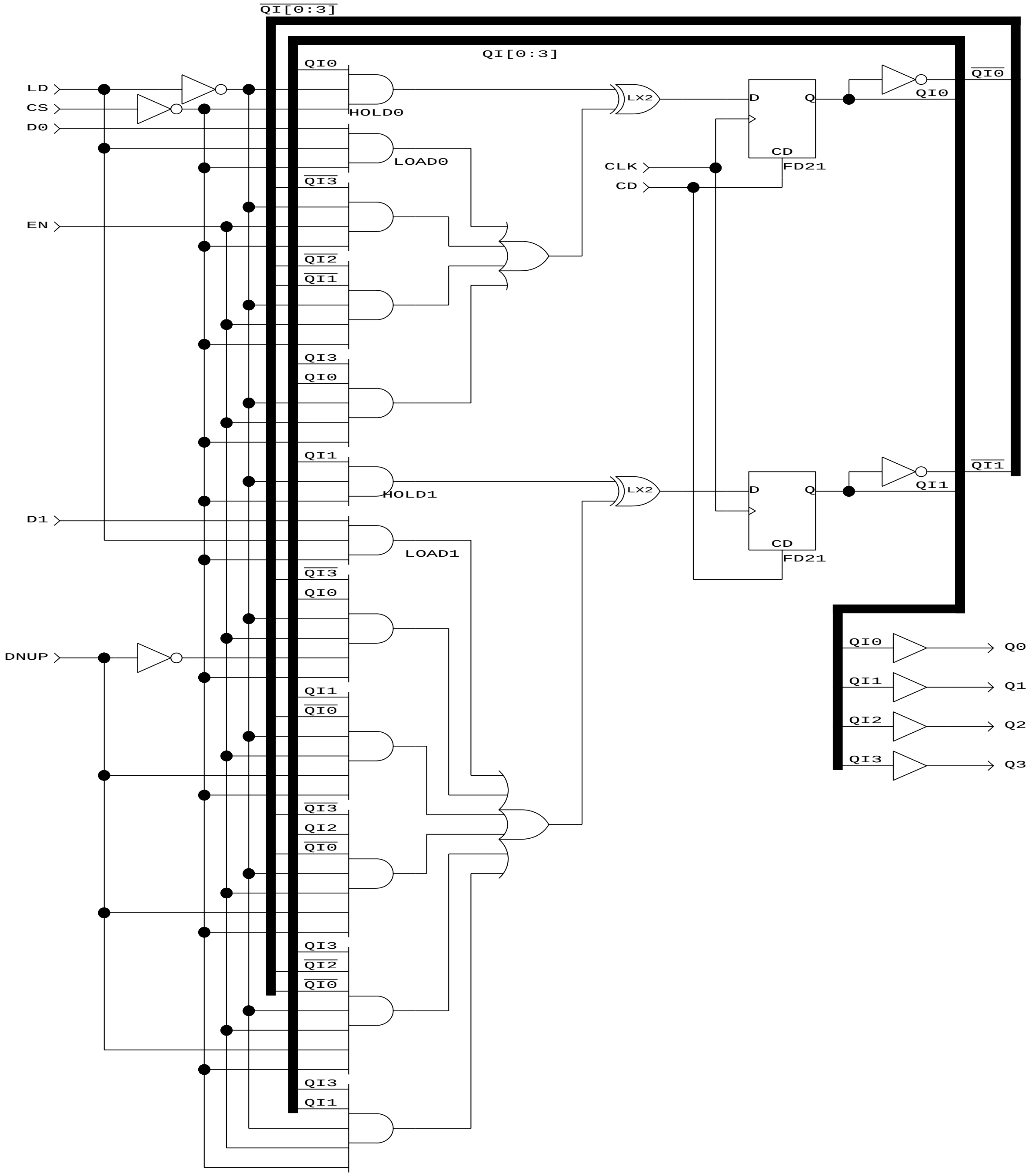
Truth Table:

The truth table is the same for both CDUD4 and CDUD8.

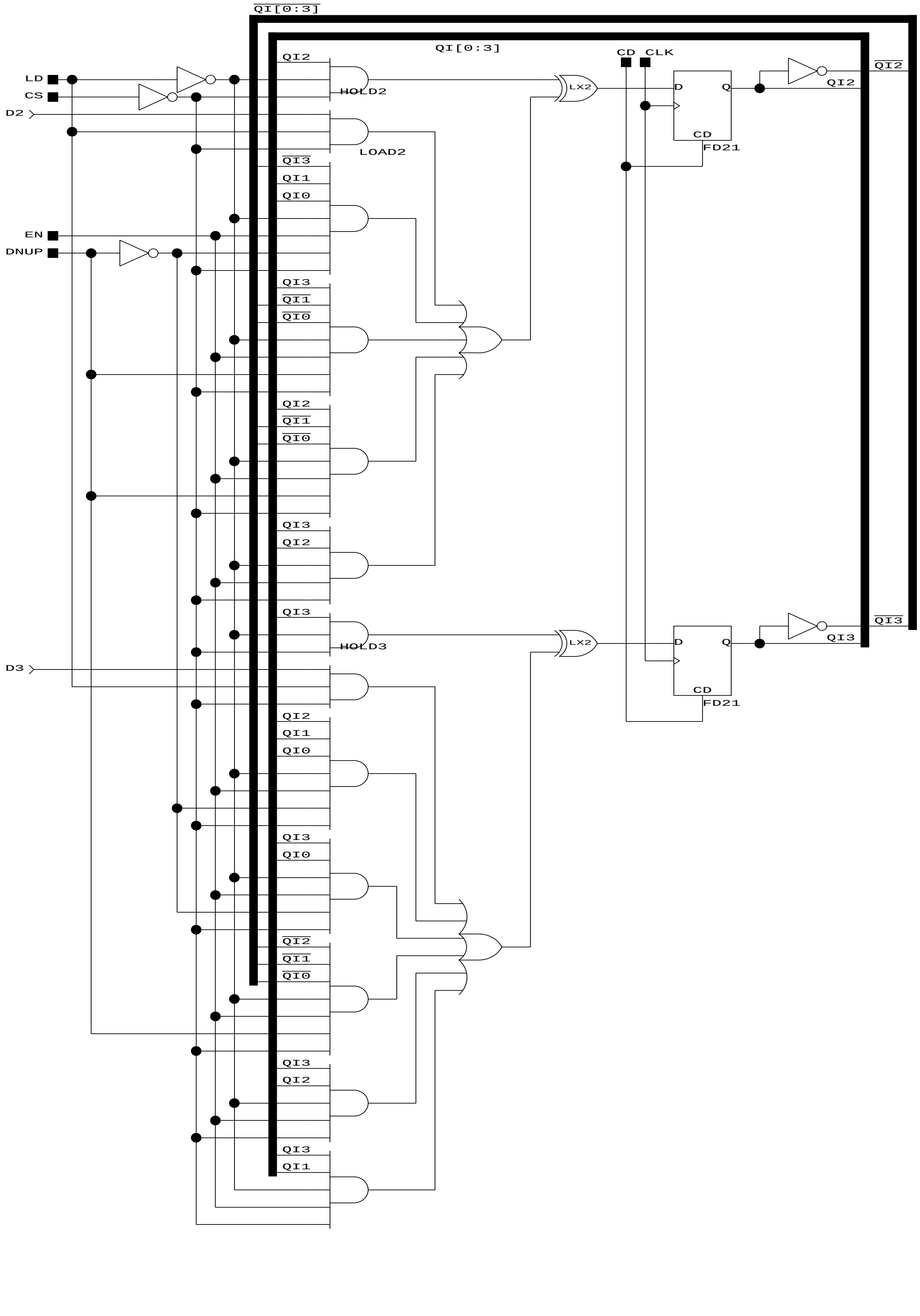
Input							**Output**
CD	**CS**	**LD**	**D**	**EN**	**DNUP**	**CLK**	**Q**
1	x	x	x	x	x	x	0
0	1	x	x	x	x	↑	0
0	0	1	d	x	x	↑	d
0	0	0	x	0	x	x	Q
0	0	0	x	1	0	↑	count up
0	0	0	x	1	1	↑	count down

Valid states for each 4-bit digit are 0~9.
Loading higher hexadecimal input values (A-F)
clears that decimal output digit on the next clock pulse.
d = any pattern of 1s and 0s on an input or set of inputs,
Q = output of flip-flop or latch, x = don’t care,
↑= rising clock edge.

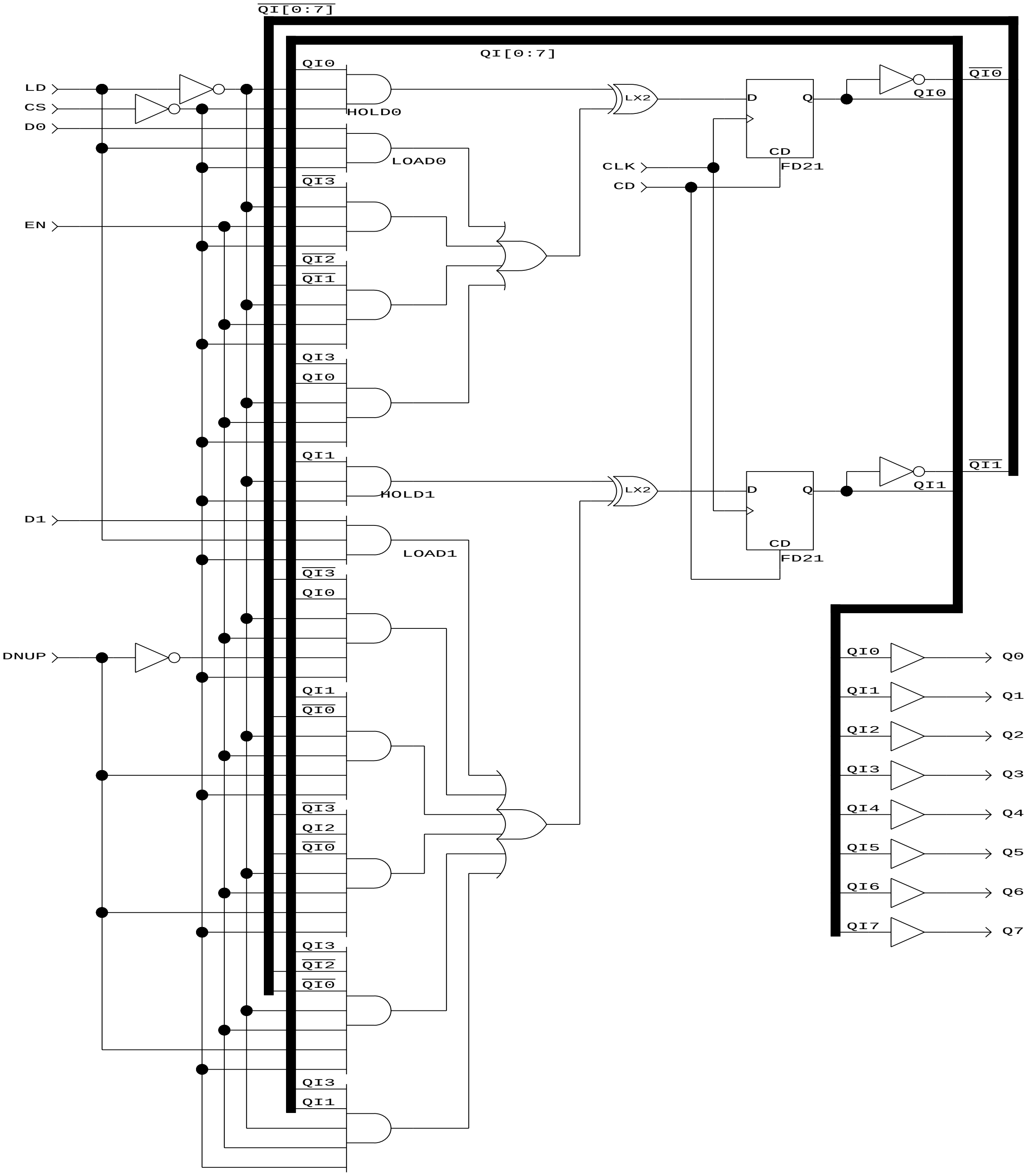
CDUD4.1


QI[0:3]
QI[0:3]
LD
CS
D0
EN
D1
DNUP
CLK
CD
QI0
QI3
QI2
QI1
HOLD0
LOAD0
HOLD1
LOAD1
LX2
D
Q
CD
FD21
QI0
QI1
Q0
Q1
Q2
Q3
QI2
QI3

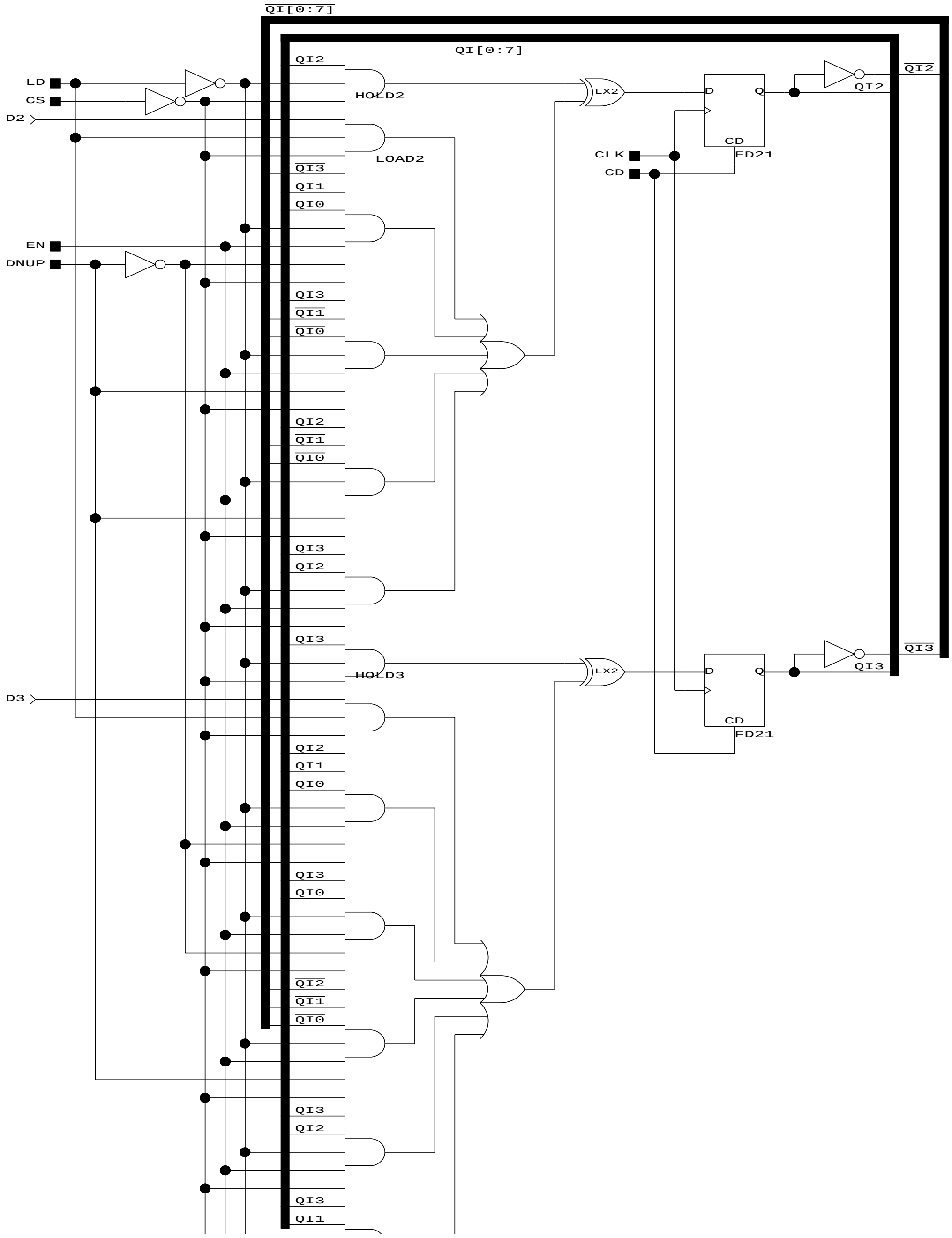
CDUD4.2


$\overline{QI[0:3]}$
QI[0:3]
CD
CLK
LD
CS
D2
QI2
HOLD2
LX2
D
Q
CD
FD21
$\overline{QI2}$
QI2
LOAD2
$\overline{QI3}$
QI1
QI0
EN
DNUP
QI3
$\overline{QI1}$
$\overline{QI0}$
QI2
$\overline{QI1}$
$\overline{QI0}$
QI3
QI2
QI3
HOLD3
D3
LX2
D
Q
CD
FD21
$\overline{QI3}$
QI3
QI2
QI1
QI0
QI3
QI0
$\overline{QI2}$
$\overline{QI1}$
$\overline{QI0}$
QI3
QI2
QI3
QI1

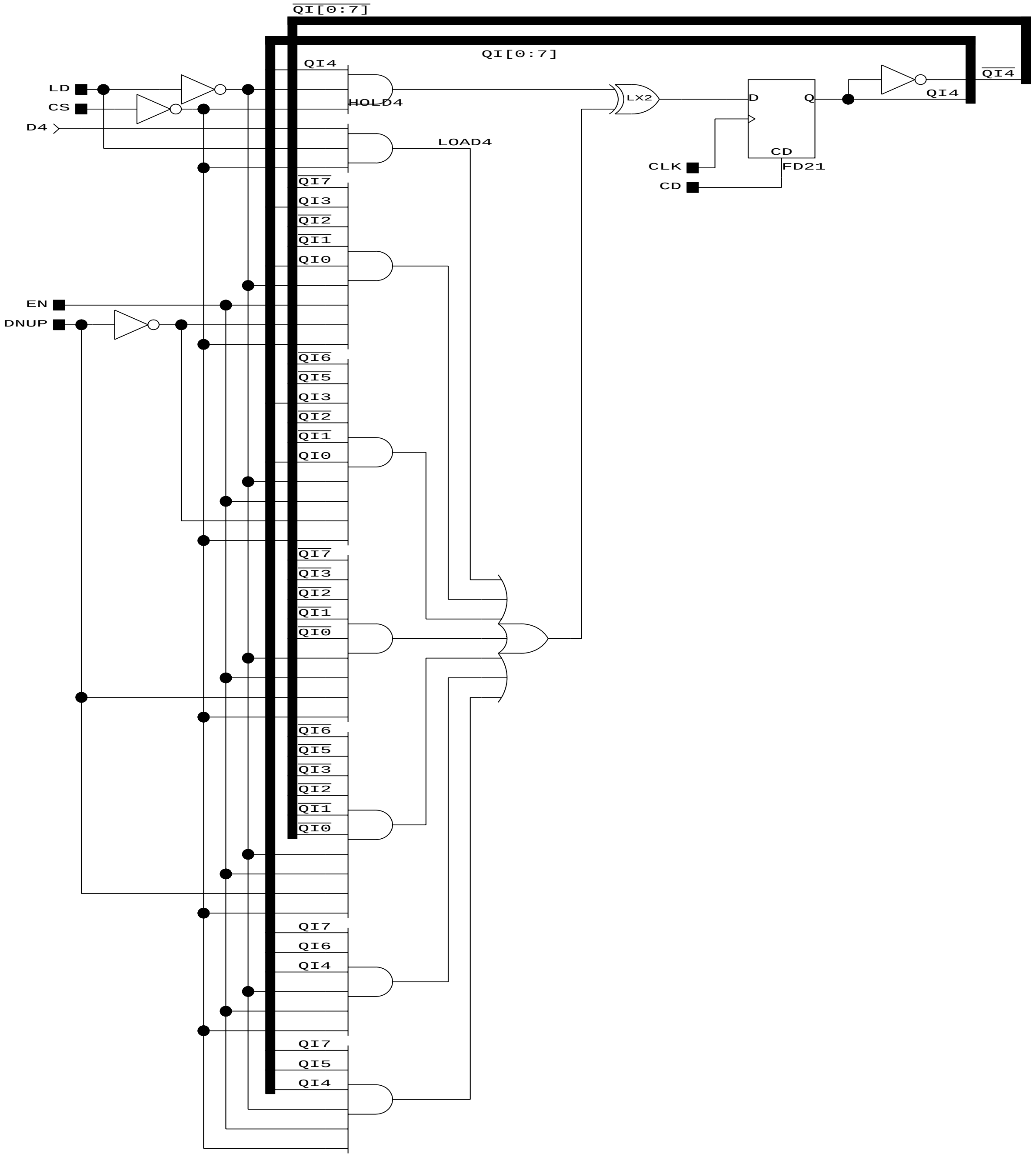
CDUD8.1


$\overline{QI[0:7]}$
QI[0:7]
QI0
LD
CS
D0
HOLD0
LOAD0
$\overline{QI3}$
EN
$\overline{QI2}$
$\overline{QI1}$
QI3
QI0
QI1
HOLD1
D1
LOAD1
$\overline{QI3}$
QI0
DNUP
QI1
$\overline{QI0}$
$\overline{QI3}$
QI2
$\overline{QI0}$
QI3
$\overline{QI2}$
$\overline{QI0}$
QI3
QI1
LX2
LX2
D
Q
CD
FD21
CLK
CD
D
Q
CD
FD21
$\overline{QI0}$
QI0
$\overline{QI1}$
QI1
QI0
Q0
QI1
Q1
QI2
Q2
QI3
Q3
QI4
Q4
QI5
Q5
QI6
Q6
QI7
Q7

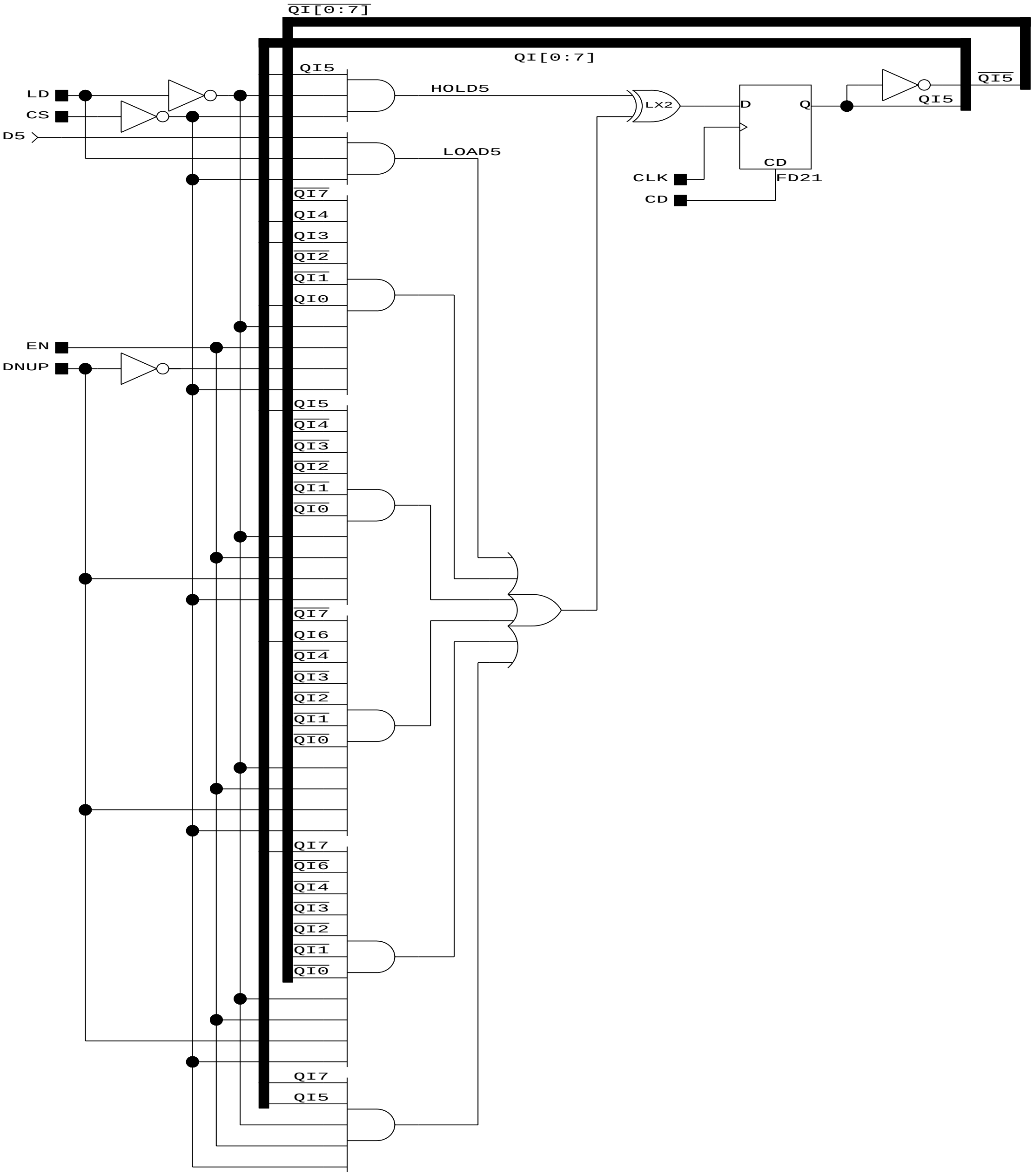
CDUD8.2


QI[0:7]
QI[0:7]
LD
CS
D2
EN
DNUP
D3
CLK
CD
QI2
QI3
QI1
QI0
HOLD2
LOAD2
HOLD3
LX2
D
Q
CD
FD21
QI2
QI3

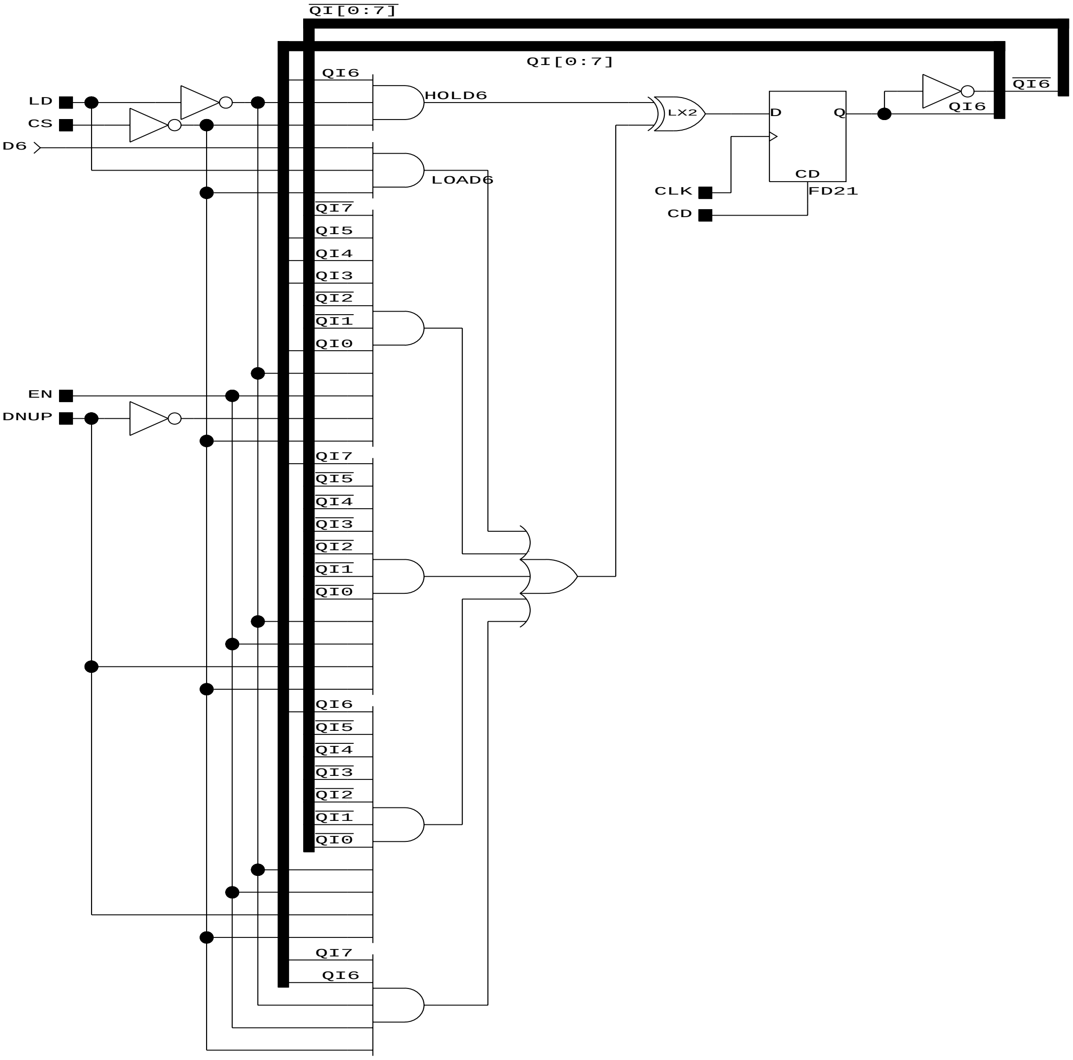
CDUD8.3


$\overline{QI[0:7]}$
QI[0:7]
QI4
LD
CS
D4
HOLD4
LX2
D
Q
CD
FD21
CLK
CD
$\overline{QI4}$
QI4
LOAD4
$\overline{QI7}$
QI3
QI2
QI1
QI0
EN
DNUP
$\overline{QI6}$
$\overline{QI5}$
QI3
QI2
QI1
QI0
$\overline{QI7}$
$\overline{QI3}$
$\overline{QI2}$
$\overline{QI1}$
$\overline{QI0}$
$\overline{QI6}$
$\overline{QI5}$
$\overline{QI3}$
$\overline{QI2}$
$\overline{QI1}$
$\overline{QI0}$
QI7
QI6
QI4
QI7
QI5
QI4

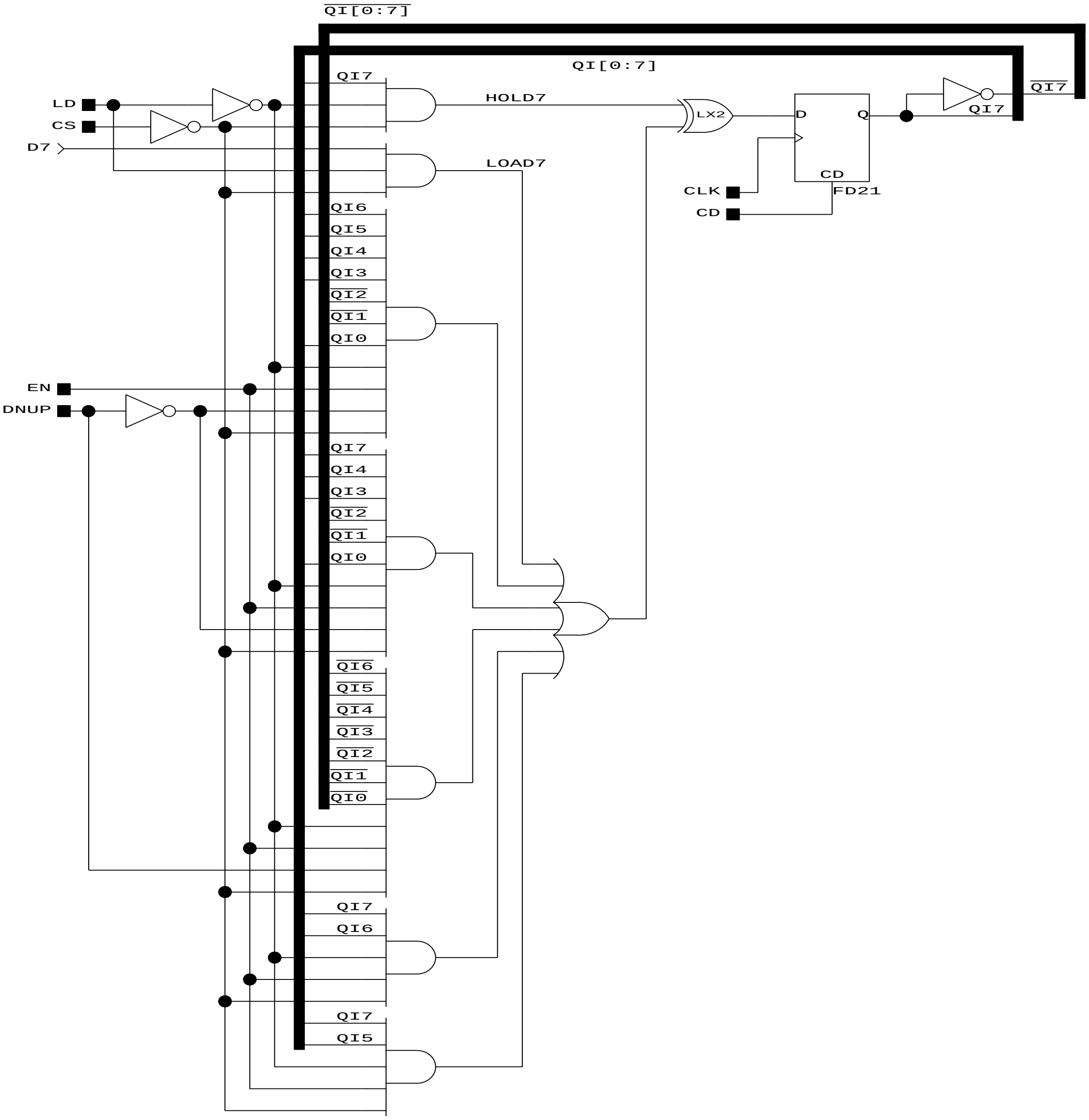
CDUD8.4


QI[0:7]
QI[0:7]
QI5
LD
CS
D5
HOLD5
LOAD5
LX2
D
Q
CD
FD21
CLK
CD
QI5
QI5
QI7
QI4
QI3
QI2
QI1
QI0
EN
DNUP
QI5
QI4
QI3
QI2
QI1
QI0
QI7
QI6
QI4
QI3
QI2
QI1
QI0
QI7
QI6
QI4
QI3
QI2
QI1
QI0
QI7
QI5

CDUD8.5

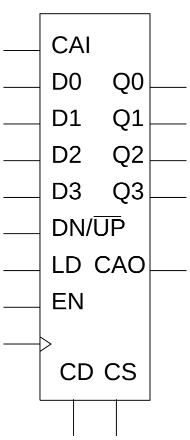

QI[0:7]
QI[0:7]
QI6
HOLD6
LX2
D
Q
QI6
QI6
LD
CS
D6
LOAD6
CD
CLK
CD
FD21
QI7
QI5
QI4
QI3
QI2
QI1
QI0
EN
DNUP
QI7
QI5
QI4
QI3
QI2
QI1
QI0
QI6
QI5
QI4
QI3
QI2
QI1
QI0
QI7
QI6

CDUD8.6

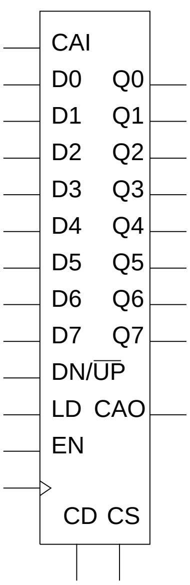

$\overline{QI[0:7]}$
QI[0:7]
LD
CS
D7
QI7
HOLD7
LOAD7
LX2
D
Q
CD
FD21
$\overline{QI7}$
QI7
CLK
CD
QI6
QI5
QI4
QI3
$\overline{QI2}$
$\overline{QI1}$
QI0
EN
DNUP
QI7
QI4
QI3
$\overline{QI2}$
$\overline{QI1}$
QI0
$\overline{QI6}$
$\overline{QI5}$
$\overline{QI4}$
$\overline{QI3}$
$\overline{QI2}$
$\overline{QI1}$
$\overline{QI0}$
QI7
QI6
QI7
QI5

CDUD4c and CDUD8c

CDUD4c



CDUD8c



Function:

4- and 8-bit decade up/down counters with asynchronous clear, synchronous clear, enable, parallel data load, CAI, and CAO.

Availability:

CDUD4c and CDUD8c can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Schematics appear on the following pages.

Type: Hard

Logic Resources:

Macro	PT	GLB	Output	Level
CDUD4c	*	2	5	1***
CDUD8c	**	4	9	1***

* CLK: 1 PT per GLB if Product Term Clock is used.
CAO: 2 PT CD: 1 PT per GLB.
Q0: 5 PT Q1: 7 PT
Q2: 6 PT Q3: 7 PT

** CLK: 1 PT per GLB if Product Term Clock is used.
CAO: 2 PT CD: 1 PT per GLB.
Q0: 5 PT Q1: 7 PT Q2: 6 PT
Q3: 7 PT Q4: 8 PT Q5: 7 PT
Q6: 6 PT Q7: 7 PT

*** (CAO is a 2-level output).

Macro Port Definition:

```
CDUD4c ([Q0..Q3],CAO,[D0..D3],CAI,CLK,LD,EN,DNUP,CD,CS);
  CDUD4c_1 ([Q0..Q2],[D0..D2],Q3,CAI,CLK,LD,EN,DNUP,CD,CS);
  CDUD4c_2 (Q3,CAO,D3,[Q0..Q2],CAI,CLK,LD,EN,DNUP,CD,CS);
CDUD8c ([Q0..Q7],CAO,[D0..D7],CAI,CLK,LD,EN,DNUP,CD,CS);
  CDUD8c_1 ([Q0..Q2],[D0..D2],Q3,CAI,CLK,LD,EN,DNUP,CD,CS);
  CDUD8c_2 (Q3,Q4,CAO,D3,D4,[Q0..Q2],[Q5..Q7],CAI,CLK,LD,
            EN,DNUP,CD,CS);
  CDUD8c_3 (Q5,Q6,D5,D6,[Q0..Q4],Q7,CAI,CLK,LD,EN,DNUP,CD,CS);
  CDUD8c_4 (Q7,D7,[Q0..Q6],CAI,CLK,LD,EN,DNUP,CD,CS);
```

Counting Ranges:

CDUD4c: 0↔9. CDUD8c: 0↔99.

Truth Table:

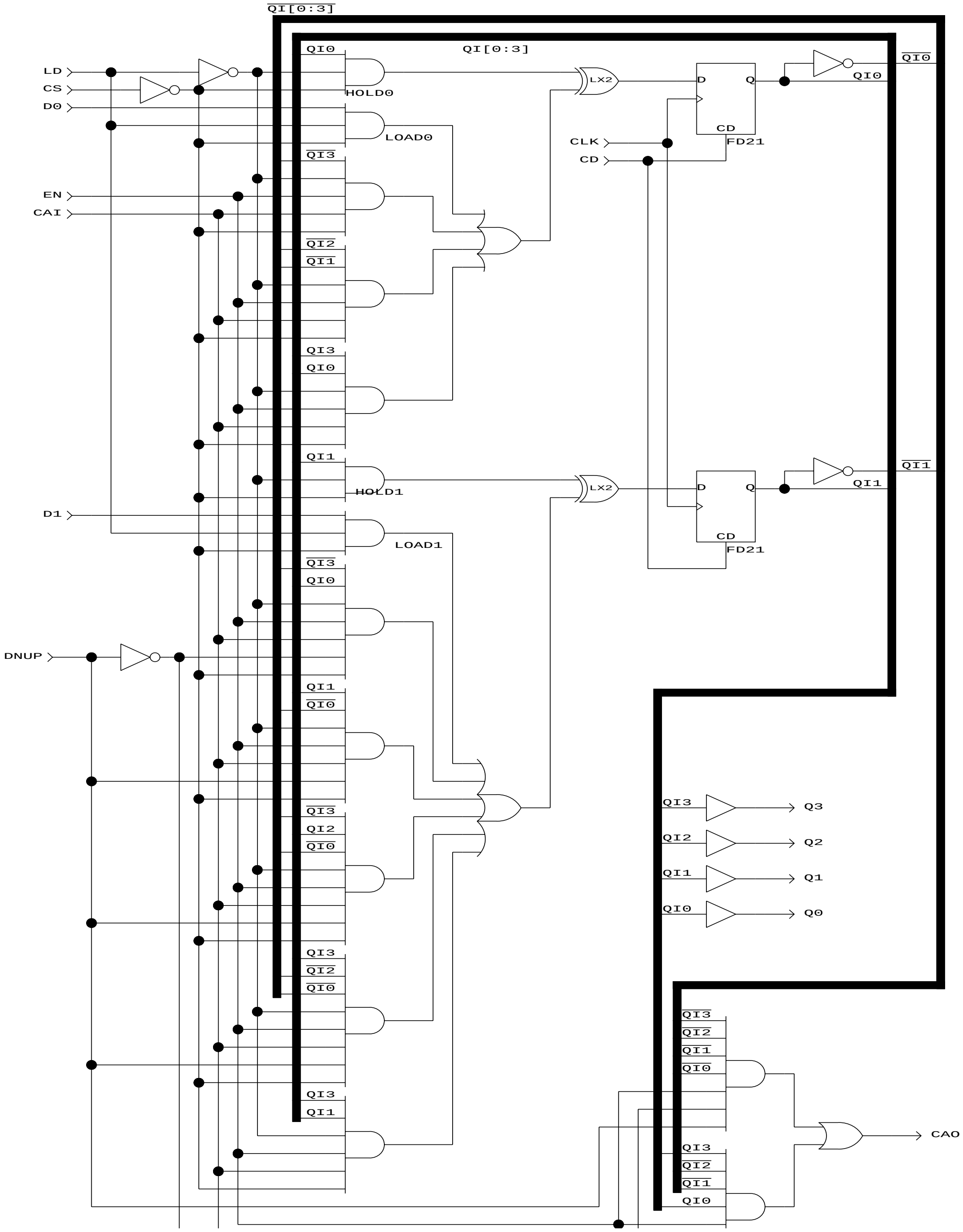
Input								Output	
CD	**CS**	**LD**	**D**	**EN**	**CAI**	**DNUP**	**CLK**	**Q**	**CAO**
1	0	x	x	x	x	x	x	0	*
0	1	x	x	x	x	x	↑	0	*
0	0	1	d	x	x	x	↑	d	**
0	0	0	x	0	x	x	x	Q	0
0	0	0	x	x	0	x	x	Q	0
0	0	0	x	1	1	0	↑	count up	0
0	0	0	x	1	1	1	↑	count down	***

* CAO = CAI·EN·DNUP

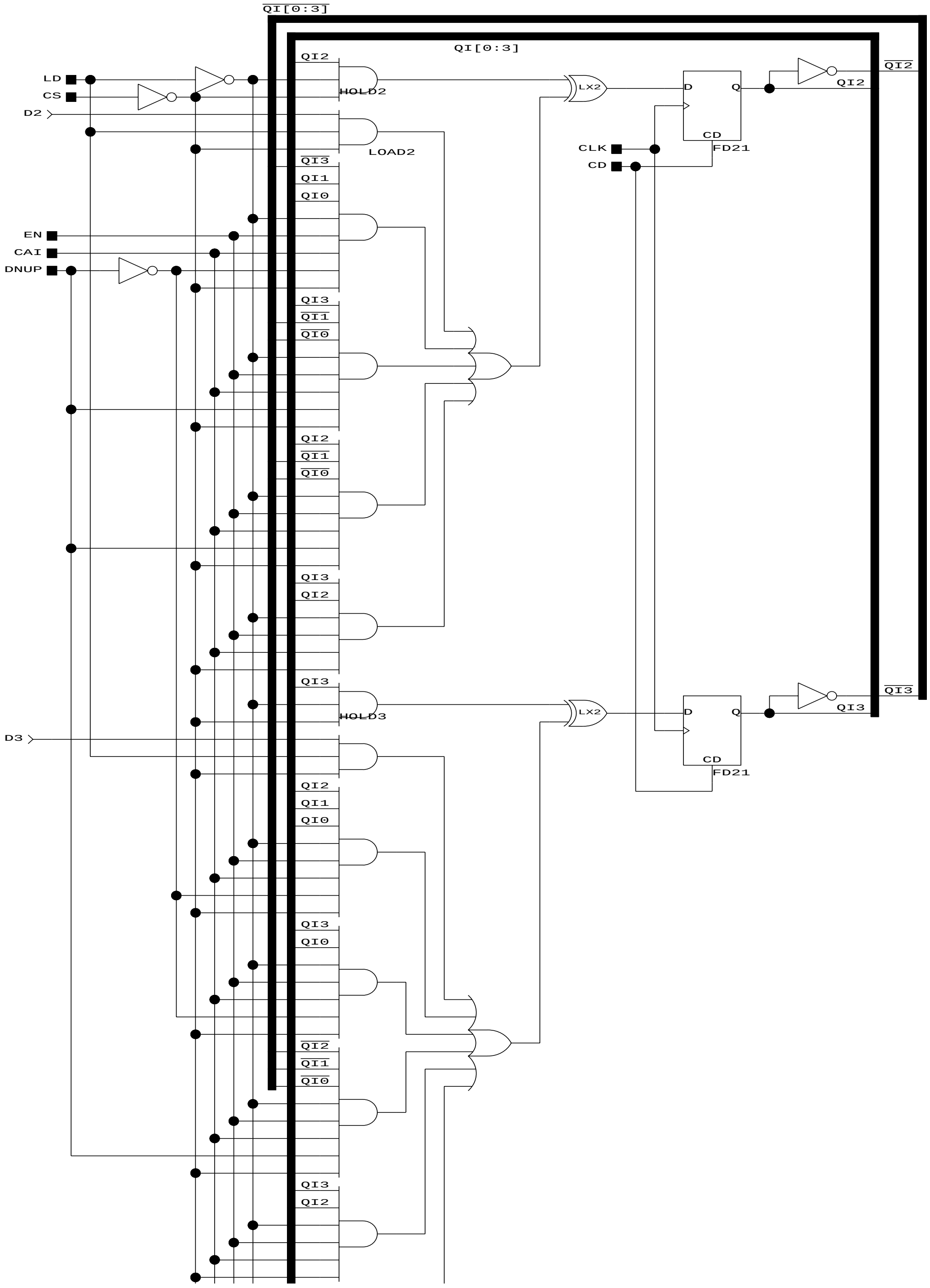
** CDUD4c: CAO = $\mathrm{CAI}\cdot\mathrm{EN}\cdot\mathrm{DNUP}\cdot\overline{\mathrm{D0}}\cdot\overline{\mathrm{D1}}\cdot\overline{\mathrm{D2}}\cdot\overline{\mathrm{D3}}+\overline{\mathrm{DNUP}}\cdot 9$
CDUD8c: CAO = $\mathrm{CAI}\cdot\mathrm{EN}\cdot\mathrm{DNUP}\cdot\overline{\mathrm{D0}}\cdot\overline{\mathrm{D1}}\cdot\overline{\mathrm{D2}}\cdot\overline{\mathrm{D3}}\cdot\overline{\mathrm{D4}}\cdot\overline{\mathrm{D5}}\cdot\overline{\mathrm{D6}}\cdot\overline{\mathrm{D7}}+\overline{\mathrm{DNUP}}\cdot 99$

*** CAO = 1 after terminal count (9 or 99) when CAI = 1 and EN = 1.
terminal count = 0 when DNUP = 1 (count down).
terminal count = 9 or 99 when DNUP=0 (count up).
Valid states for each 4-bit digit are 0~9.
Loading higher hexadecimal input values (A-F) clears that decimal output digit on the next clock pulse.
d = any pattern of 1s and 0s on an input or set of inputs,
Q = output of flip-flop or latch, x = don't care, ↑ = rising clock edge.

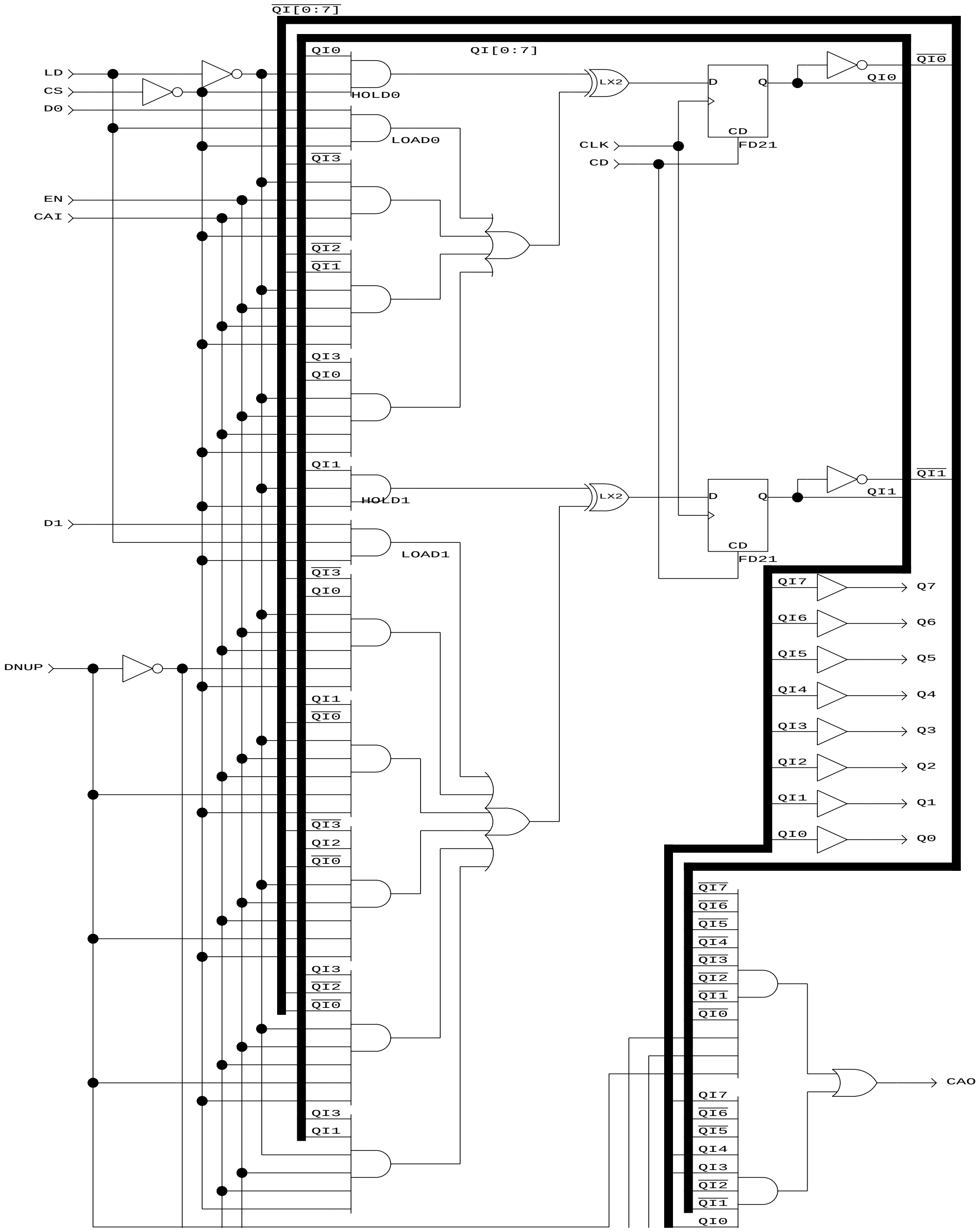
CDUD4c.1


QI[0:3]
QI[0:3]
LD
CS
D0
EN
CAI
D1
DNUP
CLK
CD
HOLD0
LOAD0
HOLD1
LOAD1
LX2
FD21
D
Q
CD
QI0
QI1
QI2
QI3
Q3
Q2
Q1
Q0
CA0

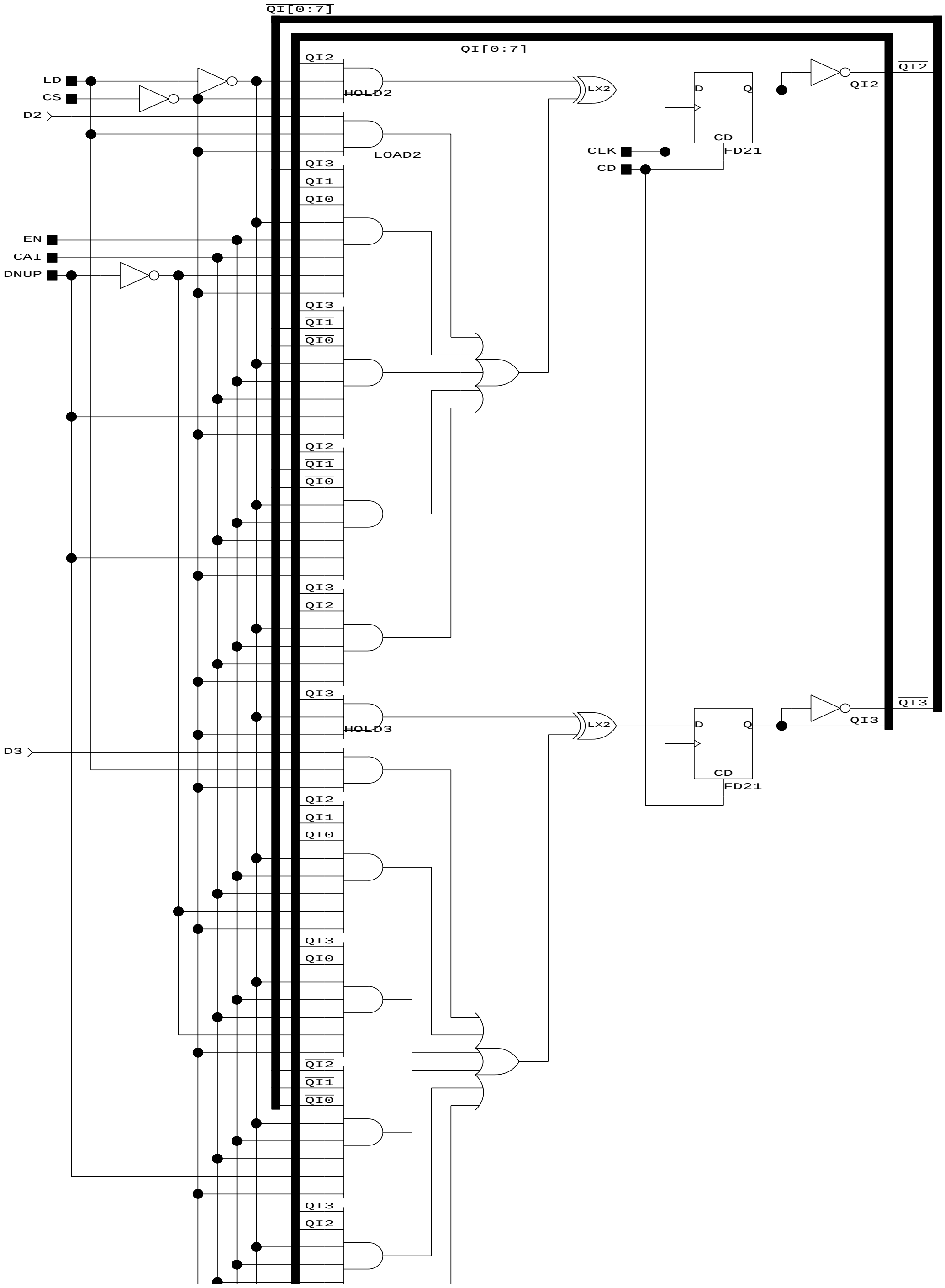
CDUD4c.2


QI[0:3]
QI[0:3]
QI2
LD
CS
D2
HOLD2
LOAD2
LX2
D
Q
CD
FD21
CLK
CD
QI2
QI2
QI3
QI1
QI0
EN
CAI
DNUP
QI3
QI1
QI0
QI2
QI1
QI0
QI3
QI2
QI3
HOLD3
D3
LX2
D
Q
CD
FD21
QI3
QI3
QI2
QI1
QI0
QI3
QI0
QI2
QI1
QI0
QI3
QI2

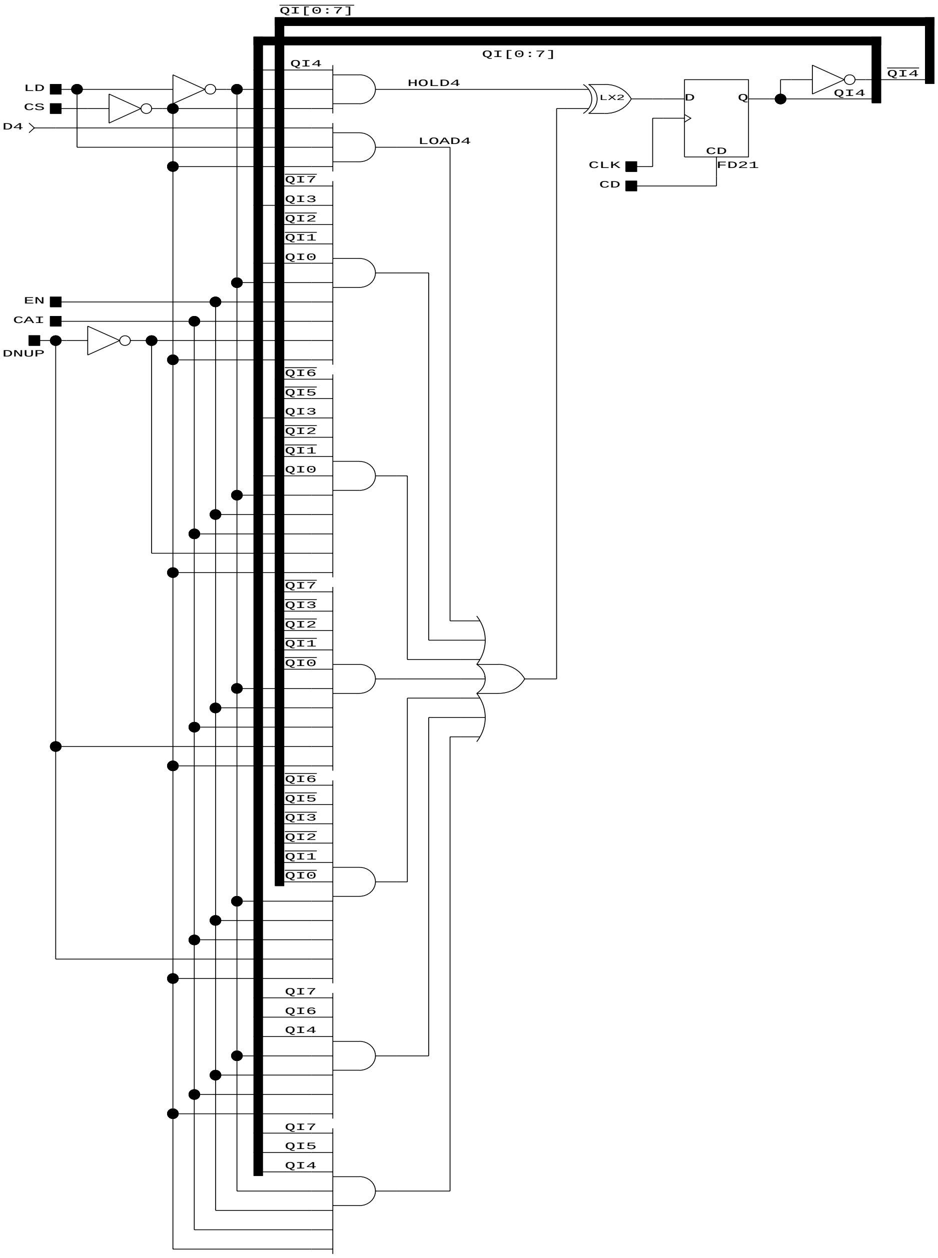
CDUD8c.1


QI[0:7]
QI0
QI[0:7]
LD
CS
D0
HOLD0
LX2
D
Q
QI0
QI0
CD
FD21
CLK
CD
LOAD0
QI3
EN
CAI
QI2
QI1
QI3
QI0
QI1
HOLD1
LX2
D
Q
QI1
QI1
CD
FD21
D1
LOAD1
QI3
QI0
QI7
Q7
QI6
Q6
QI5
Q5
QI4
Q4
QI3
Q3
QI2
Q2
QI1
Q1
QI0
Q0
DNUP
QI1
QI0
QI3
QI2
QI0
QI7
QI6
QI5
QI4
QI3
QI2
QI1
QI0
QI3
QI2
QI0
CAO
QI7
QI6
QI5
QI4
QI3
QI2
QI1
QI0
QI3
QI1

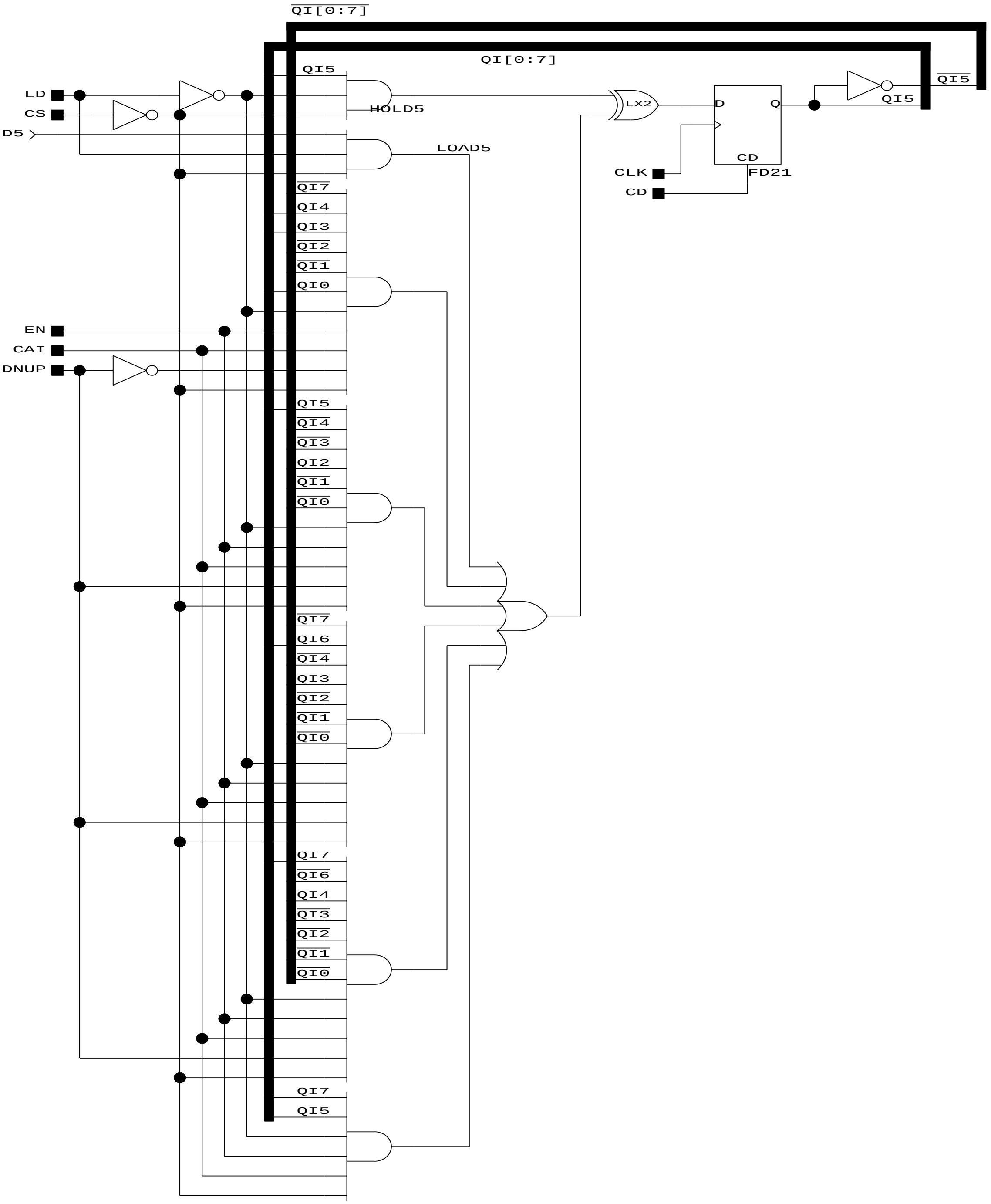
CDUD8c.2


$\overline{QI[0:7]}$
QI[0:7]
QI2
LD
CS
D2
HOLD2
LX2
D
Q
$\overline{QI2}$
QI2
CD
FD21
CLK
CD
LOAD2
$\overline{QI3}$
QI1
QI0
EN
CAI
DNUP
QI3
$\overline{QI1}$
$\overline{QI0}$
QI2
$\overline{QI1}$
$\overline{QI0}$
QI3
QI2
QI3
HOLD3
LX2
D
Q
$\overline{QI3}$
QI3
D3
CD
FD21
QI2
QI1
QI0
QI3
QI0
$\overline{QI2}$
$\overline{QI1}$
$\overline{QI0}$
QI3
QI2

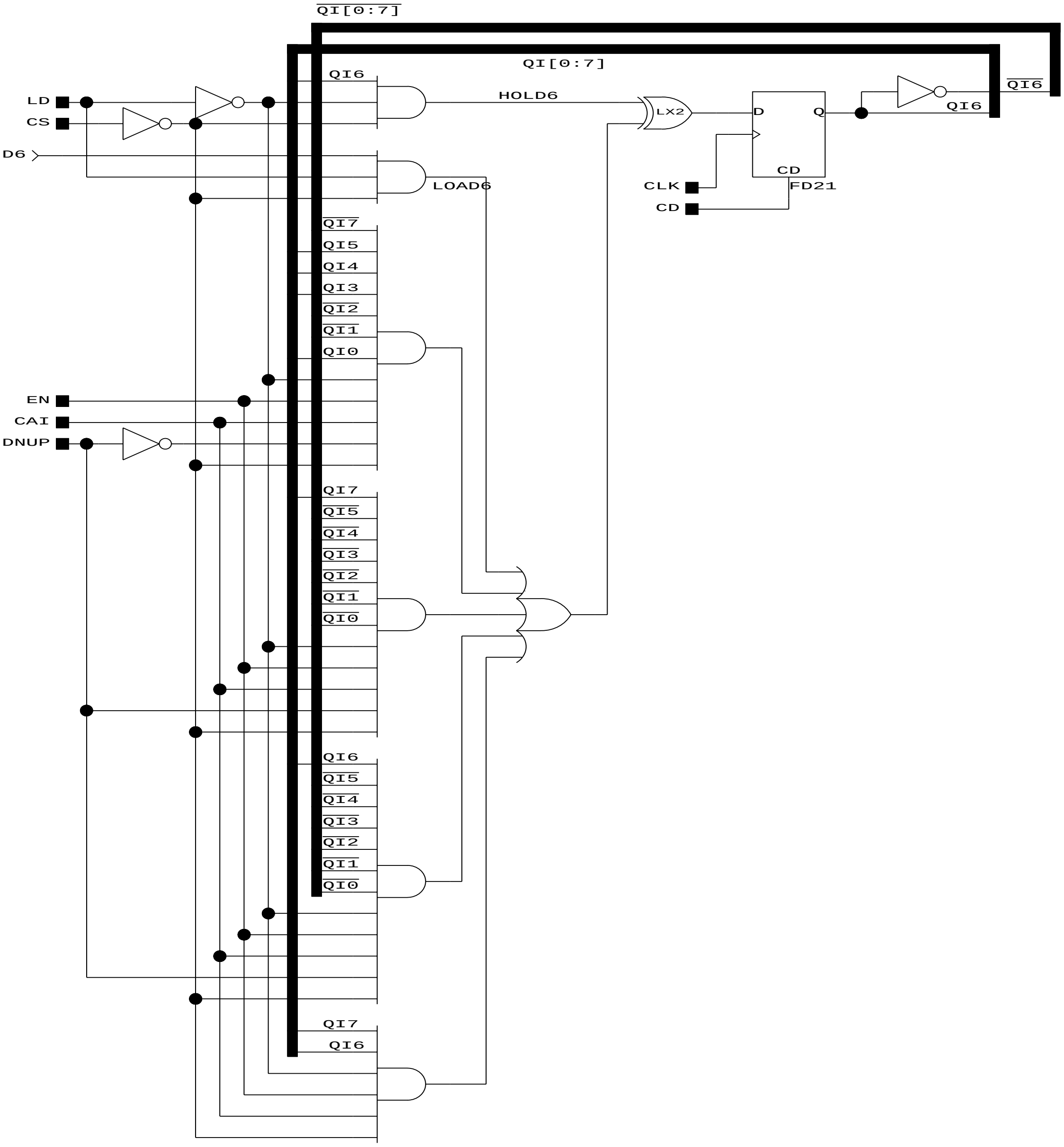
CDUD8c.3


QI[0:7]
QI[0:7]
QI4
HOLD4
LD
CS
D4
LOAD4
LX2
D
Q
CD
FD21
CLK
CD
QI4
QI4
QI7
QI3
QI2
QI1
QI0
EN
CAI
DNUP
QI6
QI5
QI3
QI2
QI1
QI0
QI7
QI3
QI2
QI1
QI0
QI6
QI5
QI3
QI2
QI1
QI0
QI7
QI6
QI4
QI7
QI5
QI4

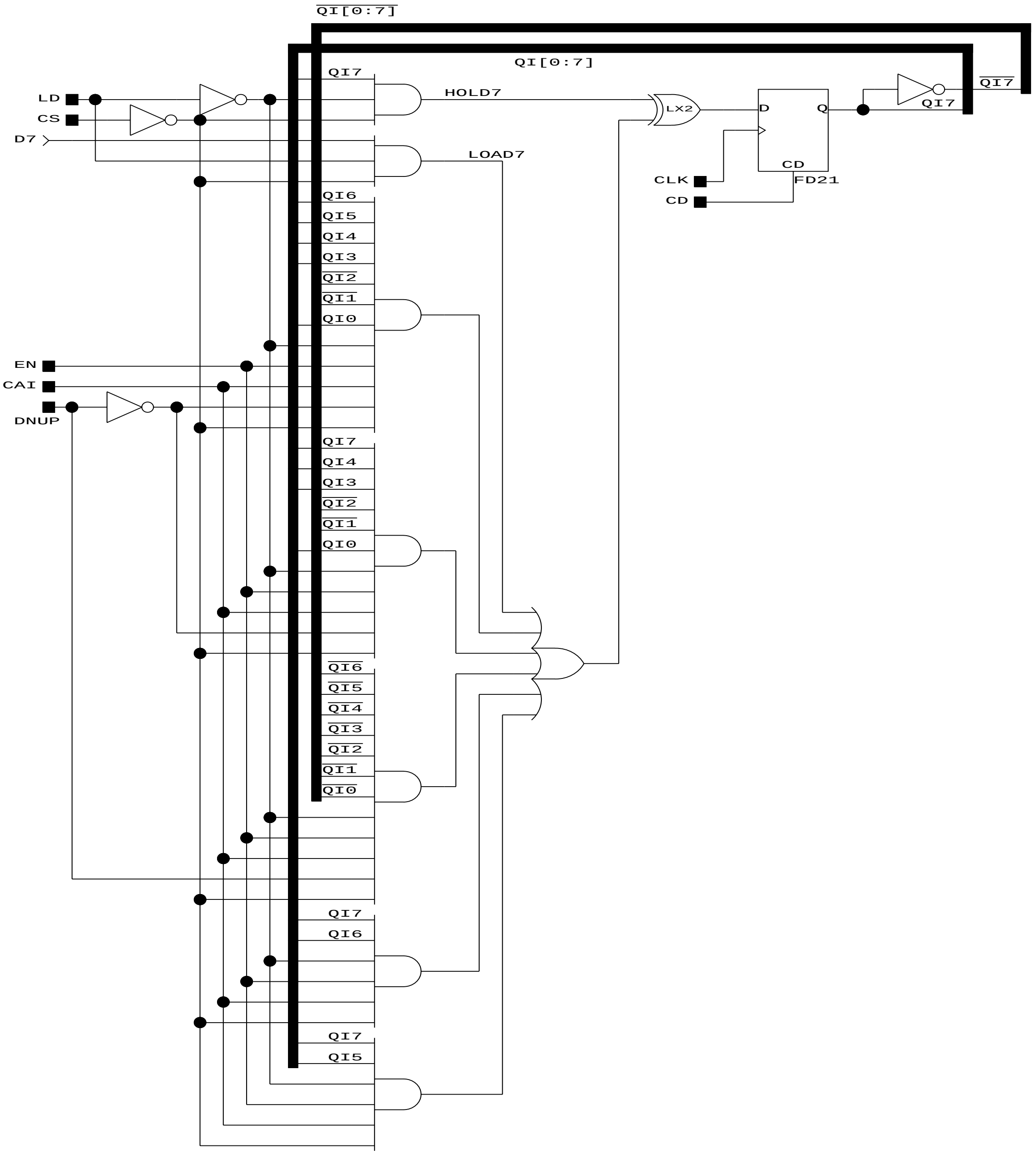
CDUD8c.4


QI[0:7]
QI[0:7]
QI5
LD
CS
D5
HOLD5
LOAD5
LX2
D
Q
CD
FD21
CLK
CD
QI5
QI5
QI7
QI4
QI3
QI2
QI1
QI0
EN
CAI
DNUP
QI5
QI4
QI3
QI2
QI1
QI0
QI7
QI6
QI4
QI3
QI2
QI1
QI0
QI7
QI6
QI4
QI3
QI2
QI1
QI0
QI7
QI5

CDUD8c.5

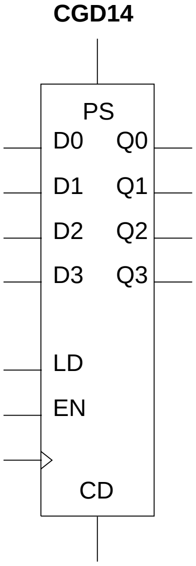

$\overline{\text{QI[0:7]}}$
QI[0:7]
QI6
HOLD6
LX2
D
Q
$\overline{\text{QI6}}$
QI6
LD
CS
D6
LOAD6
CD
FD21
CLK
CD
$\overline{\text{QI7}}$
QI5
QI4
QI3
$\overline{\text{QI2}}$
$\overline{\text{QI1}}$
QI0
EN
CAI
DNUP
QI7
$\overline{\text{QI5}}$
$\overline{\text{QI4}}$
$\overline{\text{QI3}}$
$\overline{\text{QI2}}$
$\overline{\text{QI1}}$
$\overline{\text{QI0}}$
QI6
$\overline{\text{QI5}}$
$\overline{\text{QI4}}$
$\overline{\text{QI3}}$
$\overline{\text{QI2}}$
$\overline{\text{QI1}}$
$\overline{\text{QI0}}$
QI7
QI6

CDUD8c.6


$\overline{QI[0:7]}$
QI[0:7]
QI7
LD
CS
D7
HOLD7
LX2
D
Q
$\overline{QI7}$
QI7
CD
FD21
CLK
CD
LOAD7
QI6
QI5
QI4
QI3
$\overline{QI2}$
$\overline{QI1}$
QI0
EN
CAI
DNUP
QI7
QI4
QI3
$\overline{QI2}$
$\overline{QI1}$
QI0
$\overline{QI6}$
$\overline{QI5}$
$\overline{QI4}$
$\overline{QI3}$
$\overline{QI2}$
$\overline{QI1}$
$\overline{QI0}$
QI7
QI6
QI7
QI5

Gray Code Counters

CGD14



Function:

4-bit gray code down counter with asynchronous clear, synchronous preset, enable, and parallel data load.

Availability:

CGD14 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Schematics appear on the following pages.

Type: Soft

Macro Port Definition:

```
CGD14 ([Q0..Q3],[D0..D3],CLK,PS,LD,EN,CD);
  CGD14_1 (Q0,Q1,D0,D1,Q2,Q3,CLK,PS,LD,EN,CD);
  CGD14_2 (Q2,Q3,D2,D3,Q0,Q1,CLK,PS,LD,EN,CD);
```

Gray Code Pattern: Refer to CGU14.

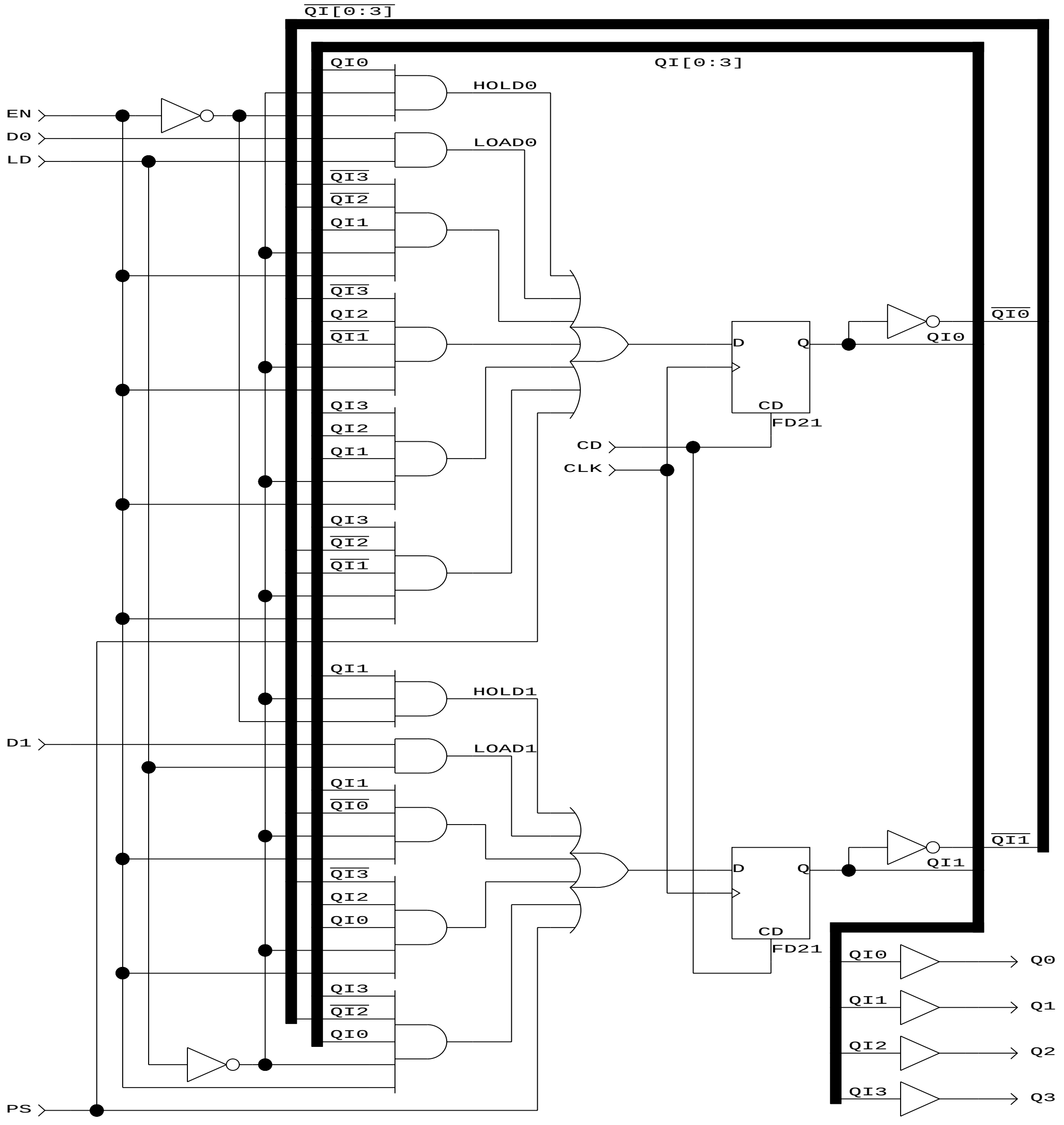
Counting Range: 15-0.

Truth Table:

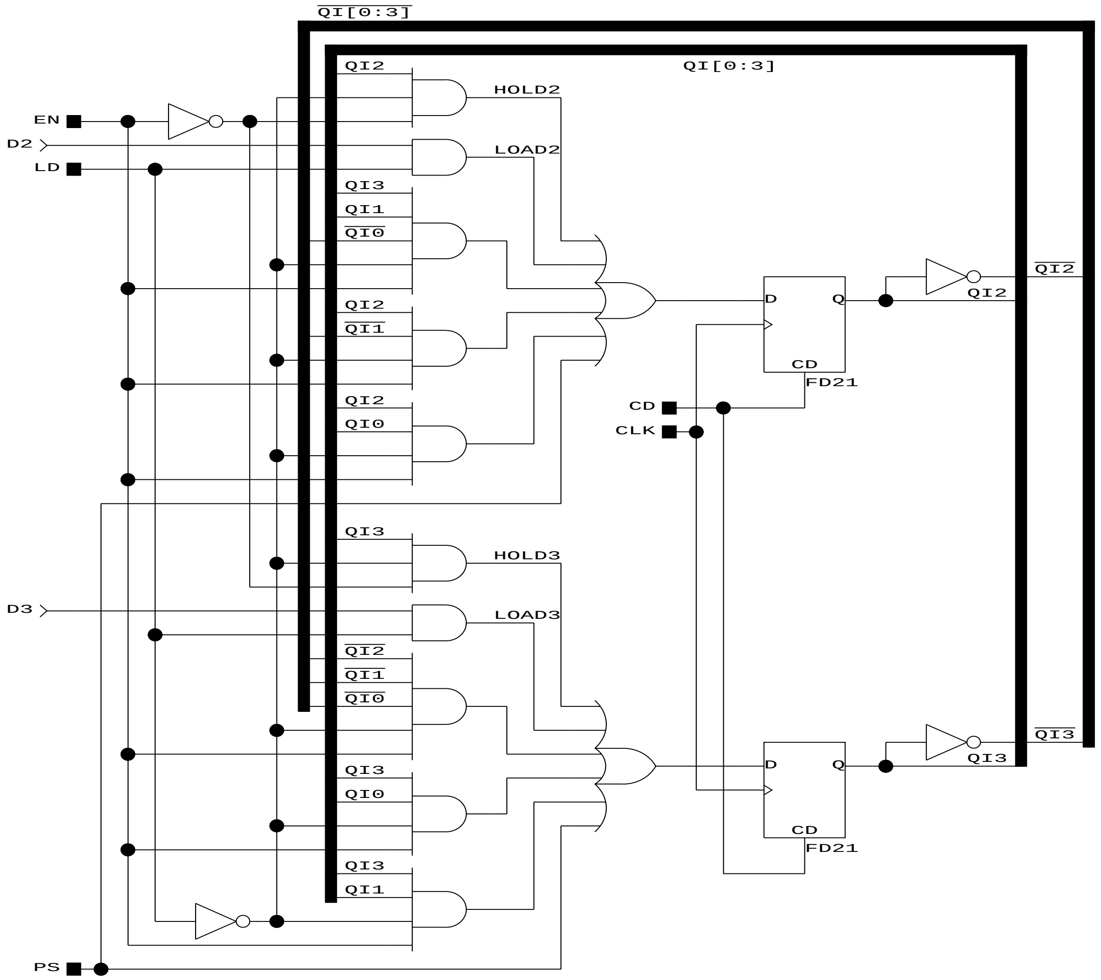
Input						Output
CD	**PS**	**LD**	**D**	**EN**	**CLK**	**Q**
1	x	x	x	x	x	0
0	1	x	x	x	↑	1
0	0	1	d	x	↑	d
0	0	0	x	0	↑	Q
0	0	0	x	1	↑	count down

d = any pattern of 1s and 0s on an input or set of inputs,
Q = output of flip-flop or latch, x = don’t care, ↑ = rising clock edge.

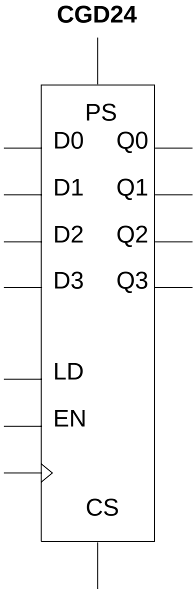
CGD14.1


$\overline{\text{QI[0:3]}}$
QI0
QI[0:3]
HOLD0
EN
D0
LD
LOAD0
$\overline{\text{QI3}}$
$\overline{\text{QI2}}$
QI1
$\overline{\text{QI3}}$
QI2
$\overline{\text{QI1}}$
$\overline{\text{QI0}}$
D
Q
QI0
CD
FD21
QI3
QI2
QI1
CD
CLK
QI3
$\overline{\text{QI2}}$
$\overline{\text{QI1}}$
QI1
HOLD1
D1
LOAD1
QI1
$\overline{\text{QI0}}$
$\overline{\text{QI1}}$
D
Q
QI1
$\overline{\text{QI3}}$
QI2
QI0
CD
FD21
QI0
Q0
QI1
Q1
QI2
Q2
QI3
Q3
QI3
$\overline{\text{QI2}}$
QI0
PS

CGD14.2


$\overline{QI[0:3]}$
QI2
QI[0:3]
HOLD2
EN
D2
LOAD2
LD
QI3
QI1
$\overline{QI0}$
$\overline{QI2}$
D
Q
QI2
QI2
$\overline{QI1}$
CD
FD21
QI2
QI0
CD
CLK
QI3
HOLD3
D3
LOAD3
$\overline{QI2}$
$\overline{QI1}$
$\overline{QI0}$
$\overline{QI3}$
D
Q
QI3
QI3
QI0
CD
FD21
QI3
QI1
PS

CGD24



Function:

4-bit gray code down counter with synchronous clear, synchronous preset, enable, and parallel data load.

Availability:

CGD24 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Schematics appear on the following pages.

Type: Soft

Macro Port Definition:

```
CGD24 ([Q0..Q3],[D0..D3],CLK,PS,LD,EN,CS);
  CGD24_1 (Q0,Q1,D0,D1,Q2,Q3,CLK,PS,LD,EN,CS);
  CGD24_2 (Q2,Q3,D2,D3,Q0,Q1,CLK,PS,LD,EN,CS);
```

Gray Code Pattern: Refer to CGU14.

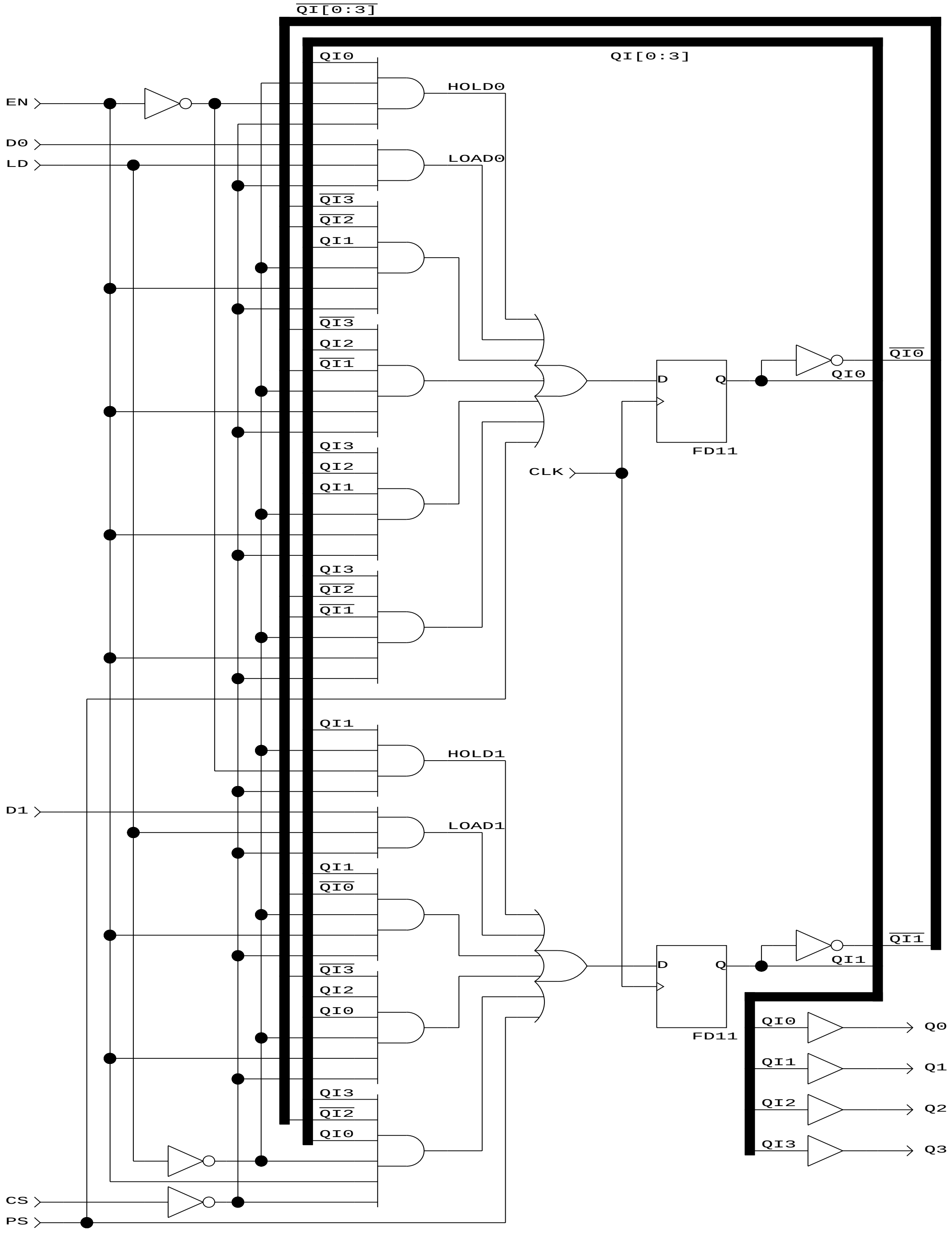
Counting Range: 15-0.

Truth Table:

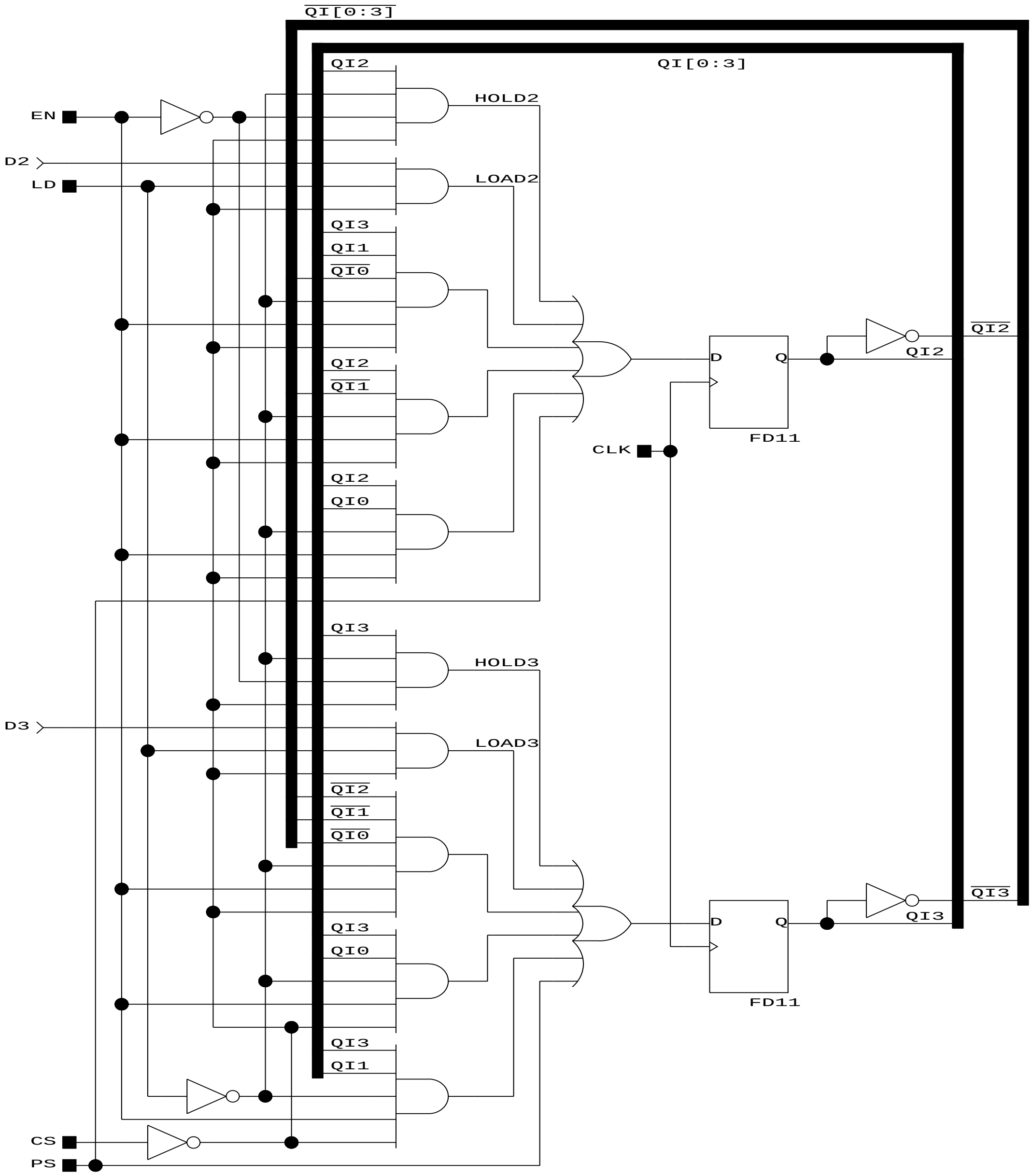
Input						Output
PS	**CS**	**LD**	**D**	**EN**	**CLK**	**Q**
1	x	x	x	x	↑	1
0	1	x	x	x	↑	0
0	0	1	d	x	↑	d
0	0	0	x	0	↑	Q
0	0	0	x	1	↑	count down

d = any pattern of 1s and 0s on an input or set of inputs,
Q = output of flip-flop or latch, x = don’t care,
↑ = rising clock edge.

CGD24.1

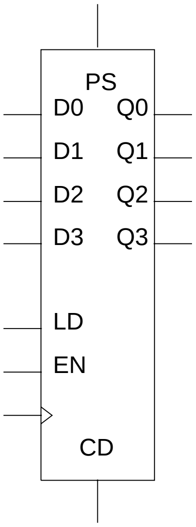

$\overline{QI[0:3]}$
QI0
QI[0:3]
EN
HOLD0
D0
LD
LOAD0
$\overline{QI3}$
$\overline{QI2}$
QI1
$\overline{QI3}$
QI2
$\overline{QI1}$
QI3
QI2
QI1
QI3
$\overline{QI2}$
$\overline{QI1}$
$\overline{QI0}$
D
Q
QI0
FD11
CLK
QI1
HOLD1
D1
LOAD1
QI1
$\overline{QI0}$
$\overline{QI3}$
QI2
QI0
QI3
$\overline{QI2}$
QI0
$\overline{QI1}$
D
Q
QI1
FD11
QI0
Q0
QI1
Q1
QI2
Q2
QI3
Q3
CS
PS

CGD24.2


$\overline{\text{QI[0:3]}}$
QI[0:3]
QI2
EN
HOLD2
D2
LD
LOAD2
QI3
QI1
$\overline{\text{QI0}}$
QI2
$\overline{\text{QI1}}$
QI2
QI0
D
Q
FD11
CLK
$\overline{\text{QI2}}$
QI2
QI3
HOLD3
D3
LOAD3
$\overline{\text{QI2}}$
$\overline{\text{QI1}}$
$\overline{\text{QI0}}$
QI3
QI0
QI3
QI1
CS
PS
D
Q
FD11
$\overline{\text{QI3}}$
QI3

CGU14

CGU14



Function:

4-bit gray code up counter with asynchronous clear, synchronous preset, enable, and parallel data load.

Availability:

CGU14 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Schematics appear on the following pages.

Type: Soft

Gray Code Pattern:

Note that codes for two successive numbers differ by one bit.

Gray Code Pattern									
0	0	0	0	0	8	1	1	0	0
1	0	0	0	1	9	1	1	0	1
2	0	0	1	1	10	1	1	1	1
3	0	0	1	0	11	1	1	1	0
4	0	1	1	0	12	1	0	1	0
5	0	1	1	1	13	1	0	1	1
6	0	1	0	1	14	1	0	0	1
7	0	1	0	0	15	1	0	0	0

Macro Port Definition:

```
CGU14 ([Q0..Q3],[D0..D3],CLK,PS,LD,EN,CD);
  CGU14_1 (Q0,Q1,D0,D1,Q2,Q3,CLK,PS,LD,EN,CD);
  CGU14_2 (Q2,Q3,D2,D3,Q0,Q1,CLK,PS,LD,EN,CD);
```

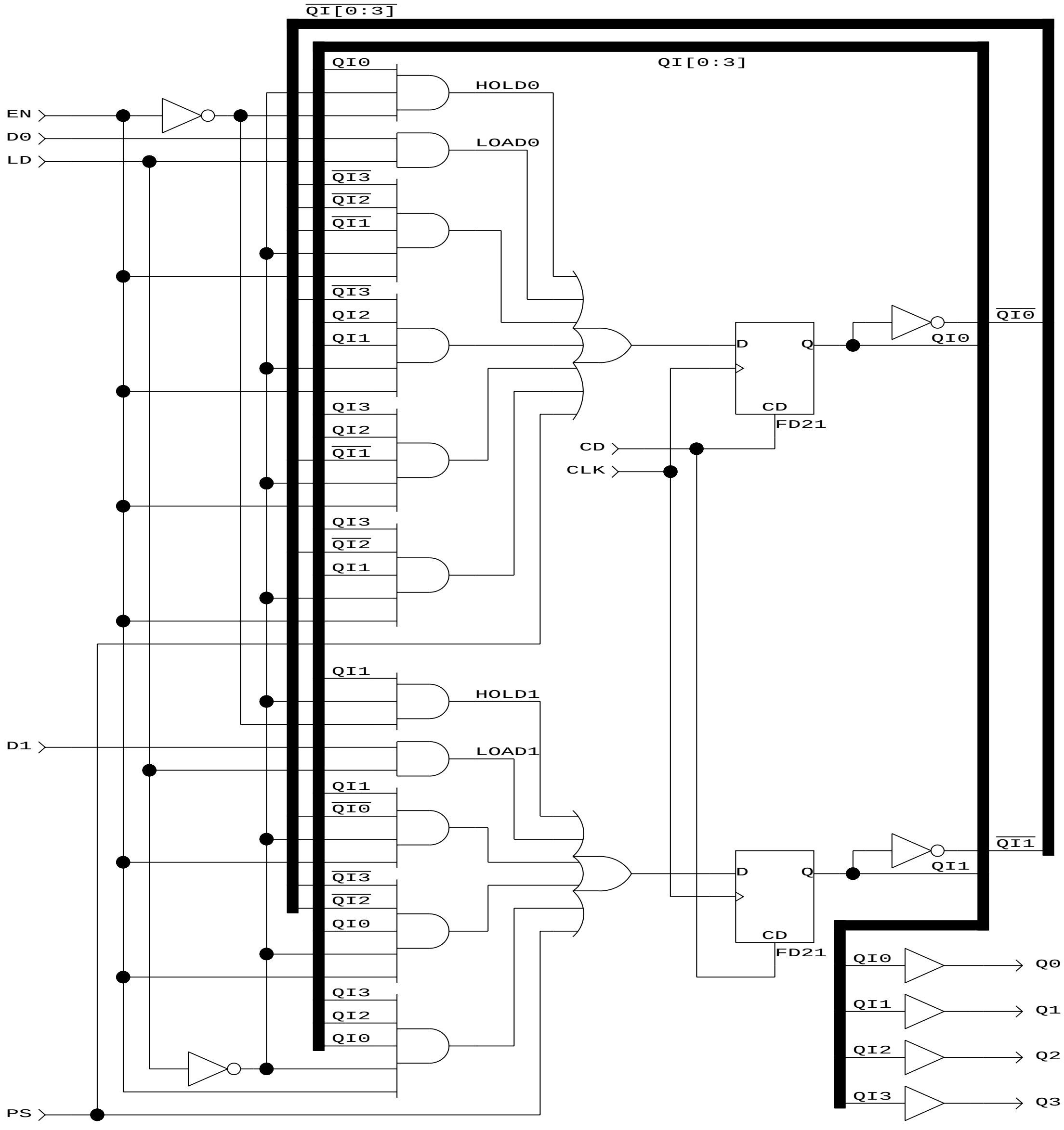
Counting Range: 0-15.

Truth Table:

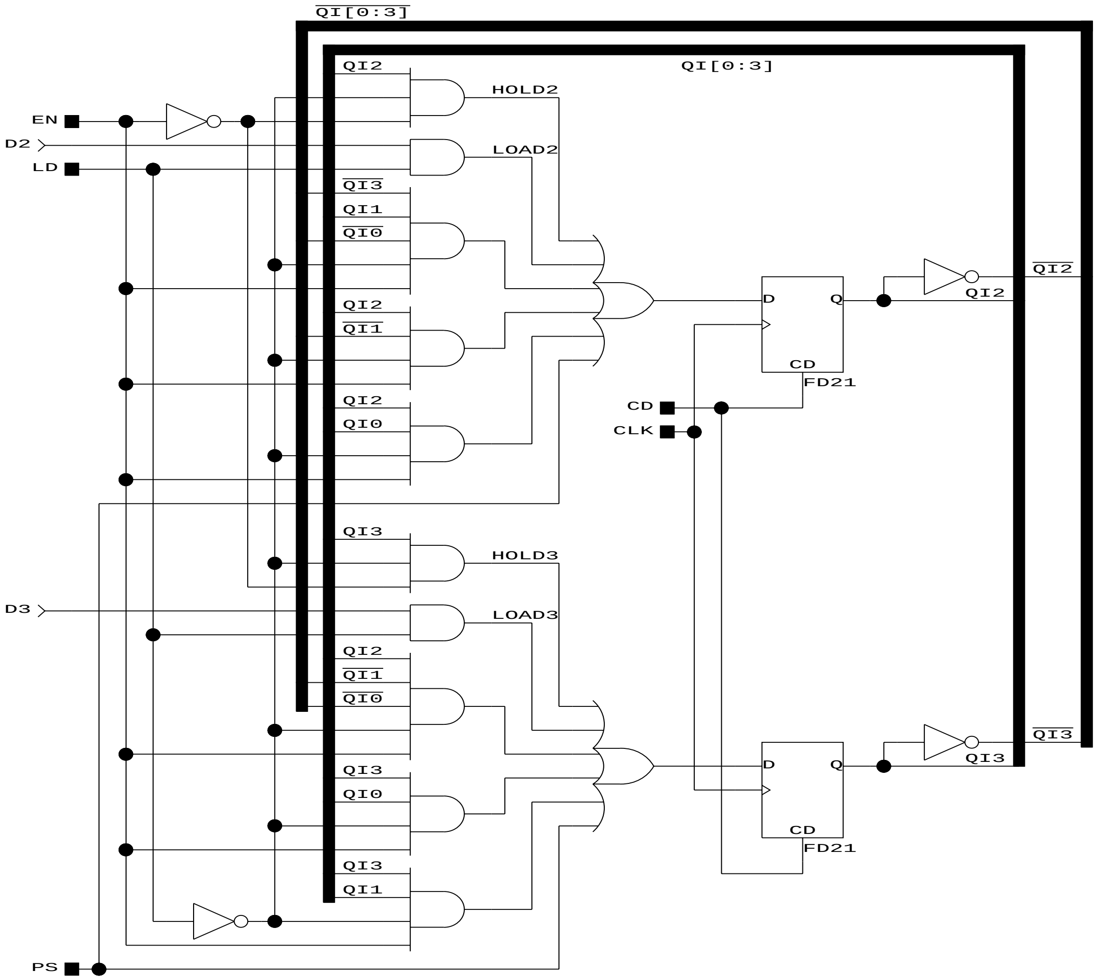
Input						Output
CD	**PS**	**LD**	**D**	**EN**	**CLK**	**Q**
1	x	x	x	x	x	0
0	1	x	x	x	↑	1
0	0	1	d	x	↑	d
0	0	0	x	0	↑	Q
0	0	0	x	1	↑	count up

d = any pattern of 1s and 0s on an input or set of inputs,
Q = output of flip-flop or latch, x = don’t care,
↑ = rising clock edge.

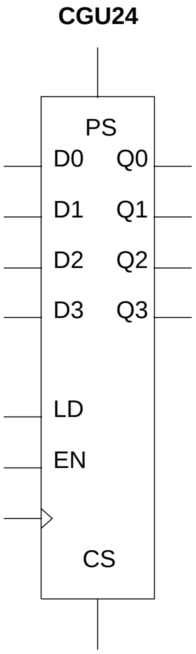
CGU14.1


$\overline{QI[0:3]}$
QI0
QI[0:3]
HOLD0
EN
D0
LD
LOAD0
$\overline{QI3}$
$\overline{QI2}$
$\overline{QI1}$
$\overline{QI3}$
QI2
QI1
QI3
QI2
$\overline{QI1}$
QI3
$\overline{QI2}$
QI1
D
Q
CD
FD21
$\overline{QI0}$
QI0
CD
CLK
QI1
HOLD1
D1
LOAD1
QI1
$\overline{QI0}$
$\overline{QI3}$
$\overline{QI2}$
QI0
QI3
QI2
QI0
PS
D
Q
CD
FD21
$\overline{QI1}$
QI1
QI0
Q0
QI1
Q1
QI2
Q2
QI3
Q3

CGU14.2


$\overline{QI[0:3]}$
QI[0:3]
QI2
HOLD2
EN
D2
LOAD2
LD
$\overline{QI3}$
QI1
$\overline{QI0}$
QI2
$\overline{QI1}$
QI2
QI0
D
Q
CD
FD21
$\overline{QI2}$
QI2
CD
CLK
QI3
HOLD3
D3
LOAD3
QI2
$\overline{QI1}$
$\overline{QI0}$
QI3
QI0
QI3
QI1
D
Q
CD
FD21
$\overline{QI3}$
QI3
PS

CGU24



Function:

4-bit gray code up counter with synchronous clear, synchronous preset, enable, and parallel data load.

Availability:

CGU24 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Schematics appear on the following pages.

Type: Soft

Macro Port Definition:

```
CGU24 ([Q0..Q3],[D0..D3],CLK,PS,LD,EN,CS);
  CGU24_1 (Q0,Q1,D0,D1,Q2,Q3,CLK,PS,LD,EN,CS);
  CGU24_2 (Q2,Q3,D2,D3,Q0,Q1,CLK,PS,LD,EN,CS);
```

Gray Code Pattern: Refer to CGU14.

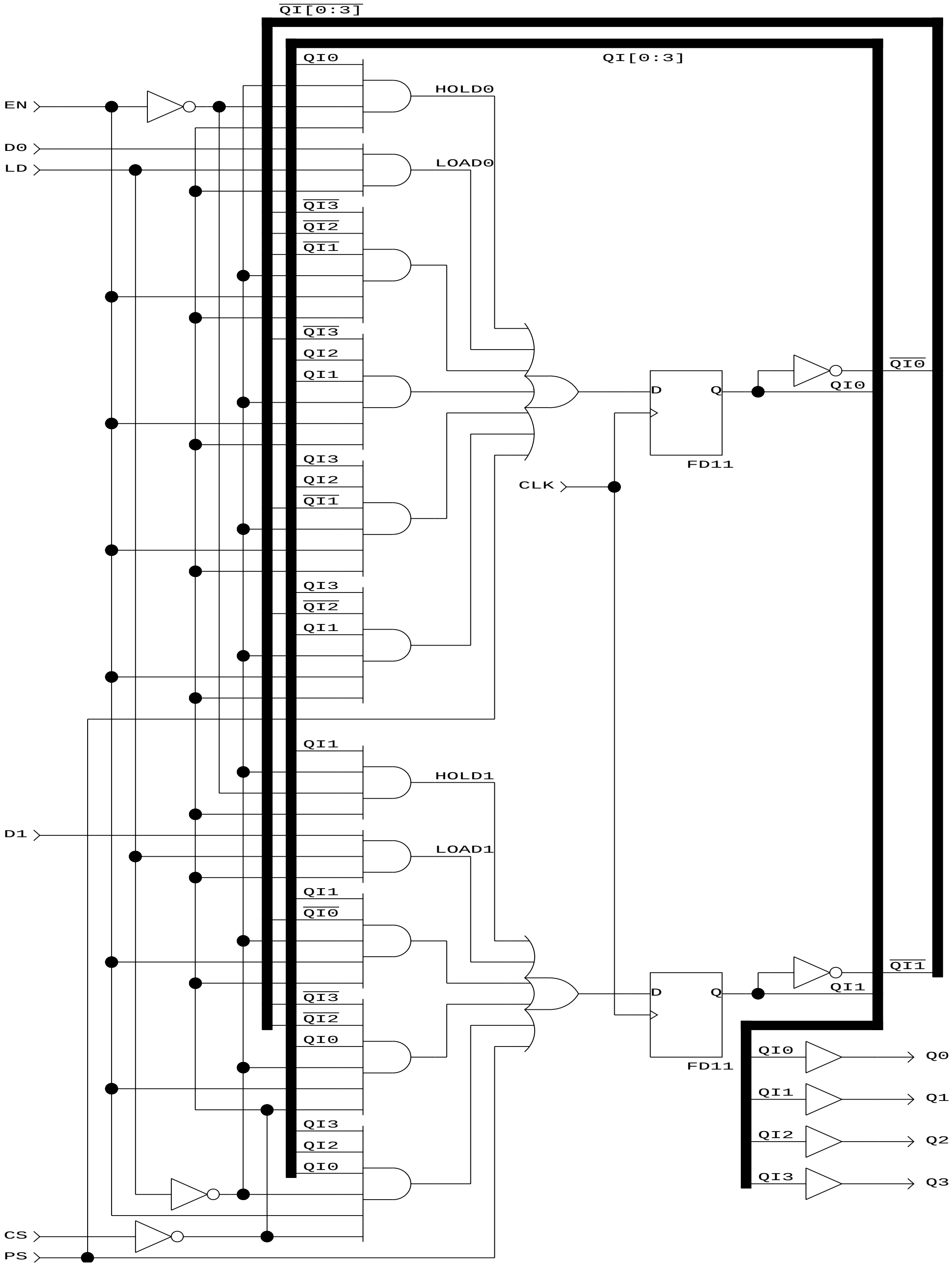
Counting Range: 0-15.

Truth Table:

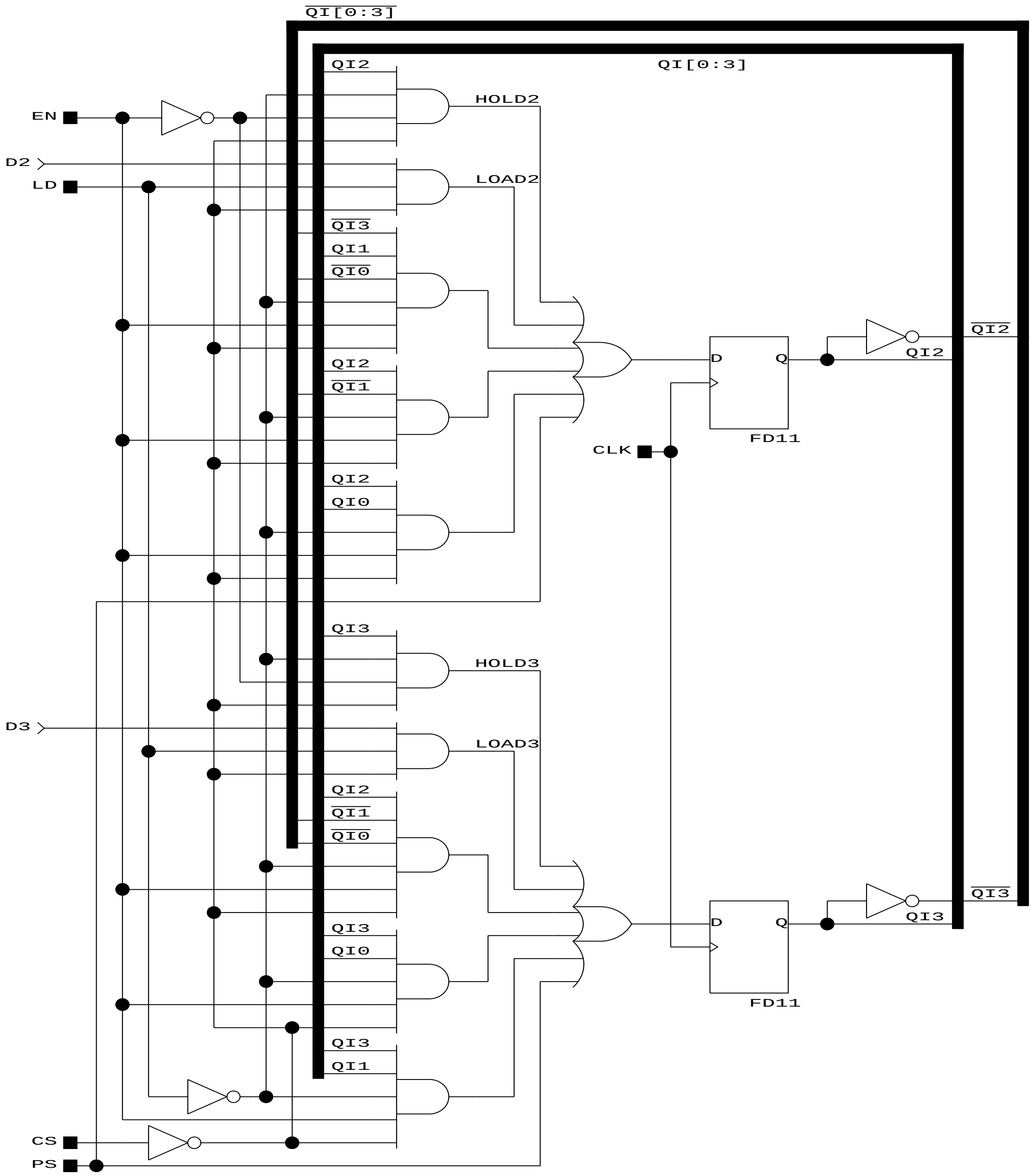
Input						Output
PS	**CS**	**LD**	**D**	**EN**	**CLK**	**Q**
1	x	x	x	x	↑	1
0	1	x	x	x	↑	0
0	0	1	d	x	↑	d
0	0	0	x	0	↑	Q
0	0	0	x	1	↑	count up

d = any pattern of 1s and 0s on an input or set of inputs,
Q = output of flip-flop or latch, x = don’t care,
↑ = rising clock edge.

CGU24.1

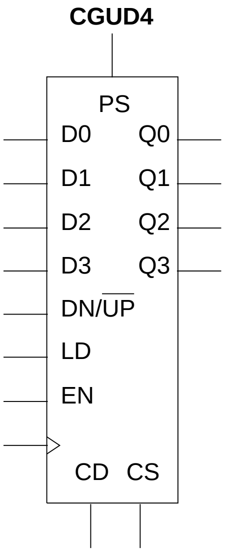

$\overline{QI[0:3]}$
QI0
QI[0:3]
HOLD0
EN
D0
LD
LOAD0
$\overline{QI3}$
$\overline{QI2}$
$\overline{QI1}$
$\overline{QI3}$
QI2
QI1
$\overline{QI0}$
D
Q
QI0
QI3
QI2
$\overline{QI1}$
FD11
CLK
QI3
$\overline{QI2}$
QI1
QI1
HOLD1
D1
LOAD1
QI1
$\overline{QI0}$
$\overline{QI1}$
D
Q
QI1
$\overline{QI3}$
$\overline{QI2}$
QI0
QI0
Q0
FD11
QI1
Q1
QI2
Q2
QI3
QI2
QI0
QI3
Q3
CS
PS

CGU24.2



QI[0:3]
QI[0:3]
QI2
EN
D2
LD
HOLD2
LOAD2
QI3
QI1
QI0
QI2
QI1
QI2
QI0
D
Q
FD11
CLK
QI2
QI2
QI3
HOLD3
D3
LOAD3
QI2
QI1
QI0
QI3
QI0
QI3
QI1
D
Q
FD11
QI3
QI3
CS
PS

CGUD4



Function:

4-bit gray code up/down counter with asynchronous clear, synchronous clear and preset, enable, and parallel data load.

Availability:

CGUD4 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Schematics appear on the following pages.

Type: Soft

Macro Port Definition:

```
CGUD4 ([Q0..Q3],[D0..D3],CLK,PS,LD,EN,DNUP,CD,CS);
  CGUD4_1 (Q0,Q1,D0,D1,Q2,Q3,CLK,PS,LD,EN,DNUP,CD,CS);
  CGUD4_2 (Q2,Q3,D2,D3,Q0,Q1,CLK,PS,LD,EN,DNUP,CD,CS);
```

Gray Code Pattern: Refer to CGU14.

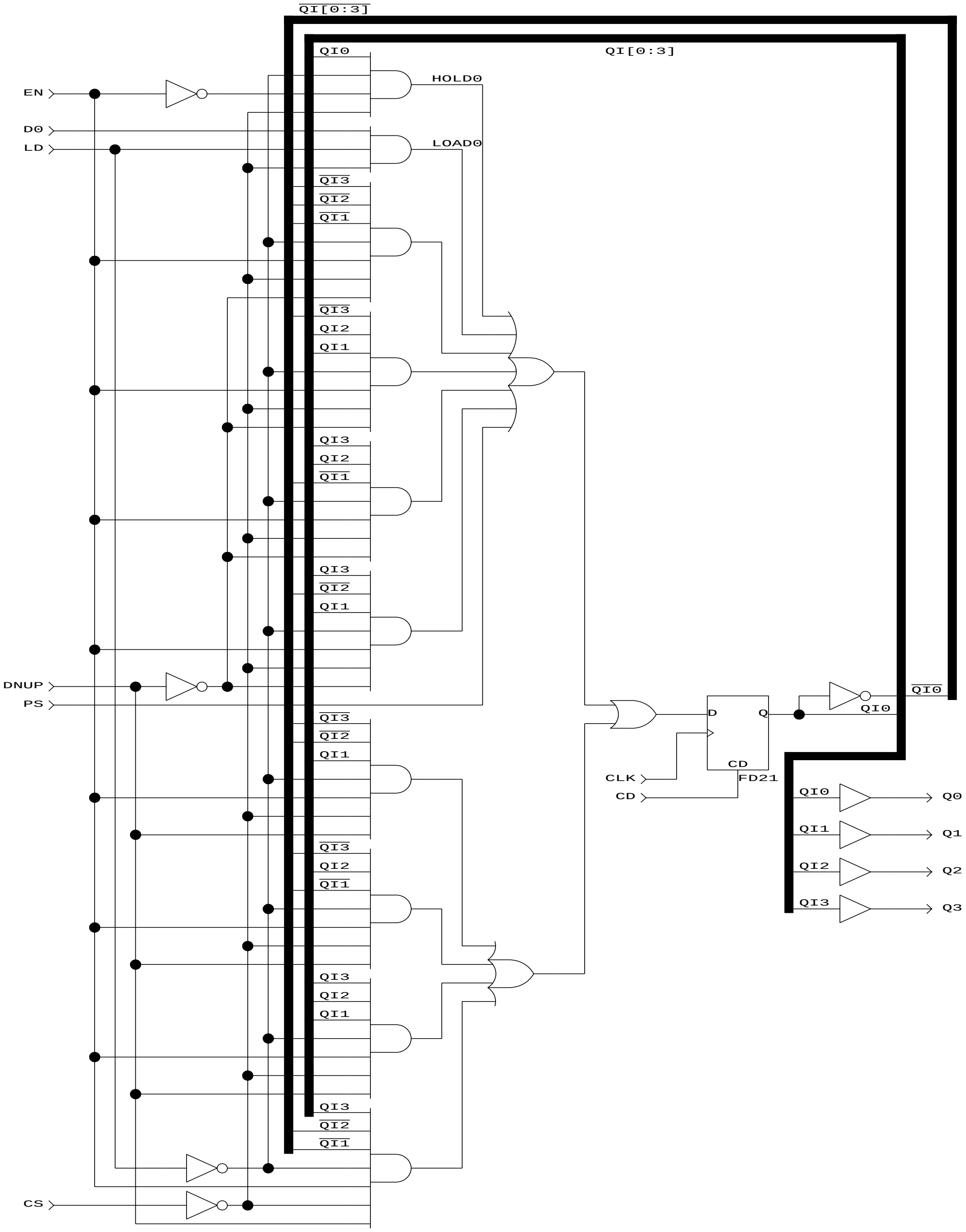
Counting Range: 0↔15.

Truth Table:

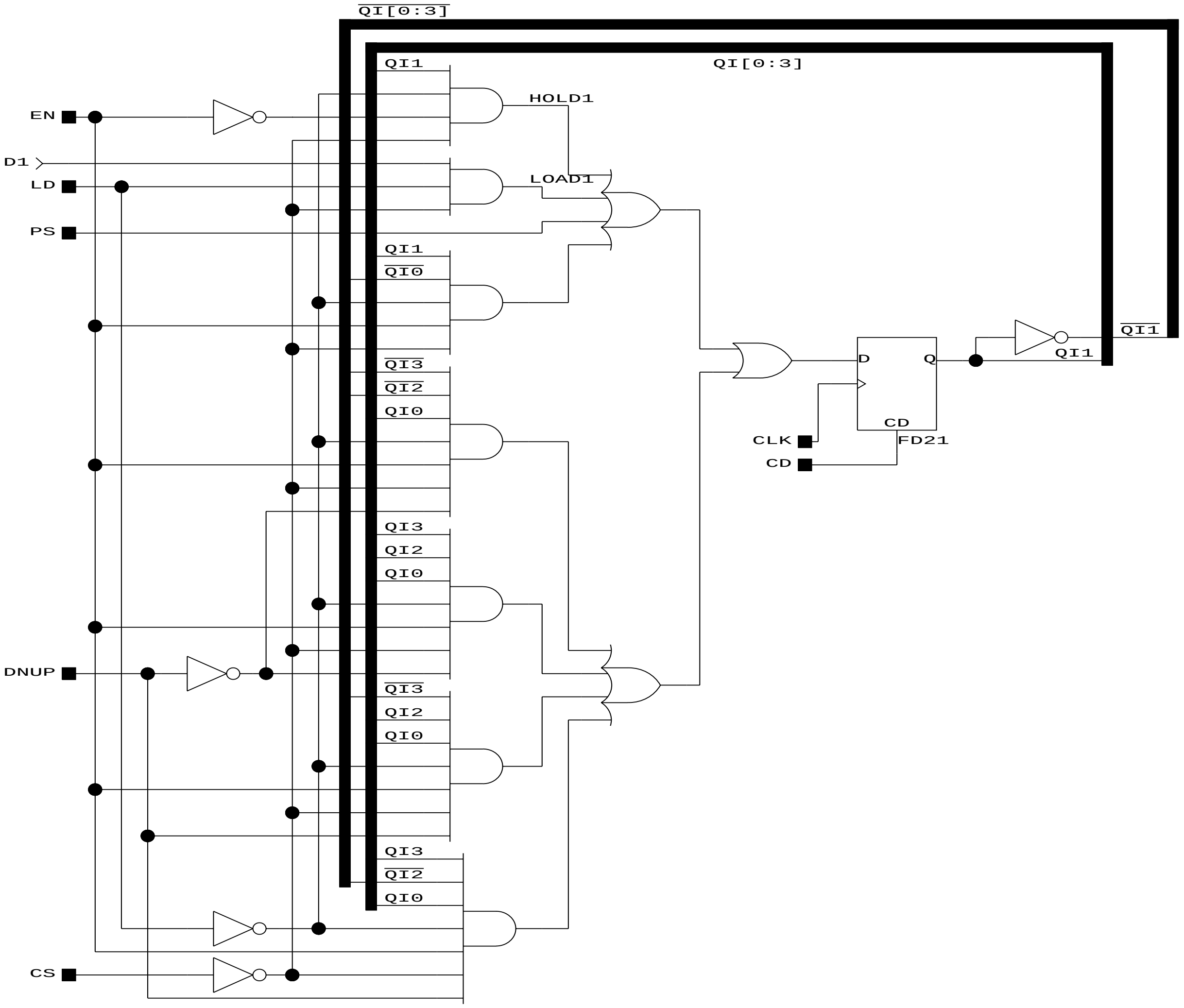
Input								Output
CD	**PS**	**CS**	**LD**	**D**	**DNUP**	**EN**	**CLK**	**Q**
1	x	x	x	x	x	x	x	0
0	1	x	x	x	x	x	↑	1
0	0	1	x	x	x	x	↑	0
0	0	0	1	d	x	x	↑	d
0	0	0	0	x	x	0	↑	Q
0	0	0	0	x	1	1	↑	count down
0	0	0	0	x	0	1	↑	count up

d = any pattern of 1s and 0s on an input or set of inputs,
Q = output of flip-flop or latch, x = don’t care,
↑ = rising clock edge.

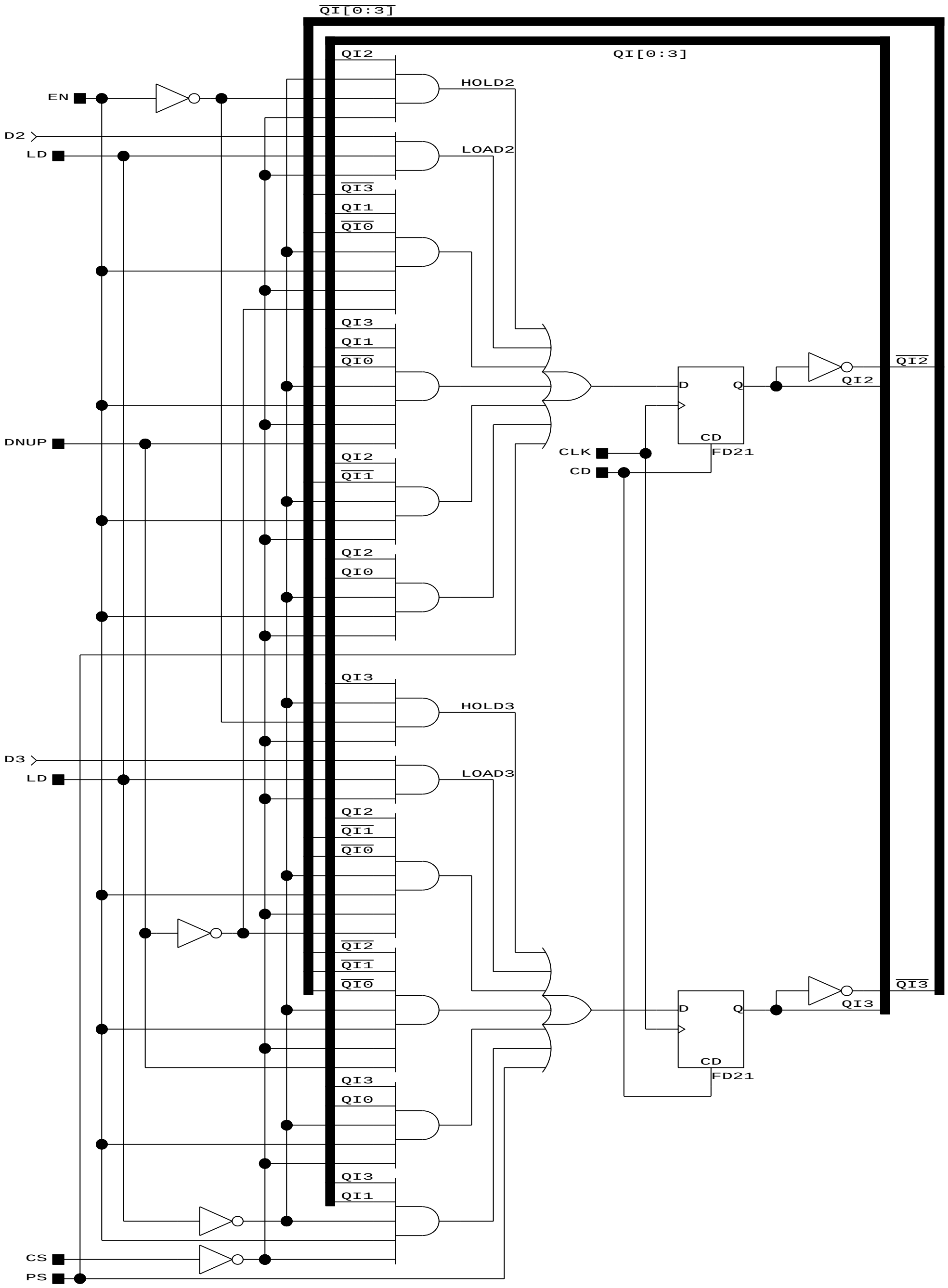
CGUD4.1


$\overline{QI[0:3]}$
QI0
QI[0:3]
HOLD0
EN
D0
LD
LOAD0
$\overline{QI3}$
$\overline{QI2}$
$\overline{QI1}$
$\overline{QI3}$
QI2
QI1
QI3
QI2
$\overline{QI1}$
QI3
$\overline{QI2}$
QI1
DNUP
PS
$\overline{QI0}$
D
Q
QI0
CD
FD21
CLK
CD
$\overline{QI3}$
$\overline{QI2}$
QI1
QI0
Q0
QI1
Q1
QI2
Q2
QI3
Q3
$\overline{QI3}$
QI2
$\overline{QI1}$
QI3
QI2
QI1
QI3
$\overline{QI2}$
$\overline{QI1}$
CS

CGUD4.2


$\overline{QI[0:3]}$
QI1
QI[0:3]
HOLD1
EN
D1
LD
LOAD1
PS
QI1
$\overline{QI0}$
$\overline{QI3}$
QI2
QI0
QI3
QI2
QI0
DNUP
$\overline{QI3}$
QI2
QI0
QI3
QI2
QI0
CS
D
Q
CD
FD21
CLK
CD
$\overline{QI1}$
QI1

CGUD4.3


$\overline{\text{QI[0:3]}}$
QI2
QI[0:3]
HOLD2
EN
D2
LD
LOAD2
$\overline{\text{QI3}}$
QI1
$\overline{\text{QI0}}$
QI3
QI1
$\overline{\text{QI0}}$
DNUP
QI2
$\overline{\text{QI1}}$
QI2
QI0
D
Q
CD
FD21
CLK
CD
$\overline{\text{QI2}}$
QI2
QI3
HOLD3
D3
LD
LOAD3
QI2
$\overline{\text{QI1}}$
$\overline{\text{QI0}}$
$\overline{\text{QI2}}$
$\overline{\text{QI1}}$
$\overline{\text{QI0}}$
D
Q
CD
FD21
$\overline{\text{QI3}}$
QI3
QI3
QI0
QI3
QI1
CS
PS

I/O Pins

This chapter contains information on the following macros:

- Bidirectional Pins
- Input Pins
- Output Pins

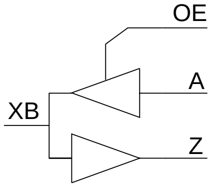
Bidirectional Pins

BI11, BI14, and BI18

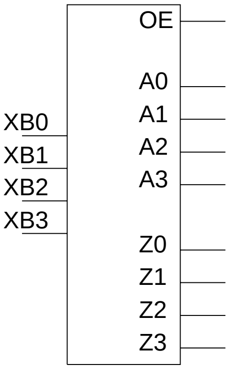
Function:

BI11:	1-bit bidirectional pin.
BI14:	Four BI11s with common Output Enable.
BI18:	Eight BI11s with common Output Enable.

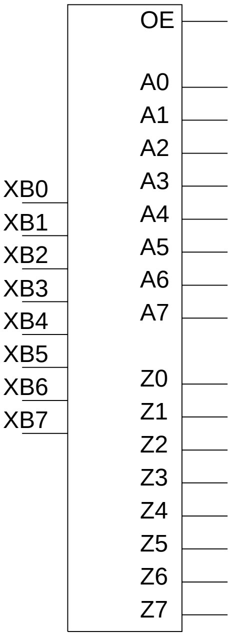
BI11



BI14



BI18



Availability:

BI11, BI14, and BI18 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Hard

Macro Port Definition:

```
BI11 (Z0,XB0,A0,OE);
BI14 ([Z0..Z3],[XB0..XB3],[A0..A3],OE);
BI18 ([Z0..Z7],[XB0..XB7],[A0..A7],OE);
```

Truth Table:

Do not drive XB0~XB_{n-1} when OE=1.

Input			Output	
OE	**A0~A_{n-1}**	**XB0~XB_{n-1}**	**XB0~XB_{n-1}**	**Z0~Z_{n-1}**
0	x	d	-	d
0	x	Z	-	X
1	d	Z	d	d

d = any pattern of 1s and 0s on an input or set of inputs, x = don't care,
X = X (unknown) state, Z = high impedance state,
- = appears in output column if a bidirectional pin acts as an input pin.

BI21, BI24, and BI28

Function:

BI21: 1-bit bidirectional pin with inverted output.
BI24: Four BI21s with common Output Enable.
BI28: Eight BI21s with common Output Enable.

Availability:

BI21, BI24, and BI28 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Hard

Macro Port Definition:

```
BI21 (Z0,XB0,A0,OE);
BI24 ([Z0..Z3],[XB0..XB3],[A0..A3],OE);
BI28 ([Z0..Z7],[XB0..XB7],[A0..A7],OE);
```

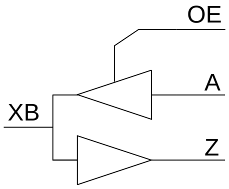
Truth Table:

Do not drive XB0~XB$_{n-1}$ when OE=1.

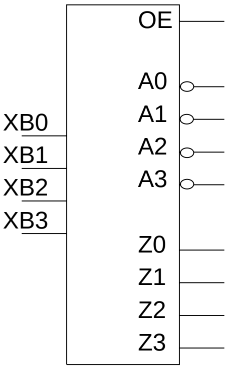
Input			Output	
OE	**A0~A$_{n-1}$**	**XB0~XB$_{n-1}$**	**XB0~XB$_{n-1}$**	**Z0~Z$_{n-1}$**
0	x	d	-	d
0	x	Z	-	X
1	d	Z	$\overline{d}$	$\overline{d}$

d = any pattern of 1s and 0s on an input or set of inputs,
$\overline{d}$ = inverse of d, x = don't care, X = X (unknown) state,
Z = high impedance state, - = appears in output column if a bidirectional pin acts as an input pin.

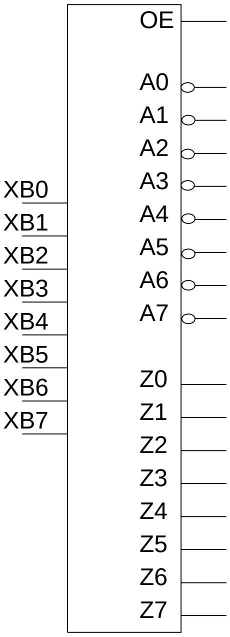
BI21



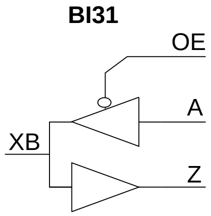
BI24



BI28



BI31, BI34, and BI38



Function:

BI31: 1-bit bidirectional pin with active low Output Enable.
BI34: Four BI31s with common Output Enable.
BI38: Eight BI31s with common Output Enable.

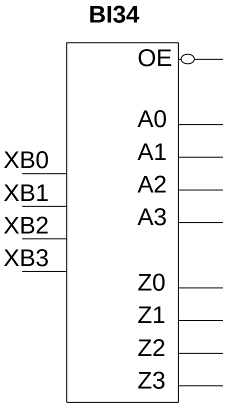
Availability:

BI31, BI34, and BI38 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Hard

Macro Port Definition:

```
BI31 (Z0,XB0,A0,OE);
BI34 ([Z0..Z3],[XB0..XB3],[A0..A3],OE);
BI38 ([Z0..Z7],[XB0..XB7],[A0..A7],OE);
```

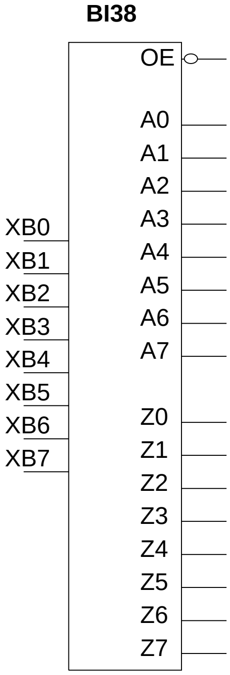


Truth Table:

Do not drive XB0~XB$_{n-1}$ when OE=0.

Input			Output	
OE	**A0~A$_{n-1}$**	**XB0~XB$_{n-1}$**	**XB0~XB$_{n-1}$**	**Z0~Z$_{n-1}$**
0	d	Z	d	d
1	x	d	-	d
1	x	Z	-	X

d = any pattern of 1s and 0s on an input or set of inputs,
x = don’t care, X = X (unknown) state, Z = high impedance state,
- = appears in output column if a bidirectional pin acts as an input pin.

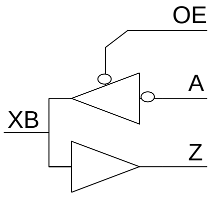


BI41, BI44, and BI48

Function:

BI41: 1-bit bidirectional pin with inverted output and active low Output Enable.
BI44: Four BI41s with common Output Enable.
BI48: Eight BI41s with common Output Enable.

BI41

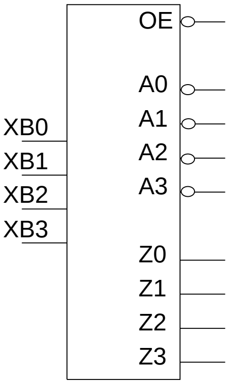


Availability:

BI41, BI44, and BI48 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Hard

BI44



Macro Port Definition:

```
BI41 (Z0,XB0,A0,OE);
BI44 ([Z0..Z3],[XB0..XB3],[A0..A3],OE);
BI48 ([Z0..Z7],[XB0..XB7],[A0..A7],OE);
```

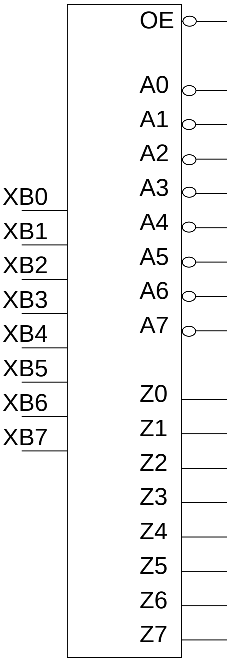
Truth Table:

Do not drive XB0~XB_{n-1} when OE=0.

Input			Output	
OE	**A0~A_{n-1}**	**XB0~XB_{n-1}**	**XB0~XB_{n-1}**	**Z0~Z_{n-1}**
0	d	Z	$\overline{d}$	$\overline{d}$
1	x	d	-	d
1	x	Z	-	X

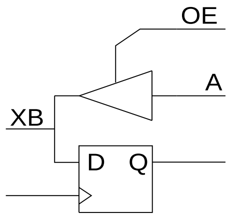
d = any pattern of 1s and 0s on an input or set of inputs,
$\overline{d}$ = inverse of d, x = don't care, X = X (unknown) state,
Z = high impedance state, - = appears in output column if a bidirectional pin acts as an input pin.

BI48

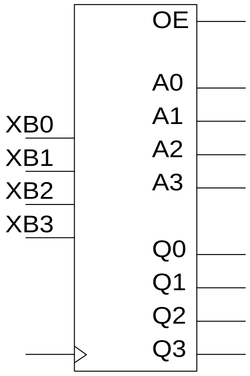


BIID11, BIID14, and BIID18

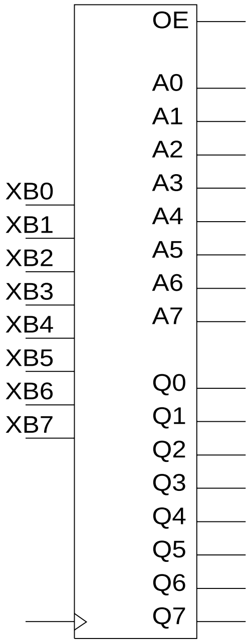
BIID11



BIID14



BIID18



Function:

BIID11:	1-bit bidirectional pin with registered input.
BIID14:	Four BIID11s with common clock and Output Enable.
BIID18:	Eight BIID11s with common clock and Output Enable.

Availability:

BIID11, BIID14, and BIID18 can be used with 1000, 2000, 3000, and 8000 devices.

Type: Hard

Macro Port Definition:

```
BIID11 (Q0,XB0,A0,CLK,OE);
BIID14 ([Q0..Q3],[XB0..XB3],[A0..A3],CLK,OE);
BIID18 ([Q0..Q7],[XB0..XB7],[A0..A7],CLK,OE);
```

Truth Table:

Do not drive XB0~XB$_{n-1}$ when OE=1.

Input				Output	
OE	**A0~A$_{n-1}$**	**XB0~XB$_{n-1}$**	**CLK**	**XB0~XB$_{n-1}$**	**Q0~Q$_{n-1}$**
0	x	d	↑	-	d
0	x	Z	↑	-	X
1	d	Z	↑	d	d
0	x	x	0	-	Q’
0	x	x	1	-	Q’
1	d	Z	0	d	Q’
1	d	Z	1	d	Q’

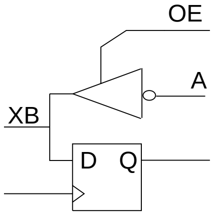
d = any pattern of 1s and 0s on an input or set of inputs,
Q’ = previous output of flip-flop or latch, x = don’t care,
X = X (unknown) state, Z = high impedance state,
- = appears in output column if a bidirectional pin acts as an input pin,
↑ = rising clock edge.

BIID21, BIID24, and BIID28

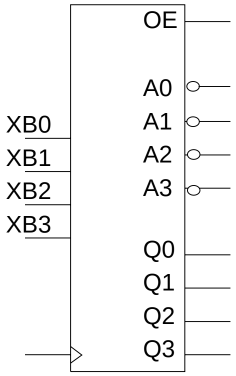
Function:

BIID21: 1-bit bidirectional pin with registered input and inverted output.
BIID24: Four BIID21s with common clock and Output Enable.
BIID28: Eight BIID21s with common clock and Output Enable.

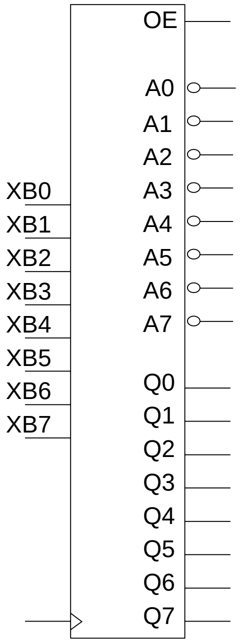
BIID21



BIID24



BIID28



Availability:

BIID21, BIID24, and BIID28 can be used with 1000, 2000, 3000, and 8000 devices.

Type: Hard

Macro Port Definition:

```
BIID21 (Q0,XB0,A0,CLK,OE);
BIID24 ([Q0..Q3],[XB0..XB3],[A0..A3],CLK,OE);
BIID28 ([Q0..Q7],[XB0..XB7],[A0..A7],CLK,OE);
```

Truth Table:

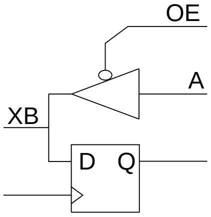
Do not drive XB0~XB$_{n-1}$ when OE=1.

Input				Output	
OE	**A0~A$_{n-1}$**	**XB0~XB$_{n-1}$**	**CLK**	**XB0~XB$_{n-1}$**	**Q0~Q$_{n-1}$**
0	x	d	↑	-	d
0	x	Z	↑	-	X
1	d	Z	↑	$\overline{d}$	$\overline{d}$
0	x	x	0	-	Q’
0	x	x	1	-	Q’
1	d	Z	0	$\overline{d}$	Q’
1	d	Z	1	$\overline{d}$	Q’

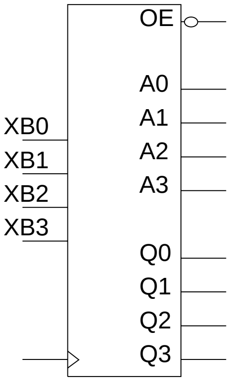
d = any pattern of 1s and 0s on an input or set of inputs, $\overline{d}$ = inverse of d,
Q’ = previous output of flip-flop or latch, x = don’t care,
X = X (unknown) state, Z = high impedance state,
- = appears in output column if a bidirectional pin acts as an input pin,
↑ = rising clock edge.

BIID31, BIID34, and BIID38

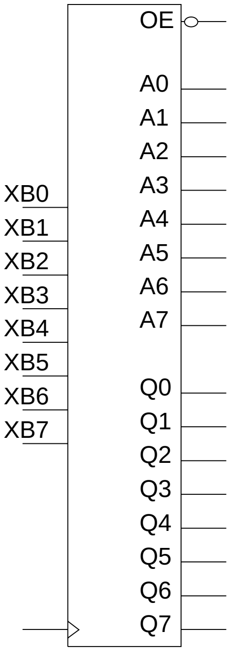
BIID31



BIID34



BIID38



Function:

BIID31:	1-bit bidirectional pin with registered input and active low enable.
BIID34:	Four BIID31s with common clock and Output Enable.
BIID38:	Eight BIID31s with common clock and Output Enable.

Availability:

BIID31, BIID34, and BIID38 can be used with 1000, 2000, 3000, and 8000 devices.

Type: Hard

Macro Port Definition:

```
BIID31 (Q0,XB0,A0,CLK,OE);
BIID34 ([Q0..Q3],[XB0..XB3],[A0..A3],CLK,OE);
BIID38 ([Q0..Q7],[XB0..XB7],[A0..A7],CLK,OE);
```

Truth Table:

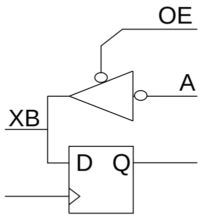
Do not drive XB0~XB$_{n-1}$ when OE=1.

Input				Output	
OE	**A0~A$_{n-1}$**	**XB0~XB$_{n-1}$**	**CLK**	**XB0~XB$_{n-1}$**	**Q0~Q$_{n-1}$**
0	d	Z	↑	d	d
1	x	d	↑	-	d
1	x	Z	↑	-	X
0	d	Z	0	d	Q’
0	d	Z	1	d	Q’
1	x	x	0	-	Q’
1	x	x	1	-	Q’

d = any pattern of 1s and 0s on an input or set of inputs,
Q’ = previous output of flip-flop or latch, x = don’t care,
X = X (unknown) state, Z = high impedance state,
- = appears in output column if a bidirectional pin acts as an input pin,
↑ = rising clock edge.

BIID41, BIID44, and BIID48

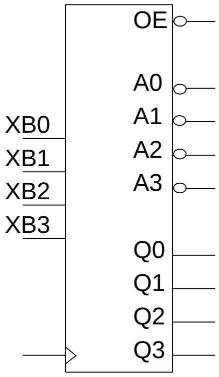
BIID41



Function:

BIID41: 1-bit bidirectional pin with registered input, inverted output, and active low enable.
BIID44: Four BIID41s with common clock and Output Enable.
BIID48: Eight BIID41s with common clock and Output Enable.

BIID44



Availability:

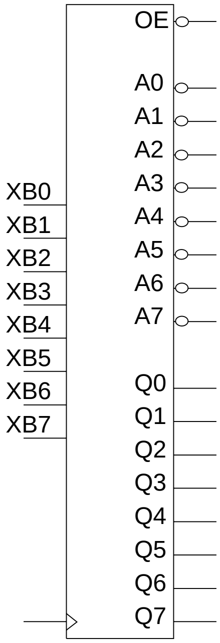
BIID41, BIID44, and BIID48 can be used with 1000, 2000, 3000, and 8000 devices.

Type: Hard

Macro Port Definition:

```
BIID41 (Q0,XB0,A0,CLK,OE);
BIID44 ([Q0..Q3],[XB0..XB3],[A0..A3],CLK,OE);
BIID48 ([Q0..Q7],[XB0..XB7],[A0..A7],CLK,OE);
```

BIID48



Truth Table:

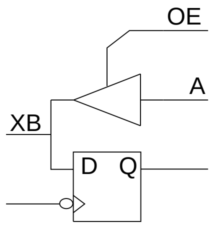
Do not drive XB0~XB$_{n-1}$ when OE=1.

Input				Output	
OE	**A0~A$_{n-1}$**	**XB0~XB$_{n-1}$**	**CLK**	**XB0~XB$_{n-1}$**	**Q0~Q$_{n-1}$**
0	d	Z	↑	$\overline{d}$	$\overline{d}$
1	x	d	↑	-	d
1	x	Z	↑	-	X
0	d	Z	0	$\overline{d}$	Q’
0	d	Z	1	$\overline{d}$	Q’
1	x	x	0	-	Q’
1	x	x	1	-	Q’

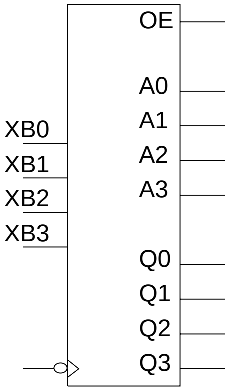
d = any pattern of 1s and 0s on an input or set of inputs, $\overline{d}$ = inverse of d,
Q’ = previous output of flip-flop or latch, x = don’t care, X = X (unknown) state,
Z = high impedance state, ↑ = rising clock edge,
- = appears in output column if a bidirectional pin acts as an input pin.

BIID51, BIID54, and BIID58

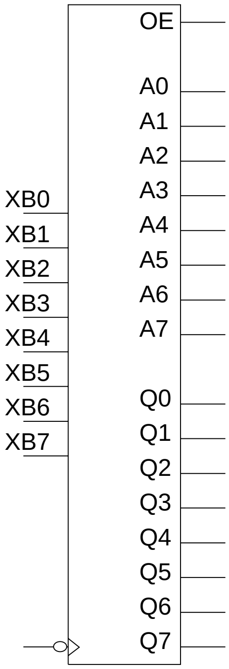
BIID51



BIID54



BIID58



Function:

BIID51:	1-bit bidirectional pin with registered input and inverted clock.
BIID54:	Four BIID51s with common clock and Output Enable.
BIID58:	Eight BIID51s with common clock and Output Enable.

Availability:

BIID51, BIID54, and BIID58 can be used with 1000, 2000, 3000, and 8000 devices.

Type: Hard

Macro Port Definition:

```
BIID51 (Q0,XB0,A0,CLK,OE);
BIID54 ([Q0..Q3],[XB0..XB3],[A0..A3],CLK,OE);
BIID58 ([Q0..Q7],[XB0..XB7],[A0..A7],CLK,OE);
```

Truth Table:

Do not drive XB0~XB$_{n-1}$ when OE=1.

Input				Output	
OE	**A0~A$_{n-1}$**	**XB0~XB$_{n-1}$**	**CLK**	**XB0~XB$_{n-1}$**	**Q0~Q$_{n-1}$**
0	x	d	↓	-	d
0	x	Z	↓	-	X
1	d	Z	↓	d	d
0	x	x	0	-	Q’
0	x	x	1	-	Q’
1	d	Z	0	d	Q’
1	d	Z	1	d	Q’

d = any pattern of 1s and 0s on an input or set of inputs,
Q’ = previous output of flip-flop or latch, x = don’t care,
X = X (unknown) state, Z = high impedance state,
- = appears in output column if a bidirectional pin acts as an input pin,
↓ = falling clock edge.

BIID61, BIID64, and BIID68

Function:

BIID61: 1-bit bidirectional pin with registered input, inverted output, and inverted clock.
BIID64: Four BIID61s with common clock and Output Enable.
BIID68: Eight BIID61s with common clock and Output Enable.

Availability:

BIID61, BIID64, and BIID68 can be used with 1000, 2000, 3000, and 8000 devices.

Type: Hard

Macro Port Definition:

```
BIID61 (Q0,XB0,A0,CLK,OE);
BIID64 ([Q0..Q3],[XB0..XB3],[A0..A3],CLK,OE);
BIID68 ([Q0..Q7],[XB0..XB7],[A0..A7],CLK,OE);
```

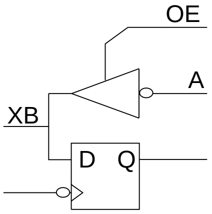
Truth Table:

Do not drive XB0~XB$_{n-1}$ when OE=1.

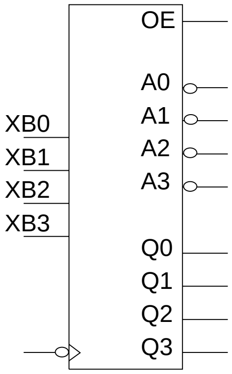
Input				Output	
OE	**A0~A$_{n-1}$**	**XB0~XB$_{n-1}$**	**CLK**	**XB0~XB$_{n-1}$**	**Q0~Q$_{n-1}$**
0	x	d	↓	-	d
0	x	Z	↓	-	X
1	d	Z	↓	$\overline{d}$	$\overline{d}$
0	x	x	0	-	Q’
0	x	x	1	-	Q’
1	d	Z	0	$\overline{d}$	Q’
1	d	Z	1	$\overline{d}$	Q’

d = any pattern of 1s and 0s on an input or set of inputs, $\overline{d}$ = inverse of d,
Q’ = previous output of flip-flop or latch,
x = don’t care, X = X (unknown) state, Z = high impedance state,
- = appears in output column if a bidirectional pin acts as an input pin,
↓ = falling clock edge.

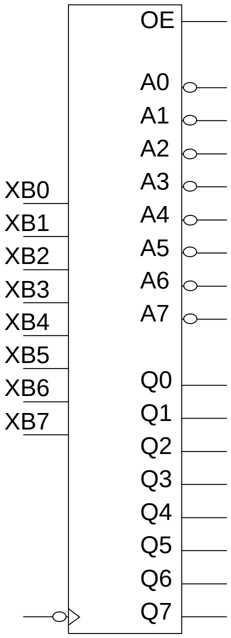
BIID61



BIID64

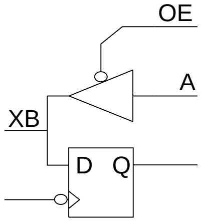


BIID68

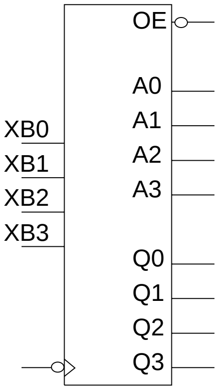


BIID71, BIID74, and BIID78

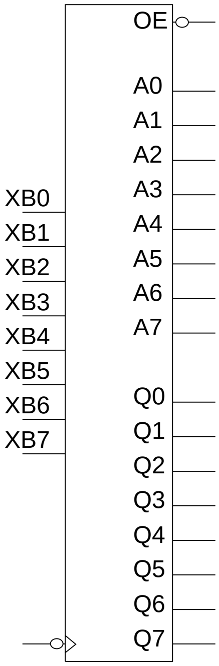
BIID71



BIID74



BIID78



Function:

BIID71:	1-bit bidirectional pin with registered input, active low enable, and inverted clock.
BIID74:	Four BIID71s with common clock and Output Enable.
BIID78:	Eight BIID71s with common clock and Output Enable.

Availability:

BIID71, BIID74, and BIID78 can be used with 1000, 2000, 3000, and 8000 devices.

Type: Hard

Macro Port Definition:

```
BIID71 (Q0,XB0,A0,CLK,OE);
BIID74 ([Q0..Q3],[XB0..XB3],[A0..A3],CLK,OE);
BIID78 ([Q0..Q7],[XB0..XB7],[A0..A7],CLK,OE);
```

Truth Table:

Do not drive XB0~XB$_{n-1}$ when OE=1.

Input				Output	
OE	**A0~A$_{n-1}$**	**XB0~XB$_{n-1}$**	**CLK**	**XB0~XB$_{n-1}$**	**Q0~Q$_{n-1}$**
0	d	Z	↓	d	d
1	x	d	↓	-	d
1	x	Z	↓	-	X
0	d	Z	0	d	Q’
0	d	Z	1	d	Q’
1	x	x	0	-	Q’
1	x	x	1	-	Q’

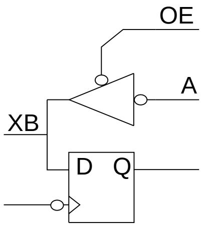
d = any pattern of 1s and 0s on an input or set of inputs,
Q’ = previous output of flip-flop or latch,
x = don’t care, X = X (unknown) state, Z = high impedance state,
- = appears in output column if a bidirectional pin acts as an input pin,
↓ = falling clock edge.

BIID81, BIID84, and BIID88

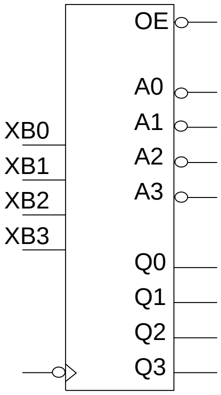
Function:

BIID81: 1-bit bidirectional pin with registered input, inverted output, active low enable, and inverted clock.
BIID84: Four BIID81s with common clock and Output Enable.
BIID88: Eight BIID81s with common clock and Output Enable.

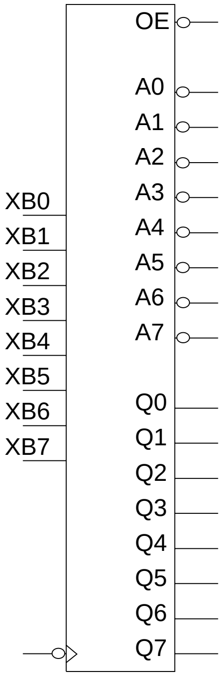
BIID81



BIID84



BIID88



Availability:

BIID81, BIID84, and BIID88 can be used with 1000, 2000, 3000, and 8000 devices.

Type: Hard

Macro Port Definition:

```
BIID81 (Q0,XB0,A0,CLK,OE);
BIID84 ([Q0..Q3],[XB0..XB3],[A0..A3],CLK,OE);
BIID88 ([Q0..Q7],[XB0..XB7],[A0..A7],CLK,OE);
```

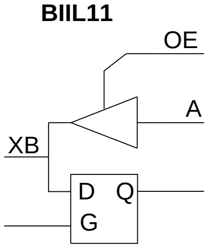
Truth Table:

Do not drive XB0~XB$_{n-1}$ when OE=1.

Input				Output	
OE	**A0~A$_{n-1}$**	**XB0~XB$_{n-1}$**	**CLK**	**XB0~XB$_{n-1}$**	**Q0~Q$_{n-1}$**
0	d	Z	↓	$\overline{d}$	$\overline{d}$
1	x	d	↓	-	d
1	x	Z	↓	-	X
0	d	Z	0	$\overline{d}$	Q’
0	d	Z	1	$\overline{d}$	Q’
1	x	x	0	-	Q’
1	x	x	1	-	Q’

d = any pattern of 1s and 0s on an input or set of inputs, $\overline{d}$ = inverse of d,
Q’ = previous output of flip-flop or latch, x = don’t care,
X = X (unknown) state, Z = high impedance state, ↓ = falling clock edge,
- = appears in output column if a bidirectional pin acts as an input pin.

BIIL11, BIIL14, and BIIL18

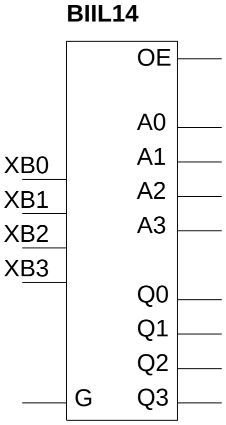


Function:

BIIL11:	1-bit bidirectional pin with latched input.
BIIL14:	Four BIIL11s with common G and Output Enable.
BIIL18:	Eight BIIL11s with common G and Output Enable.

Availability:

BIIL11, BIIL14, and BIIL18 can be used with 1000, 2000, 3000, and 8000 devices.



Type: Hard

Macro Port Definition:

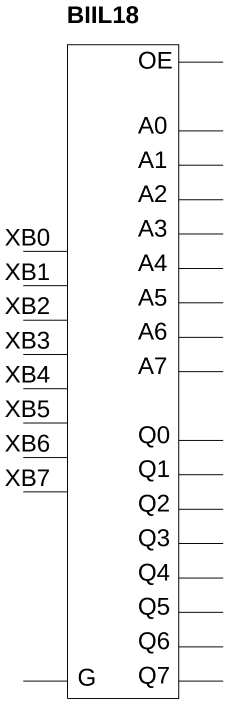
```
BIIL11 (Q0,XB0,A0,G,OE);
BIIL14 ([Q0..Q3],[XB0..XB3],[A0..A3],G,OE);
BIIL18 ([Q0..Q7],[XB0..XB7],[A0..A7],G,OE);
```

Truth Table:

Do not drive XB0~XB$_{n-1}$ when OE=1.

Input				Output	
OE	**A0~A$_{n-1}$**	**XB0~XB$_{n-1}$**	**G**	**XB0~XB$_{n-1}$**	**Q0~Q$_{n-1}$**
0	x	x	0	-	Q’
1	d	Z	0	d	Q’
0	x	d	1	-	d
0	x	Z	1	-	X
1	d	Z	1	d	d

d = any pattern of 1s and 0s on an input or set of inputs,
Q’ = previous output of flip-flop or latch, x = don’t care,
X = X (unknown) state, Z = high impedance state,
- = appears in output column if a bidirectional pin acts as an input pin.

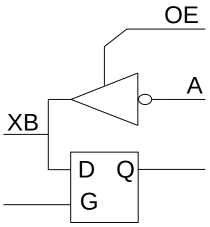


BIIL21, BIIL24, and BIIL28

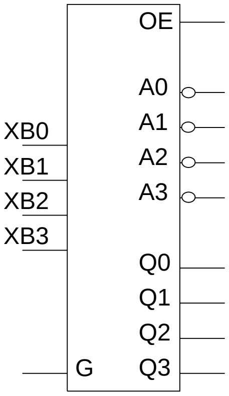
Function:

BIIL21:	1-bit bidirectional pin with latched input and inverted output.
BIIL24:	Four BIIL21s with common G and Output Enable.
BIIL28:	Eight BIIL21s with common G and Output Enable.

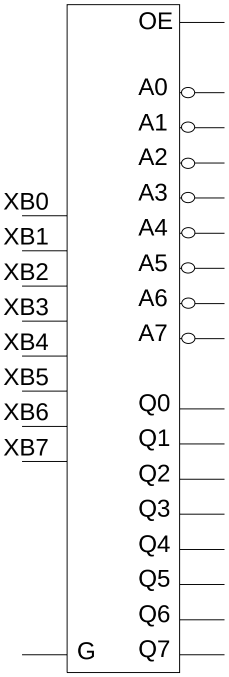
BIIL21



BIIL24



BIIL28



Availability:

BIIL21, BIIL24, and BIIL28 can be used with 1000, 2000, 3000, and 8000 devices.

Type: Hard

Macro Port Definition:

```
BIIL21 (Q0,XB0,A0,G,OE);
BIIL24 ([Q0..Q3],[XB0..XB3],[A0..A3],G,OE);
BIIL28 ([Q0..Q7],[XB0..XB7],[A0..A7],G,OE);
```

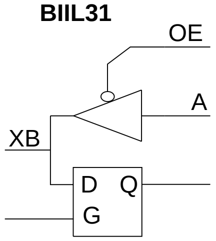
Truth Table:

Do not drive XB0~XB$_{n-1}$ when OE=1.

Input				**Output**	
OE	**A0~A$_{n-1}$**	**XB0~XB$_{n-1}$**	**G**	**XB0~XB$_{n-1}$**	**Q0~Q$_{n-1}$**
0	x	x	0	-	Q’
1	d	Z	0	$\overline{d}$	Q’
0	x	d	1	-	d
0	x	Z	1	-	X
1	d	Z	1	$\overline{d}$	$\overline{d}$

d = any pattern of 1s and 0s on an input or set of inputs, $\overline{d}$ = inverse of d,
Q’ = previous output of flip-flop or latch, x = don’t care,
X = X (unknown) state, Z = high impedance state,
- = appears in output column if a bidirectional pin acts as an input pin.

BIIL31, BIIL34, and BIIL38



Function:

BIIL31:	1-bit bidirectional pin with latched input and active low enable.
BIIL34:	Four BIIL31s with common G and Output Enable.
BIIL38:	Eight BIIL31s with common G and Output Enable.

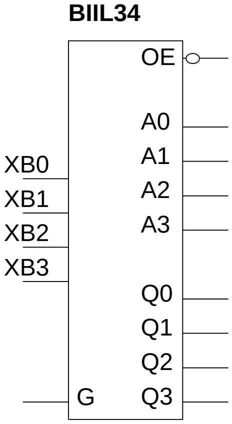
Availability:

BIIL31, BIIL34, and BIIL38 can be used with 1000, 2000, 3000, and 8000 devices.

Type: Hard

Macro Port Definition:

```
BIIL31 (Q0,XB0,A0,G,OE);
BIIL34 ([Q0..Q3],[XB0..XB3],[A0..A3],G,OE);
BIIL38 ([Q0..Q7],[XB0..XB7],[A0..A7],G,OE);
```

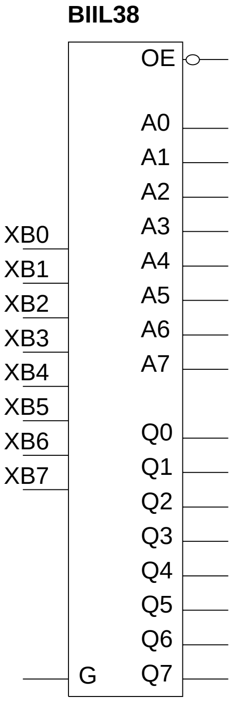


Truth Table:

Do not drive XB0~XB$_{n-1}$ when OE=0.

Input				Output	
OE	**A0~A$_{n-1}$**	**XB0~XB$_{n-1}$**	**G**	**XB0~XB$_{n-1}$**	**Q0~Q$_{n-1}$**
0	d	Z	0	d	Q’
1	x	x	0	-	Q’
0	d	Z	1	d	d
1	x	d	1	-	d
1	x	Z	1	-	X

d = any pattern of 1s and 0s on an input or set of inputs,
Q’ = previous output of flip-flop or latch, x = don’t care,
X = X (unknown) state, Z = high impedance state,
- = appears in output column if a bidirectional pin acts as an input pin.

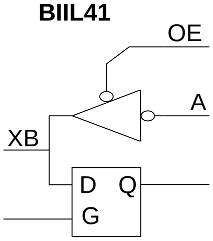


BIIL41, BIIL44, and BIIL48

Function:

BIIL41:	1-bit bidirectional pin with latched input, inverted output, and active low enable.
BIIL44:	Four BIIL41s with common G and Output Enable.
BIIL48:	Eight BIIL41s with common G and Output Enable.

BIIL41

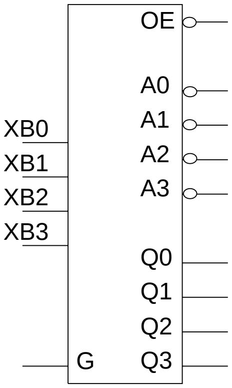


Availability:

BIIL41, BIIL44, and BIIL48 can be used with 1000, 2000, 3000, and 8000 devices.

Type: Hard

BIIL44



Macro Port Definition:

```
BIIL41 (Q0,XB0,A0,G,OE);
BIIL44 ([Q0..Q3],[XB0..XB3],[A0..A3],G,OE);
BIIL48 ([Q0..Q7],[XB0..XB7],[A0..A7],G,OE);
```

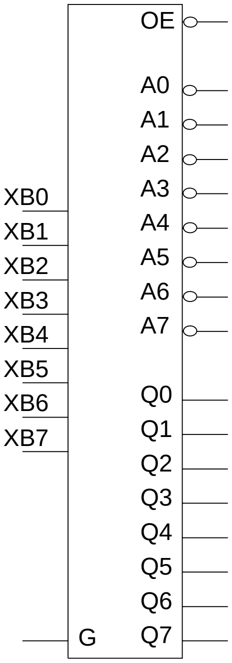
Truth Table:

Do not drive XB0~XB$_{n-1}$ when OE=0.

Input				Output	
OE	**A0~A$_{n-1}$**	**XB0~XB$_{n-1}$**	**G**	**XB0~XB$_{n-1}$**	**Q0~Q$_{n-1}$**
0	d	Z	0	$\overline{d}$	Q’
1	x	x	0	-	Q’
0	d	Z	1	$\overline{d}$	d
1	x	d	1	-	d
1	x	Z	1	-	X

d = any pattern of 1s and 0s on an input or set of inputs, $\overline{d}$ = inverse of d,
Q’ = previous output of flip-flop or latch, x = don’t care,
X = X (unknown) state, Z = high impedance state,
- = appears in output column if a bidirectional pin acts as an input pin.

BIIL48

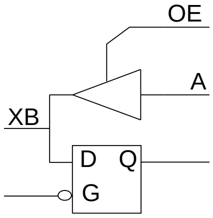


BIIL51, BIIL54, and BIIL58

Function:

BIIL51:	1-bit bidirectional pin with latched input and inverted G.
BIIL54:	Four BIIL51s with common G and Output Enable.
BIIL58:	Eight BIIL51s with common G and Output Enable.

BIIL51

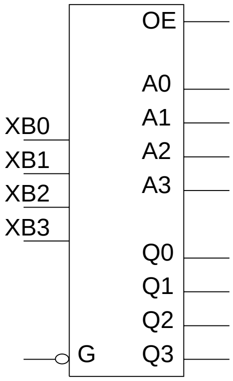


Availability:

BIIL51, BIIL54, and BIIL58 can be used with 1000, 2000, 3000, and 8000 devices.

Type: Hard

BIIL54



Macro Port Definition:

```
BIIL51 (Q0,XB0,A0,G,OE);
BIIL54 ([Q0..Q3],[XB0..XB3],[A0..A3],G,OE);
BIIL58 ([Q0..Q7],[XB0..XB7],[A0..A7],G,OE);
```

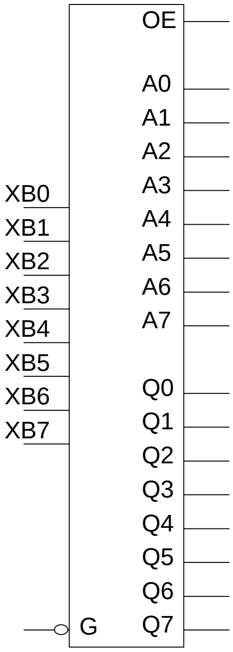
Truth Table:

Do not drive XB0~XB_{n-1} when OE=1.

Input				Output	
OE	**A0~A_{n-1}**	**XB0~XB_{n-1}**	**G**	**XB0~XB_{n-1}**	**Q0~Q_{n-1}**
0	x	d	0	-	d
0	x	Z	0	-	X
1	d	Z	0	d	d
0	x	x	1	-	Q’
1	d	Z	1	d	Q’

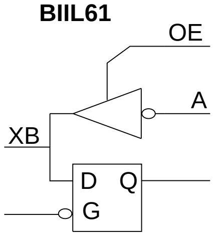
d = any pattern of 1s and 0s on an input or set of inputs,
Q’ = previous output of flip-flop or latch, x = don’t care,
X = unknown state, Z = high impedance state,
- = appears in output column if a bidirectional pin acts as an input pin.

BIIL58



BIIL61, BIIL64, and BIIL68

BIIL61



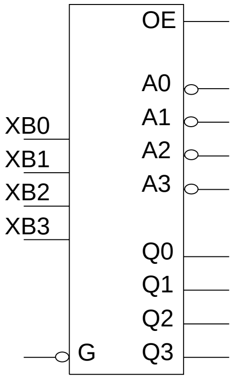
Function:

BIIL61: 1-bit bidirectional pin with latched input, inverted output, and inverted G.
BIIL64: Four BIIL61s with common G and Output Enable.
BIIL68: Eight BIIL61s with common G and Output Enable.

Availability:

BIIL61, BIIL64, and BIIL68 can be used with 1000, 2000, 3000, and 8000 devices.

BIIL64



Type: Hard

Macro Port Definition:

```
BIIL61 (Q0,XB0,A0,G,OE);
BIIL64 ([Q0..Q3],[XB0..XB3],[A0..A3],G,OE);
BIIL68 ([Q0..Q7],[XB0..XB7],[A0..A7],G,OE);
```

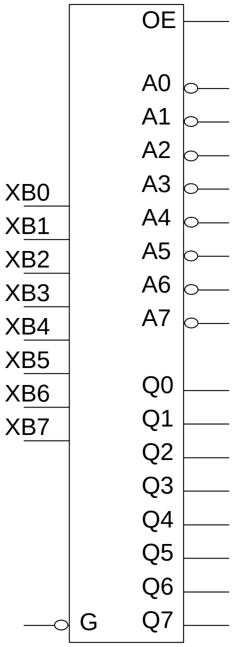
Truth Table:

Do not drive XB0~XB$_{n-1}$ when OE=1.

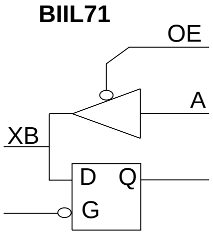
Input				Output	
OE	**A0~A$_{n-1}$**	**XB0~XB$_{n-1}$**	**G**	**XB0~XB$_{n-1}$**	**Q0~Q$_{n-1}$**
0	x	d	0	-	d
0	x	Z	0	-	X
1	d	Z	0	$\overline{d}$	$\overline{d}$
0	x	x	1	-	Q’
1	d	Z	1	$\overline{d}$	Q’

d = any pattern of 1s and 0s on an input or set of inputs, $\overline{d}$ = inverse of d,
Q’ = previous output of flip-flop or latch, x = don’t care,
X = unknown state, Z = high impedance state,
- = appears in output column if a bidirectional pin acts as an input pin.

BIIL68



BIIL71, BIIL74, and BIIL78

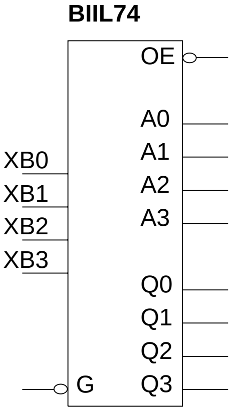


Function:

BIIL71: 1-bit bidirectional pin with latched input, active low enable, and inverted G.
BIIL74: Four BIIL71s with common G and Output Enable.
BIIL78: Eight BIIL71s with common G and Output Enable.

Availability:

BIIL71, BIIL74, and BIIL78 can be used with 1000, 2000, 3000, and 8000 devices.



Type: Hard

Macro Port Definition:

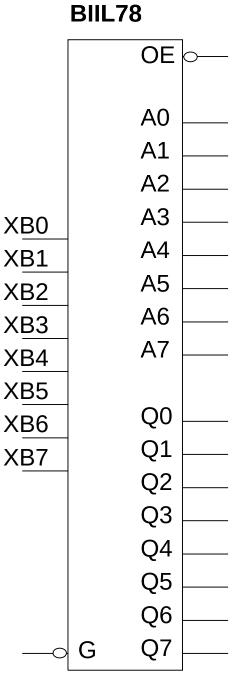
```
BIIL71 (Q0,XB0,A0,G,OE);
BIIL74 ([Q0..Q3],[XB0..XB3],[A0..A3],G,OE);
BIIL78 ([Q0..Q7],[XB0..XB7],[A0..A7],G,OE);
```

Truth Table:

Do not drive XB0~XB$_{n-1}$ when OE=0.

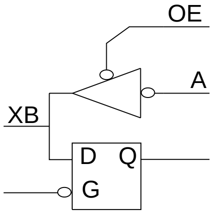
Input				Output	
OE	A0~A$_{n-1}$	XB0~XB$_{n-1}$	G	XB0~XB$_{n-1}$	Q0~Q$_{n-1}$
0	d	Z	0	d	d
1	x	d	0	-	d
1	x	Z	0	-	X
0	d	Z	1	d	Q’
1	x	x	1	-	Q’

d = any pattern of 1s and 0s on an input or set of inputs,
Q’ = previous output of flip-flop or latch, x = don’t care,
X = unknown state, Z = high impedance state,
- = appears in output column if a bidirectional pin acts as an input pin.



BIIL81, BIIL84, and BIIL88

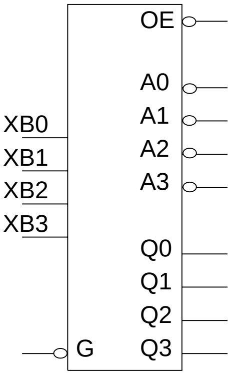
BIIL81



Function:

BIIL81:	1-bit bidirectional pin with latched input, inverted output, active low enable, and inverted G.
BIIL84:	Four BIIL81s with common G and Output Enable.
BIIL88:	Eight BIIL81s with common G and Output Enable.

BIIL84



Availability:

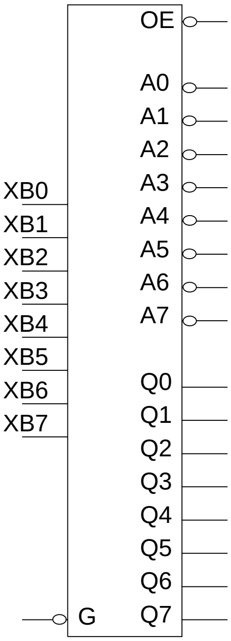
BIIL81, BIIL84, and BIIL88 can be used with 1000, 2000, 3000, and 8000 devices.

Type: Hard

Macro Port Definition:

```
BIIL81 (Q0,XB0,A0,G,OE);
BIIL84 ([Q0..Q3],[XB0..XB3],[A0..A3],G,OE);
BIIL88 ([Q0..Q7],[XB0..XB7],[A0..A7],G,OE);
```

BIIL88



Truth Table:

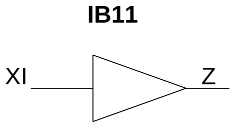
Do not drive XB0~XB$_{n-1}$ when OE=0.

Input				**Output**	
OE	**A0~A$_{n-1}$**	**XB0~XB$_{n-1}$**	**G**	**XB0~XB$_{n-1}$**	**Q0~Q$_{n-1}$**
0	d	Z	0	$\bar{d}$	$\bar{d}$
1	x	d	0	-	d
1	x	Z	0	-	X
0	d	Z	1	$\bar{d}$	Q’
1	x	x	1	-	Q’

d = any pattern of 1s and 0s on an input or set of inputs, $\bar{d}$ = inverse of d,
Q’ = previous output of flip-flop or latch, x = don’t care,
X = unknown state, Z = high impedance state,
- = appears in output column if a bidirectional pin acts as an input pin.

Input Pins

IB11



Function: 1-bit input pin.

Availability:

IB11 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Hard

Macro Port Definition:

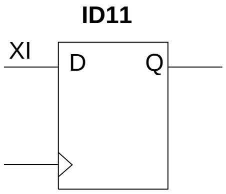
```
IB11(Z0,XI0);
```

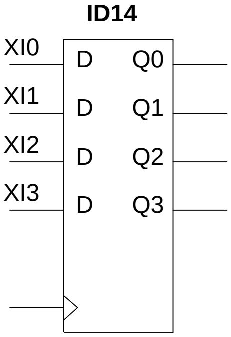
Truth Table:

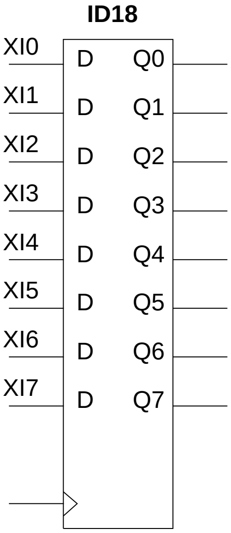
Input	**Output**
XI0	**Z0**
d	d

d = any pattern of 1s and 0s on an input or set of inputs,
XI0 = external input pin, Z0 = output.

ID11, ID14, and ID18







Function:

ID11: 1-bit registered input pin.
ID14: Four ID11s with common clock.
ID18: Eight ID11s with common clock.

Availability:

ID11, ID14, and ID18 can be used with 1000, 2000, 3000, and 8000 devices.

Type: Hard

Macro Port Definition:

```
ID11 (Q0,XI0,CLK);
ID14 ([Q0..Q3],[XI0..XI3],CLK);
ID18 ([Q0..Q7],[XI0..XI7],CLK);
```

Truth Table:

Input		Output
$XI0\sim XI_{n-1}$	**CLK**	**$Q0\sim Q_{n-1}$**
d	↑	d
x	0	Q0'~Qn'
x	1	Q0'~Qn'

d = any pattern of 1s and 0s on an input or set of inputs,
Q0'~Qn' = previous output of flip-flop or latch,
x = don't care, ↑ = rising clock edge.

ID21, ID24, and ID28

Function:

ID21: 1-bit registered input pin with inverted clock.
ID24: Four ID21s with common clock.
ID28: Eight ID21s with common clock.

Availability:

ID21, ID24, and ID28 can be used with1000, 2000, 3000, and 8000 devices.

Type: Hard

Macro Port Definition:

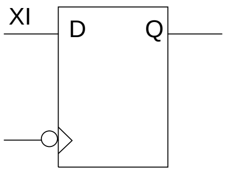
```
ID21 (Q0,XI0,CLK);
ID24 ([Q0..Q3],[XI0..XI3],CLK);
ID28 ([Q0..Q7],[XI0..XI7],CLK);
```

Truth Table:

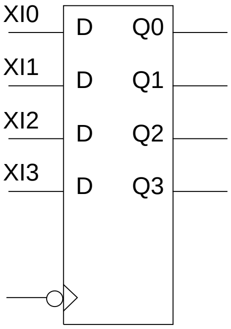
Input		**Output**
XI0~XI$_{n-1}$	**CLK**	**Q0~Q$_{n-1}$**
d	↓	d
x	0	Q0'~Qn'
x	1	Q0'~Qn'

d = any pattern of 1s and 0s on an input or set of inputs,
Q0'~Qn' = previous output of flip-flop or latch,
x = don't care, ↓ = falling clock edge.

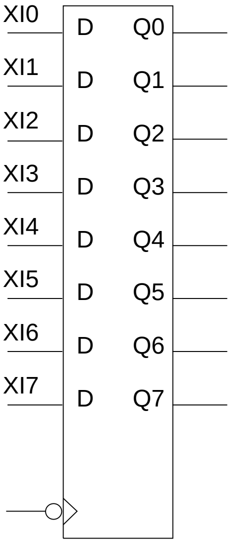
ID21



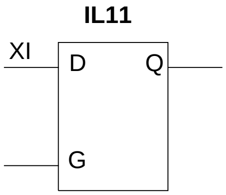
ID24

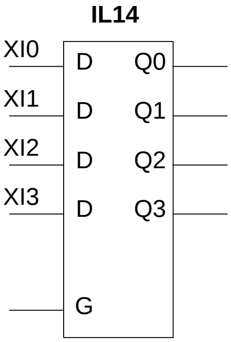


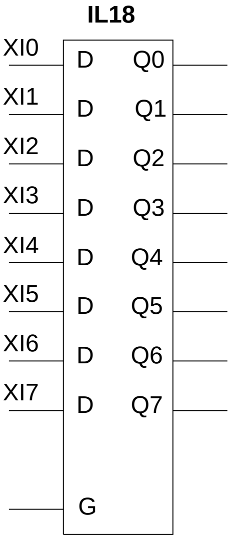
ID28



IL11, IL14, and IL18







Function:

IL11:	1-bit input pin with D latch on input.
IL14:	Four IL11s with common G.
IL18:	Eight IL11s with common G.

Availability:

IL11, IL14, and IL18 can be used with 1000, 2000, 3000, and 8000 devices.

Type: Hard

Macro Port Definition:

```
IL11 (Q0,XI0,G);
IL14 ([Q0..Q3],[XI0..XI3],G);
IL18 ([Q0..Q7],[XI0..XI7],G);
```

Truth Table:

Input		Output
XI0~XI$_{n-1}$	**G**	**Q0~Q$_{n-1}$**
x	0	Q0'~Qn'
d	1	d

d = any pattern of 1s and 0s on an input or set of inputs,
G = gate for latch, x = don't care,
Q0'~Qn' = previous output of flip-flop or latch.

IL21, IL24, and IL28

Function:

IL21: 1-bit input pin with D latch on input, inverted enable.
IL24: Four IL21s with common G.
IL28: Eight IL21s with common G.

Availability:

IL21, IL24, and IL28 can be used with 1000, 2000, 3000, and 8000 devices.

Type: Hard

Macro Port Definition:

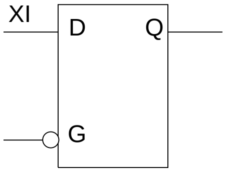
```
IL21 (Q0,XI0,G);
IL24 ([Q0..Q3],[XI0..XI3],G);
IL28 ([Q0..Q7],[XI0..XI7],G);
```

Truth Table:

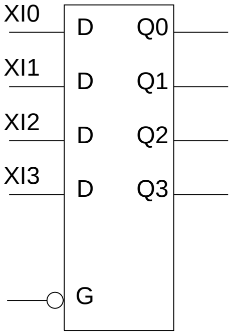
Input		**Output**
XI0~XI$_{n-1}$	**G**	**Q0~Q$_{n-1}$**
d	0	d
x	1	Q0’~Qn’

d = any pattern of 1s and 0s on an input or set of inputs,
Q0’~Qn’ = previous output of flip-flop or latch,
x = don’t care.

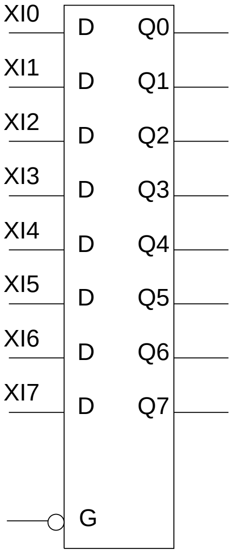
IL21



IL24

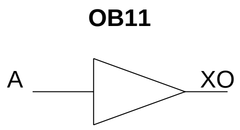


IL28



Output Pins

OB11



Function: 1-bit output pin.

Availability:

OB11 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Hard

Macro Port Definition:

```
OB11 (XO0,A0);
```

Truth Table:

Input	Output
A0	**XO0**
d	d

d = any pattern of 1s and 0s on an input or set of inputs

OB21, OB24, and OB28

Function:

OB21:	1-bit inverting output pin.
OB24:	Four OB21s.
OB28:	Eight OB21s.

Availability:

OB21, OB24, and OB28 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Hard

Macro Port Definition:

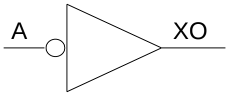
```
OB21 (XO0,A0);
OB24 ([XO0..XO3],[A0..A3]);
OB28 ([XO0..XO7],[A0..A7]);
```

Truth Table:

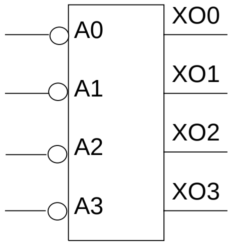
Input	Output
A0~A$_{n-1}$	**XO0~XO$_{n-1}$**
d	$\overline{d}$

d = any pattern of 1s and 0s on an input or set of inputs,
$\overline{d}$ = inverse of d.

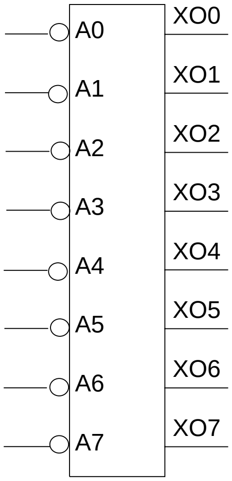
OB21



OB24



OB28

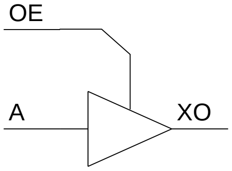


OT11, OT14, and OT18

Function:

OT11: 1-bit 3-state output pin.
OT14: Four OT11s with common Output Enable.
OT18: Eight OT11s with common Output Enable.

OT11

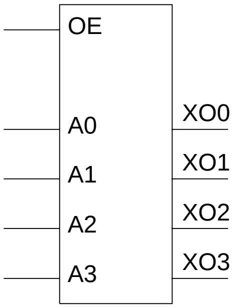


Availability:

OT11, OT14, and OT18 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Hard

OT14



Macro Port Definition:

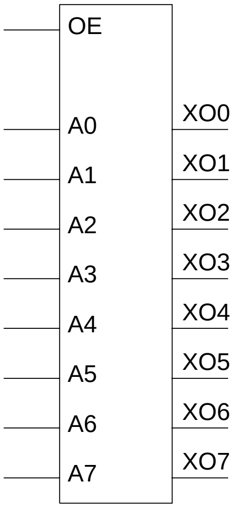
```
OT11 (XO0,A0,OE);
OT14 ([XO0..XO3],[A0..A3],OE);
OT18 ([XO0..XO7],[A0..A7],OE);
```

Truth Table:

Input		Output
OE	**A0~A_{n-1}**	**XO0~XO_{n-1}**
0	x	Z
1	d	d

d = any pattern of 1s and 0s on an input or set of inputs,
x = don’t care, Z = high impedance state.

OT18



OT21, OT24, and OT28

Function:

OT21:	1-bit inverting 3-state output pin.
OT24:	Four OT21s with common Output Enable.
OT28:	Eight OT21s with common Output Enable.

Availability:

OT21, OT24, and OT28 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Hard

Macro Port Definition:

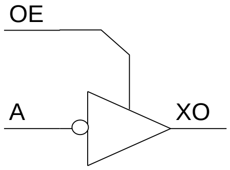
```
OT21 (XO0,A0,OE);
OT24 ([XO0..XO3],[A0..A3],OE);
OT28 ([XO0..XO7],[A0..A7],OE);
```

Truth Table:

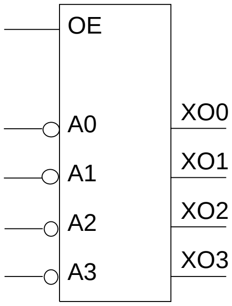
Input		Output
OE	**A0~A_{n-1}**	**XO0~XO_{n-1}**
0	x	Z
1	d	$\overline{d}$

d = any pattern of 1s and 0s on an input or set of inputs,
$\overline{d}$ = inverse of d, x = don’t care, Z = high impedance state.

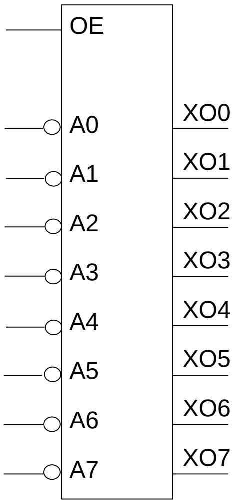
OT21



OT24



OT28



OT31, OT34, and OT38

Function:

OT31: 1-bit 3-state output pin with active low enable.
OT34: Four OT31s with common Output Enable.
OT38: Eight OT31s with common Output Enable.

Availability:

OT31, OT34, and OT38 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Hard

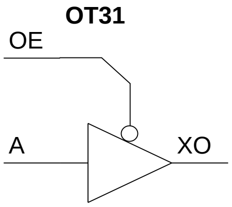
Macro Port Definition:

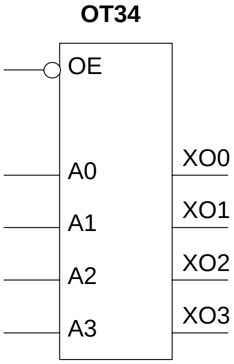
```
OT31 (XO0,A0,OE);
OT34 ([XO0..XO3],[A0..A3],OE);
OT38 ([XO0..XO7],[A0..A7],OE);
```

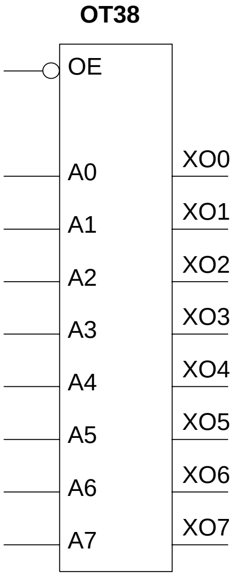
Truth Table:

Input		**Output**
OE	**A0~A$_{n-1}$**	**XO0~XO$_{n-1}$**
0	d	d
1	x	Z

d = any pattern of 1s and 0s on an input or set of inputs,
x = don’t care, Z = high impedance state.







OT41, OT44, and OT48

Function:

OT41:	1-bit inverting 3-state output pin with active low enable.
OT44:	Four OT41s with common Output Enable.
OT48:	Eight OT41s with common Output Enable.

Availability:

OT41, OT44, and OT48 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Hard

Macro Port Definition:

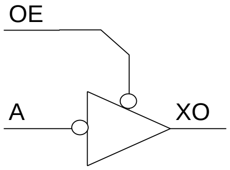
```
OT41 (XO0,A0,OE);
OT44 ([XO0..XO3],[A0..A3],OE);
OT48 ([XO0..XO7],[A0..A7],OE);
```

Truth Table:

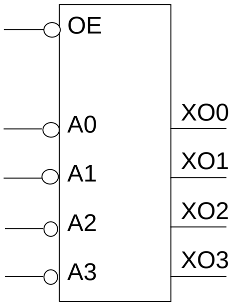
Input		Output
OE	**A0~A$_{n-1}$**	**XO0~XO$_{n-1}$**
0	d	$\overline{d}$
1	x	Z

d = any pattern of 1s and 0s on an input or set of inputs,
$\overline{d}$ = inverse of d, x = don't care, Z = high impedance state.

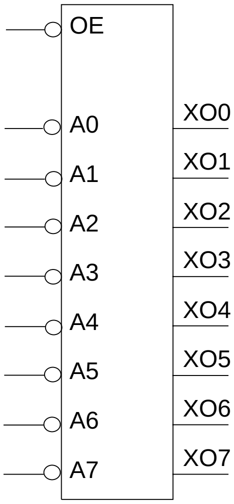
OT41



OT44



OT48



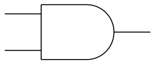
Logic Gates

This chapter contains information on logic gate macros.

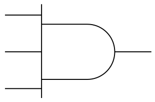
Logic Gates

AND2 through AND18

AND2



AND3



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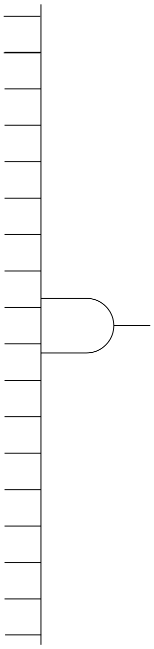
AND18



Function:

2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, and 18 input AND gates.

Availability:

AND2 through AND18 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Logic Primitive

Macro Port Definition:

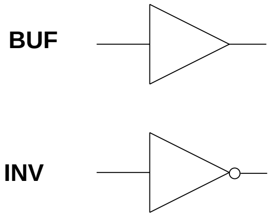
```
AND2 (Z0,A0,A1);
AND3 (Z0,[A0..A2]);
AND4 (Z0,[A0..A3]);
...
AND18 (Z0,[A0..A17]);
```

Truth Table:

The truth table is the same for all ANDs.

Input	Output
All inputs high	High
One or more inputs low	Low

BUF and INV



Function:

BUF: single input buffer.
INV: single input inverter.

Availability:

BUF and INV can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Logic Primitive

Macro Port Definition:

```
BUF (Z0,A0);
INV (ZN0,A0);
```

Truth Tables:

For BUF:

Input	Output
High	High
Low	Low

For INV:

Input	Output
High	Low
Low	High

NAND2 through NAND12, and NAND16

Function:

2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, and 16 input NAND gates.

Availability:

NAND2 through NAND12, and NAND16 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Logic Primitive

Macro Port Definition:

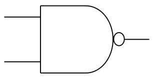
```
NAND2 (ZN0,A0,A1);
NAND3 (ZN0,[A0..A2]);
NAND4 (ZN0,[A0..A3]);
...
NAND12 (ZN0,[A0..A11]);
NAND16 (ZN0,[A0..A15]);
```

Truth Table:

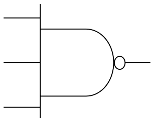
The truth table is the same for all NANDs.

Input	Output
All inputs high	Low
One or more inputs low	High

NAND2

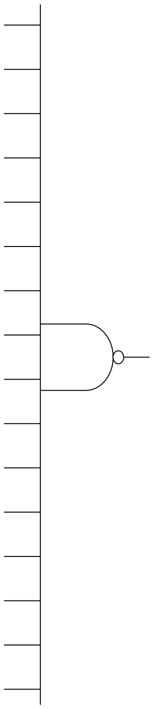


NAND3



...

NAND16



NOR2 through NOR12, and NOR16

Function:

2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, and 16 input NOR gates.

Availability:

NOR2 through NOR12, and NOR16 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Logic Primitive

Macro Port Definition:

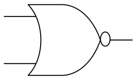
```
NOR2 (ZN0,A0,A1);
NOR3 (ZN0,[A0..A2]);
NOR4 (ZN0,[A0..A3]);
...
NOR12 (ZN0,[A0..A11]);
NOR16 (ZN0,[A0..A15]);
```

Truth Table:

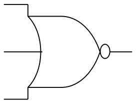
The truth table is the same for all NORs.

Input	Output
All inputs low	High
One or more inputs high	Low

NOR2

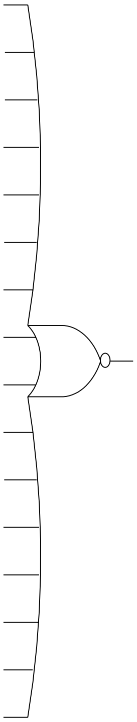


NOR3



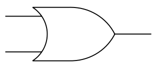
...

NOR16

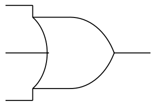


OR2 through OR12, and OR16

OR2

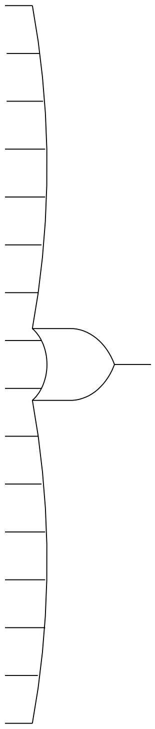


OR3



...

OR16



Function:

2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, and 16 input OR gates.

Availability:

OR2 through OR12, and OR16 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Logic Primitive

Macro Port Definition:

```
OR2 (Z0,A0,A1);
OR3 (Z0,[A0..A2]);
OR4 (Z0,[A0..A3]);
...
OR12 (Z0,[A0..A11]);
OR16 (Z0,[A0..A15]);
```

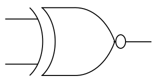
Truth Table:

The truth table is the same for all ORs.

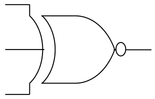
Input	Output
All inputs low	Low
One or more inputs high	High

XNOR2, XNOR3, XNOR4, XNOR7, XNOR8, and XNOR9

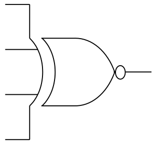
XNOR2



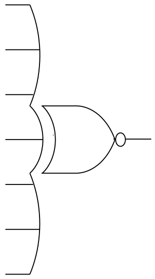
XNOR3



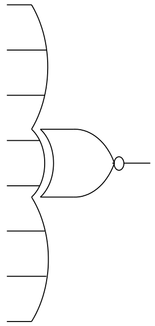
XNOR4



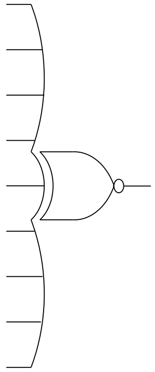
XNOR7



XNOR8



XNOR9



Function:

2, 3, 4, 7, 8, and 9 input XNOR gates.

Availability:

XNOR2, XNOR3, XNOR4, XNOR7, XNOR8, and XNOR9 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type:

Logic Primitive:	XNOR2, XNOR3, and XNOR4.
Soft:	XNOR9.
Hard:	XNOR7 and XNOR8.

Logic Resources:

Macro	PT	GLB	Output	Level
XNOR2	2	.25	1	1
XNOR3	4	.25	1	1
XNOR4	8	.5	1	1
XNOR7	12	1	1	1
XNOR8	16	1	1	1

* ZN0: 2 PT B0: 16 PT

Macro Port Definition:

```
XNOR2 (ZN0,A0,A1);
XNOR3 (ZN0,[A0..A2]);
XNOR4 (ZN0,[A0..A3]);
XNOR7 (ZN0,[A0..A6]);
XNOR8 (ZN0,[A0..A7]);
XNOR9 (ZN0,[A0..A8]);
  XNOR9_1 (B0,[A0..A7]);
  XNOR9_2 (ZN0,B0,A8);
```

Truth Table:

The truth table is the same for all XNORs.

Input	Output
All inputs low	High
Odd number of inputs high	Low
Even number of inputs high	High

XOR2, LXOR2, XOR3, XOR4, XOR8, and XOR9

Function:

2, 3, 4, 8, and 9 input XOR gates.

Availability:

LXOR2, XOR2, XOR3, XOR4, XOR8, and XOR9 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type:

Logic Primitive:	XOR2, XOR3, and XOR4.
Soft:	XOR9.
Hard:	XOR8.
Physical (in the silicon):	LXOR2.

LXOR2 specifies the use of the physical XOR2 gate in the GLB. See the *Lattice Semiconductor Data Book* for more information.

Logic Resources:

Macro	PT	GLB	Output	Level
XOR2	2	.25	1	1
XOR3	4	.25	1	1
XOR4	8	.5	1	1
XOR8	16	1	1	1

* Z0: 2 PT B0: 16 PT

LXOR2: depends on usage.

Macro Port Definition:

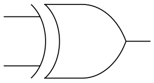
```
XOR2 (Z0,A0,A1);
LXOR2 (Z0,A0,A1);
XOR3 (Z0,[A0..A2]);
XOR4 (Z0,[A0..A3]);
XOR8 (Z0,[A0..A7]);
XOR9 (Z0,[A0..A8]);
  XOR9_1 (B0,[A0..A7]);
  XOR9_2 ([Z0,B0,A8);
```

Truth Table:

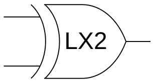
The truth table is the same for all XORs.

Input	Output
All inputs low	Low
Odd number of inputs high	High
Even number of inputs high	Low

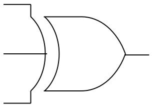
XOR2



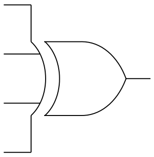
LXOR2



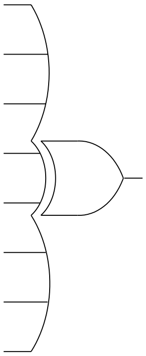
XOR3



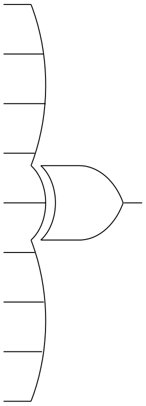
XOR4



XOR8



XOR9



MUX/DMUX

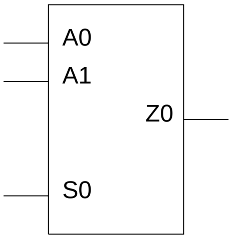
This chapter contains information on the following macros:

- Multiplexers
- Demultiplexers

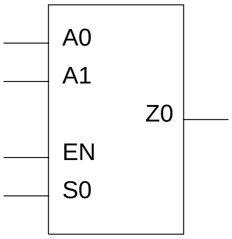
Multiplexers

MUX2 and MUX2E

MUX2



MUX2E



Function:

MUX2: 1 of 2 input mux.
MUX2E: 1 of 2 input mux with enable.

Availability:

Both MUX2 and MUX2E can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Soft

Macro Port Definition:

```
MUX2 (Z0,A0,A1,S0);
MUX2E (Z0,A0,A1,EN,S0);
```

Truth Table:

Gray areas (EN) apply only to MUX2E.

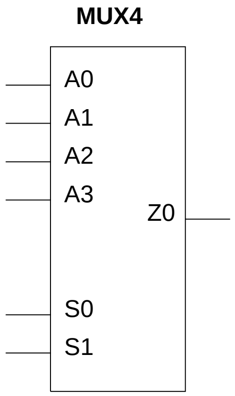
Input		Output
EN	**S0**	**Z0**
1	0	A0
1	1	A1
0	x	0

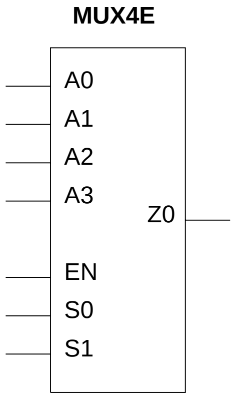
A0..A_{n-1} = inputs, x = don’t care.

MUX4 and MUX4E

Function:

MUX4:	1 of 4 input mux.
MUX4E:	1 of 4 input mux with enable.





Availability:

Both MUX4 and MUX4E can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Soft

Macro Port Definition:

```
MUX4 (Z0,[A0..A3],S0,S1);
MUX4E (Z0,[A0..A3],EN,S0,S1);
```

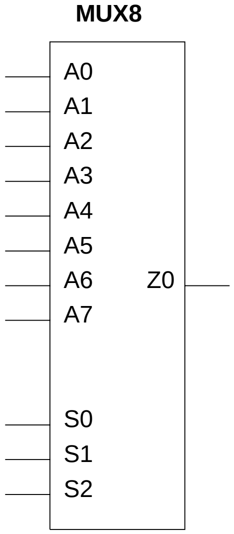
Truth Table:

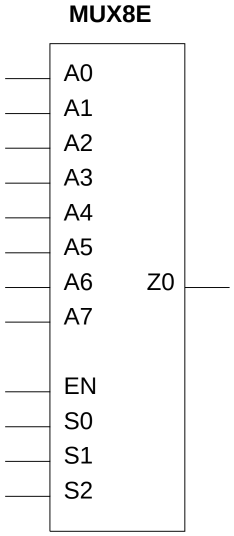
Gray areas (EN) apply only to MUX4E.

Input			Output
EN	**S1**	**S0**	**Z0**
1	0	0	A0
1	0	1	A1
1	1	0	A2
1	1	1	A3
0	x	x	0

A0..A_{n-1} = inputs, x = don’t care.

MUX8 and MUX8E





Function:

MUX8:	1 of 8 input mux.
MUX8E:	1 of 8 input mux with enable.

Availability:

Both MUX8 and MUX8E can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Soft

Macro Port Definition:

```
MUX8 (Z0,[A0..A7],[S0..S2]);
MUX8E (Z0,[A0..A7],EN,[S0..S2]);
```

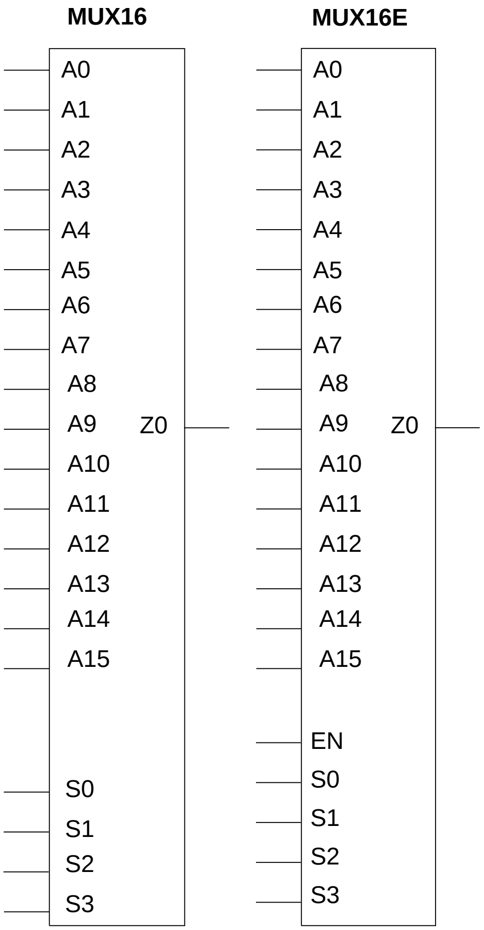
Truth Table:

Gray areas (EN) apply only to MUX8E.

Input				Output
EN	**S2**	**S1**	**S0**	**Z0**
1	0	0	0	A0
1	0	0	1	A1
1	0	1	0	A2
1	0	1	1	A3
1	1	0	0	A4
1	1	0	1	A5
1	1	1	0	A6
1	1	1	1	A7
0	x	x	x	0

A0..A_{n-1} = inputs, x = don’t care.

MUX16 and MUX16E



Function:

MUX16:	One of 16 input mux.
MUX16E:	One of 16 input mux with enable.

Availability:

Both MUX16 and MUX16E can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Schematics appear on the following pages.

Type: Soft

Macro Port Definition:

```
MUX16 (Z0,[A0..A15],[S0..S3]);
MUX16E (Z0,[A0..A15],EN,[S0..S3]);
```

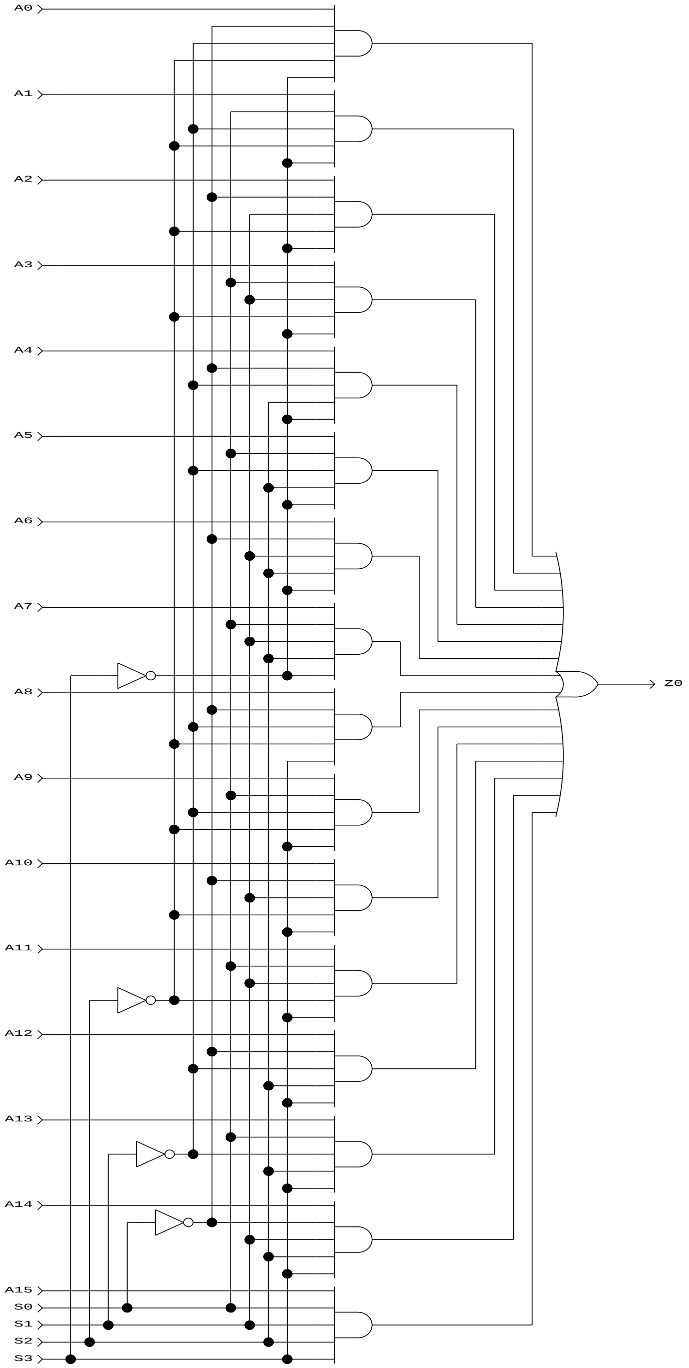
Truth Table:

Gray areas (EN) apply only to MUX16E.

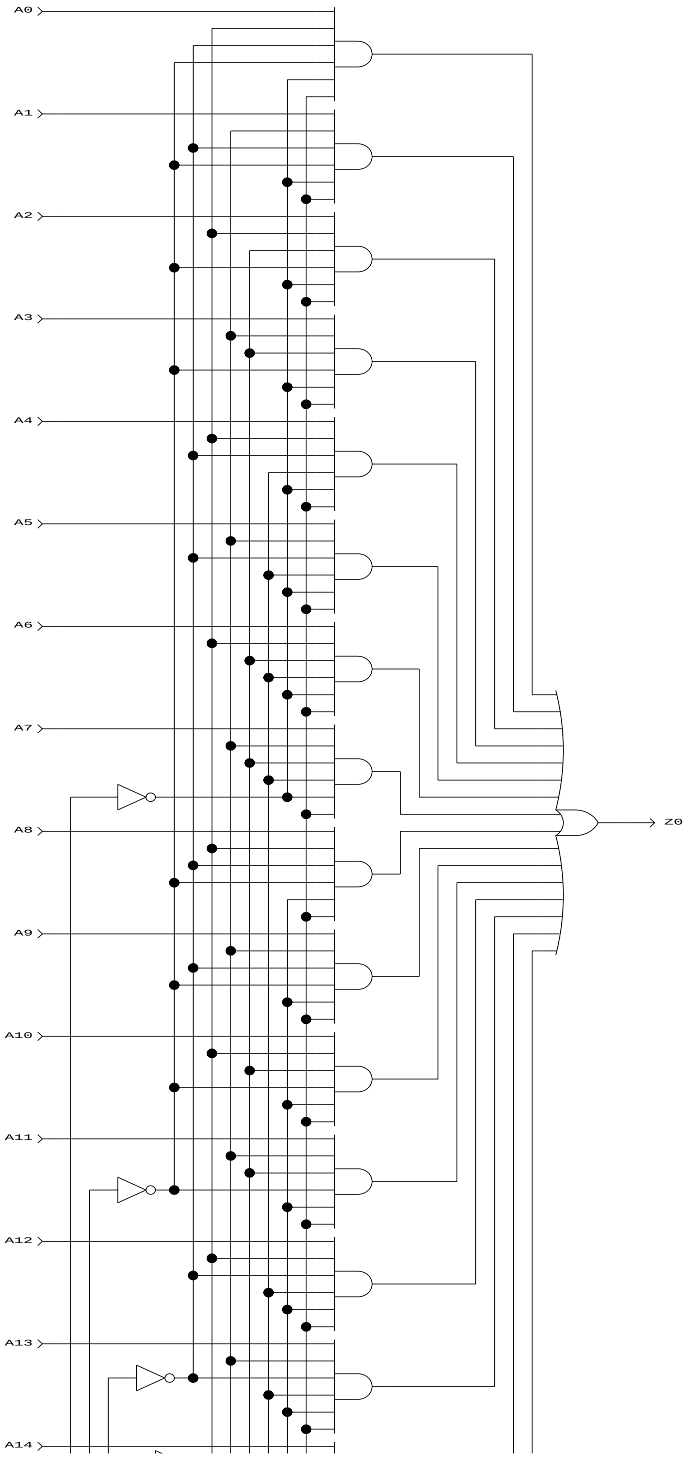
Input					Output
EN	**S3**	**S2**	**S1**	**S0**	**Z0**
1	0	0	0	0	A0
1	0	0	0	1	A1
1	0	0	1	0	A2
1	0	0	1	1	A3
1	0	1	0	0	A4
1	0	1	0	1	A5
1	0	1	1	0	A6
1	0	1	1	1	A7
1	1	0	0	0	A8
1	1	0	0	1	A9
1	1	0	1	0	A10
1	1	0	1	1	A11
1	1	1	0	0	A12
1	1	1	0	1	A13
1	1	1	1	0	A14
1	1	1	1	1	A15
0	x	x	x	x	0

A0..A_{n-1} = inputs, x = don’t care.

MUX16



MUX16E

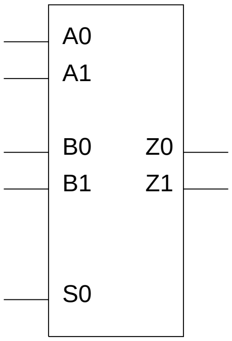


MUX22 and MUX22E

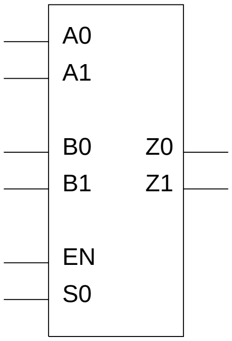
Function:

MUX22: Dual 1 of 2 input mux with common select line.
MUX22E: Dual 1 of 2 input mux with common select line and enable.

MUX22



MUX22E



Availability:

Both MUX22 and MUX22E can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Soft

Macro Port Definition:

```
MUX22 (Z0,Z1,A0,A1,B0,B1,S0);
MUX22E (Z0,Z1,A0,A1,B0,B1,EN,S0);
```

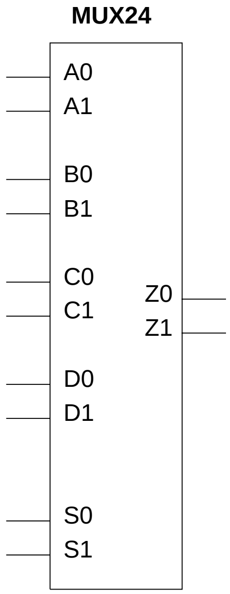
Truth Table:

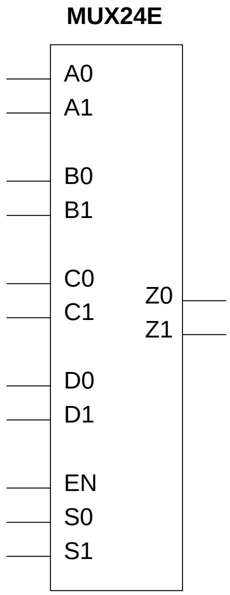
Gray areas (EN) apply only to MUX22E.

Input		Output	
EN	**S0**	**Z0**	**Z1**
1	0	A0	A1
1	1	B0	B1
0	x	0	0

A0..A_{n-1} = inputs, B0..B_{n-1} = inputs,
x = don’t care.

MUX24 and MUX24E





Function:

MUX24: Dual 1 of 4 input mux with common select line.
MUX24E: Dual 1 of 4 input mux with common select line and enable.

Availability:

Both MUX24 and MUX24E can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Soft

Macro Port Definition:

```
MUX24 (Z0,Z1,A0,A1,B0,B1,C0,C1,D0,D1,S0,S1);
MUX24E (Z0,Z1,A0,A1,B0,B1,C0,C1,D0,D1,EN,S0,S1);
```

Truth Table:

Gray areas (EN) apply only to MUX24E.

Input			Output	
EN	**S1**	**S0**	**Z0**	**Z1**
1	0	0	A0	A1
1	0	1	B0	B1
1	1	0	C0	C1
1	1	1	D0	D1
0	x	x	0	0

A0..A_{n-1} = inputs, B0..B_{n-1} = inputs,
x = don't care.

MUX42 and MUX42E

Function:

MUX42: Quad 1 of 2 input mux with common select line.
MUX42E: Quad 1 of 2 input mux with common select line and enable.

Availability:

Both MUX42 and MUX42E can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Soft

Macro Port Definition:

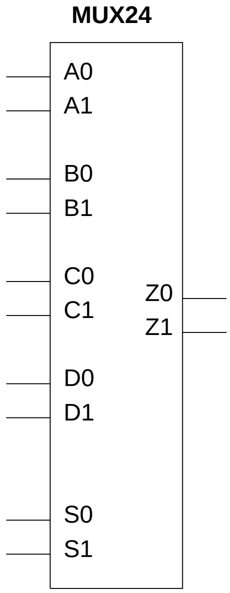
```
MUX42 ([Z0..Z3],[A0..A3],[B0..B3],S0);
MUX42E ([Z0..Z3],[A0..A3],[B0..B3],EN,S0);
```

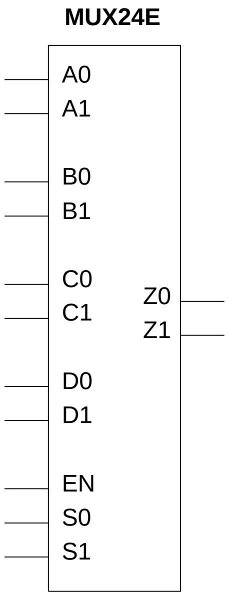
Truth Table:

Gray areas (EN) apply only to MUX42E.

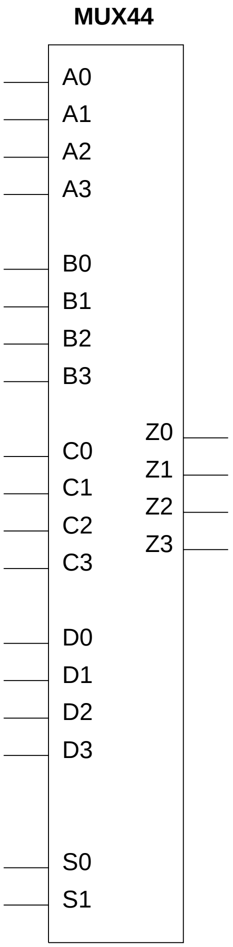
Input		Output			
EN	**S0**	**Z0**	**Z1**	**Z2**	**Z3**
1	0	A0	A1	A2	A3
1	1	B0	B1	B2	B3
0	x	0	0	0	0

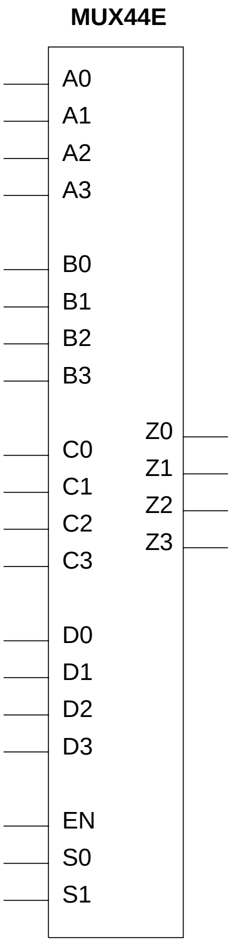
A0..A_{n-1} = inputs, B0..B_{n-1} = inputs,
x = don't care.





MUX44 and MUX44E





Function:

MUX44:	Quad 1 of 4 input mux with common select line.
MUX44E:	Quad 1 of 4 input mux with common select line and enable.

Availability:

Both MUX44 and MUX44E can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Soft

Macro Port Definition:

```
MUX44 ([Z0..Z3],[A0..A3],[B0..B3],
       [C0..C3],[D0..D3],S0,S1);
  MUX44_1 (Z0,Z1,A0,A1,B0,B1,C0,C1,
           D0,D1,S0,S1);
  MUX44_2 (Z2,Z3,A2,A3,B2,B3,C2,C3,
           D2,D3,S0,S1);
MUX44E ([Z0..Z3],[A0..A3],[B0..B3],
        [C0..C3],[D0..D3],EN,S0,S1);
  MUX44E_1 (Z0,Z1,A0,A1,B0,B1,C0,C1,
            D0,D1,EN,S0,S1);
  MUX44E_2 (Z2,Z3,A2,A3,B2,C3,C2,C3,
            D2,D3,EN,S0,S1);
```

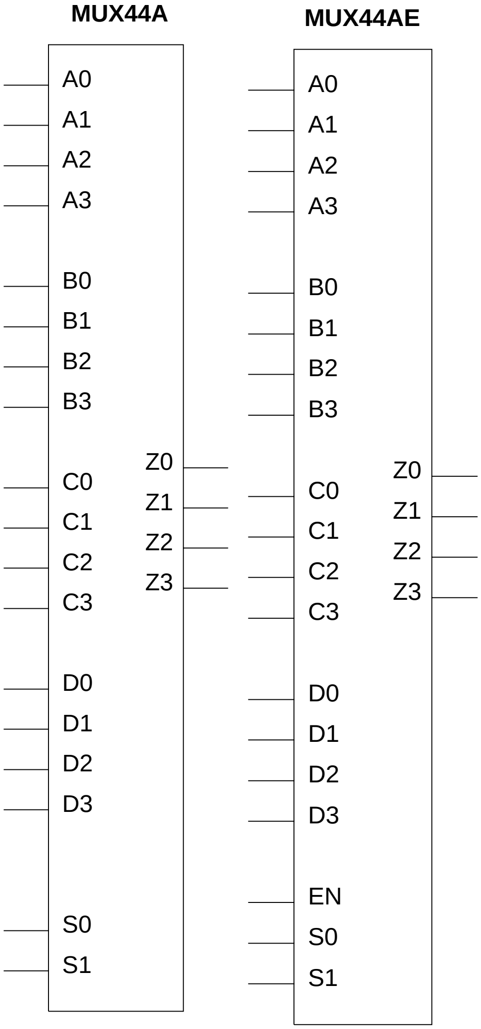
Truth Table:

Gray areas (EN) apply only to MUX44E.

Input			Output			
EN	**S1**	**S0**	**Z0**	**Z1**	**Z2**	**Z3**
1	0	0	A0	A1	A2	A3
1	0	1	B0	B1	B2	B3
1	1	0	C0	C1	C2	C3
1	1	1	D0	D1	D2	D3
0	x	x	0	0	0	0

A0..A_{n-1} = inputs, B0..B_{n-1} = inputs, x = don’t care, C0..C_{n-1} = inputs, D0..D_{n-1} = inputs.

MUX44A and MUX44AE



Function:

MUX44A: Quad 1 of 4 input mux with common select line.
MUX44AE: Quad 1 of 4 input mux with common select line and enable.

Availability:

Both MUX44A and MUX44AE can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Schematics appear on the following pages.

Type: Soft

Macro Port Definition:

```
MUX44A  ([Z0..Z3],[A0..A3],[B0..B3],
         [C0..C3],[D0..D3],S0,S1);
MUX44AE ([Z0..Z3],[A0..A3],[B0..B3],
         [C0..C3],[D0..D3],EN,S0,S1);
```

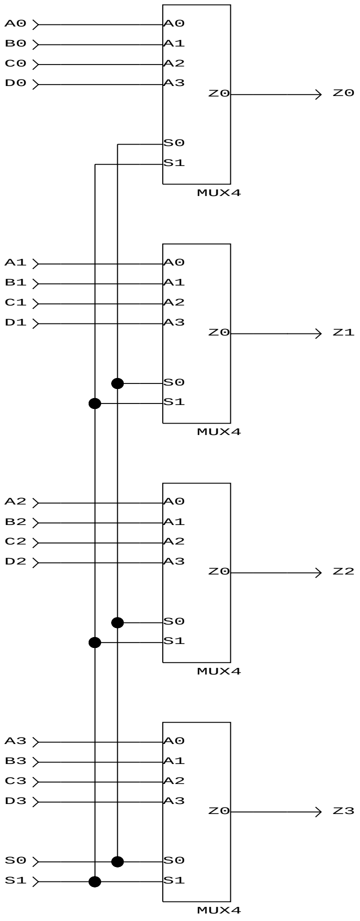
Truth Table:

Gray areas (EN) apply only to MUX44AE.

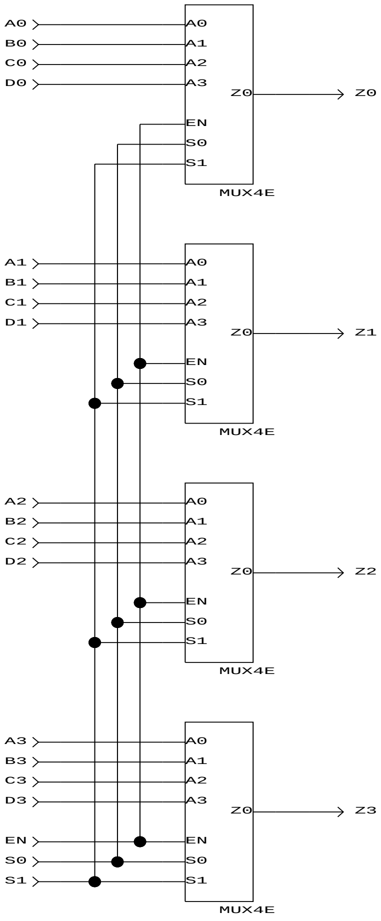
Input			Output			
EN	**S1**	**S0**	**Z0**	**Z1**	**Z2**	**Z3**
1	0	0	A0	A1	A2	A3
1	0	1	B0	B1	B2	B3
1	1	0	C0	C1	C2	C3
1	1	1	D0	D1	D2	D3
0	x	x	0	0	0	0

A0..A_{n-1} = inputs, B0..B_{n-1} = inputs, x = don’t care,
C0..C_{n-1} = inputs, D0..D_{n-1} = inputs.

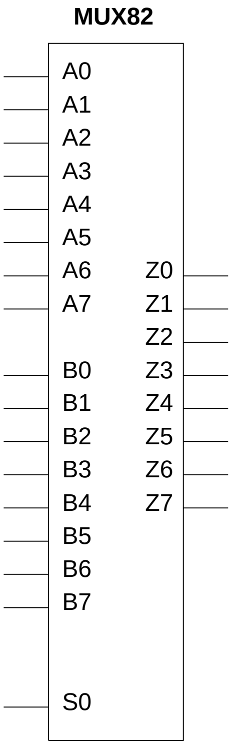
MUX44A


A0
B0
C0
D0
A0
A1
A2
A3
Z0
S0
S1
MUX4
Z0
A1
B1
C1
D1
A0
A1
A2
A3
Z0
S0
S1
MUX4
Z1
A2
B2
C2
D2
A0
A1
A2
A3
Z0
S0
S1
MUX4
Z2
A3
B3
C3
D3
S0
S1
A0
A1
A2
A3
Z0
S0
S1
MUX4
Z3

MUX44AE


A0
B0
C0
D0
A0
A1
A2
A3
Z0
Z0
EN
S0
S1
MUX4E
A1
B1
C1
D1
A0
A1
A2
A3
Z0
Z1
EN
S0
S1
MUX4E
A2
B2
C2
D2
A0
A1
A2
A3
Z0
Z2
EN
S0
S1
MUX4E
A3
B3
C3
D3
EN
S0
S1
A0
A1
A2
A3
Z0
Z3
EN
S0
S1
MUX4E

MUX82 and MUX82E



Function:

MUX82: Octal 1 of 2 input mux with common select line.
MUX82E: Octal 1 of 2 input mux with common select line and enable.

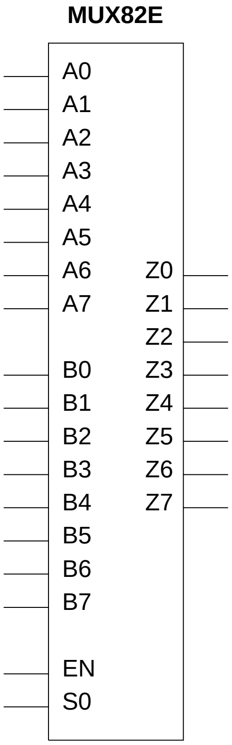
Availability:

Both MUX82 and MUX82E can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Soft

Macro Port Definition:

```
MUX82 ([Z0..Z7],[A0..A7],[B0..B7],S0);
  MUX82_1 ([Z0..Z3],[A0..A3],[B0..B3],S0);
  MUX82_2 ([Z4..Z7],[A4..A7],[B4..B7],S0);
MUX82E ([Z0..Z7],[A0..A7],[B0..B7],EN,S0);
  MUX82E_1 ([Z0..Z3],[A0..A3],[B0..B3],EN,S0);
  MUX82E_2 ([Z4..Z7],[A4..A7],[B4..B7],EN,S0);
```



Truth Table:

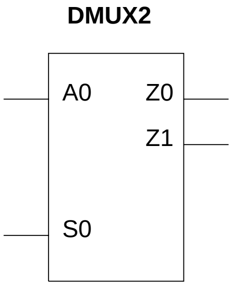
Gray areas (EN) apply only to MUX82E.

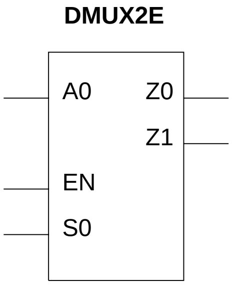
Input		Output							
EN	**S0**	**Z0**	**Z1**	**Z2**	**Z3**	**Z4**	**Z5**	**Z6**	**Z7**
1	0	A0	A1	A2	A3	A4	A5	A6	A7
1	1	B0	B1	B2	B3	B4	B5	B6	B7
0	x	0	0	0	0	0	0	0	0

A0..A_{n-1} = inputs, B0..B_{n-1} = inputs, x = don’t care.

Demultiplexers

DMUX2 and DMUX2E





Function:

DMUX2: 1 of 2 output demux.
DMUX2E: 1 of 2 output demux with enable.

Availability:

Both DMUX2 and DMUX2E can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Soft

Macro Port Definition:

```
DMUX2 (Z0,Z1,A0,S0);
DMUX2E Z0,Z1,A0,EN,S0);
```

Truth Table:

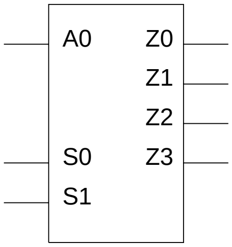
Gray areas (EN) apply only to DMUX2E.

Input		Output	
EN	**S0**	**Z0**	**Z1**
1	0	A0	0
1	1	0	A0
0	x	0	0

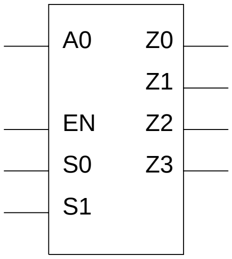
A0..A_{n-1} = inputs, x = don’t care.

DMUX4 and DMUX4E

DMUX4



DMUX4E



Function:

DMUX4: 1 of 4 output demux.
DMUX4E: 1 of 4 output demux with enable.

Availability:

Both DMUX4 and DMUX4E can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Soft

Macro Port Definition:

```
DMUX4 ([Z0..Z3],A0,S0,S1);
DMUX4E ([Z0..Z3],A0,EN,S0,S1);
```

Truth Table:

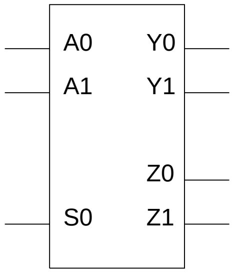
Gray areas (EN) apply only to DMUX4E.

Input			Output			
EN	**S1**	**S0**	**Z0**	**Z1**	**Z2**	**Z3**
1	0	0	A0	0	0	0
1	0	1	0	A0	0	0
1	1	0	0	0	A0	0
1	1	1	0	0	0	A0
0	x	x	0	0	0	0

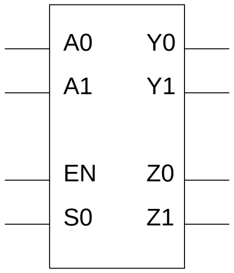
A0..A_{n-1} = inputs, x = don’t care.

DMUX22 and DMUX22E

DMUX22



DMUX22E



Function:

DMUX22: Dual 1 of 2 output demux with common select line.
DMUX22E: Dual 1 of 2 output demux with common select line and enable.

Availability:

Both DMUX22 and DMUX22E can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Soft

Macro Port Definition:

```
DMUX22 (Y0,Y1,Z0,Z1,A0,A1,S0);
DMUX22E (Y0,Y1,Z0,Z1,A0,A1,EN,S0);
```

Truth Table:

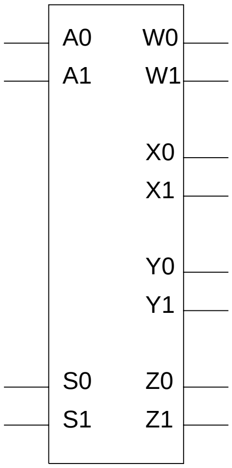
Gray areas (EN) apply only to DMUX22E.

Input		Output			
EN	**S0**	**Y0**	**Y1**	**Z0**	**Z1**
1	0	A0	A1	0	0
1	1	0	0	A0	A1
0	x	0	0	0	0

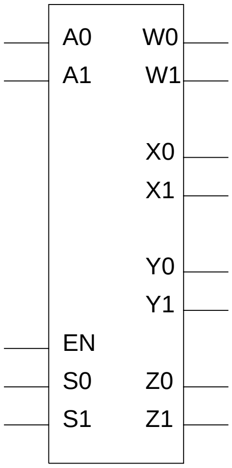
A0..A_{n-1} = inputs, x = don’t care.

DMUX24 and DMUX24E

DMUX24



DMUX24E



Function:

DMUX24: Dual 1 of 4 output demux with common select line.
DMUX24E: Dual 1 of 4 output demux with common select line and enable.

Availability:

Both DMUX24 and DMUX24E can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Soft

Macro Port Definition:

```
DMUX24 (W0,W1,X0,X1,Y0,Y1,Z0,Z1,A0,A1,S0,S1);
  DMUX24_1 (W0,X0,Y0,Z0,A0,S0,S1);
  DMUX24_2 (W1,X1,Y1,Z1,A1,S0,S1);
DMUX24E (W0,W1,X0,X1,Y0,Y1,Z0,Z1,A0,A1,EN,S0,S1);
  DMUX24E_1 (W0,X0,Y0,Z0,A0,EN,S0,S1);
  DMUX24E_2 (W1,X1,Y1,Z1,A1,EN,S0,S1);
```

Truth Table:

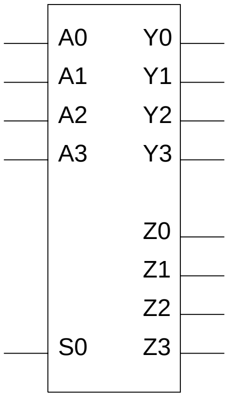
Gray areas (EN) apply only to DMUX24E.

Input			Output							
EN	**S1**	**S0**	**W0**	**W1**	**X0**	**X1**	**Y0**	**Y1**	**Z0**	**Z1**
1	0	0	A0	A1	0	0	0	0	0	0
1	0	1	0	0	A0	A1	0	0	0	0
1	1	0	0	0	0	0	A0	A1	0	0
1	1	1	0	0	0	0	0	0	A0	A1
		x	0	0	0	0	0	0	0	0

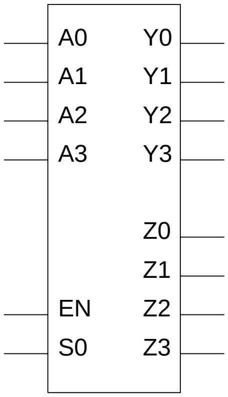
A0..A_{n-1} = inputs, x = don’t care.

DMUX42 and DMUX42E

DMUX42



DMUX42E



Function:

DMUX42: Quad 1 of 2 output demux with common select line.
DMUX42E: Quad 1 of 2 output demux with common select line and enable.

Availability:

Both DMUX42 and DMUX42E can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Soft

Macro Port Definition:

```
DMUX42 ([Y0..Y3],[Z0..Z3],[A0..A3],S0);
  DMUX42_1 (Y0,Y1,Z0,Z1,A0,A1,S0);
  DMUX42_2 (Y2,Y3,Z2,Z3,A2,A3,S0);
DMUX42E ([Y0..Y3],[Z0..Z3],[A0..A3],EN,S0);
  DMUX42E_1 (Y0,Y1,Z0,Z1,A0,A1,EN,S0);
  DMUX42E_2 (Y2,Y3,Z2,Z3,A2,A3,EN,S0);
```

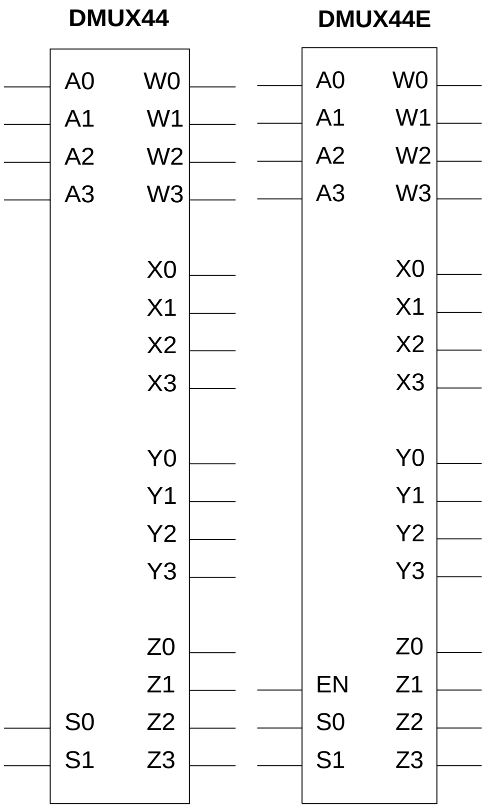
Truth Table:

Gray areas (EN) apply only to DMUX42E.

Input		Output							
EN	**S0**	**Y0**	**Y1**	**Y2**	**Y3**	**Z0**	**Z1**	**Z2**	**Z3**
1	0	A0	A1	A2	A3	0	0	0	0
1	1	0	0	0	0	A0	A1	A2	A3
0	x	0	0	0	0	0	0	0	0

A0..A_{n-1} = inputs, x = don’t care.

DMUX44 and DMUX44E



Function:

DMUX44:	Quad 1 of 4 output demux with common select line.
DMUX44E:	Quad 1 of 4 output demux with common select line enable.

Availability:

Both DMUX44 and DMUX44E can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Soft

Macro Port Definition:

```
DMUX44 ([W0..W3],[X0..X3],[Y0..Y3],
        [Z0..Z3],[A0..A3],S0,S1);
  DMUX44_1 (W0,X0,Y0,Z0,A0,S0,S1);
  DMUX44_2 (W1,X1,Y1,Z1,A1,S0,S1);
  DMUX44_3 (W2,X2,Y2,Z2,A2,S0,S1);
  DMUX44_4 (W3,X3,Y3,Z3,A3,S0,S1);
DMUX44E ([W0..W3],[X0..X3],[Y0..Y3],
         [Z0..Z3],[A0..A3],EN,S0,S1);
  DMUX44E_1 (W0,X0,Y0,Z0,A0,EN,S0,S1);
  DMUX44E_2 (W1,X1,Y1,Z1,A1,EN,S0,S1);
  DMUX44E_3 (W2,X2,Y2,Z2,A2,EN,S0,S1);
  DMUX44E_4 (W3,X3,Y3,Z3,A3,EN,S0,S1);
```

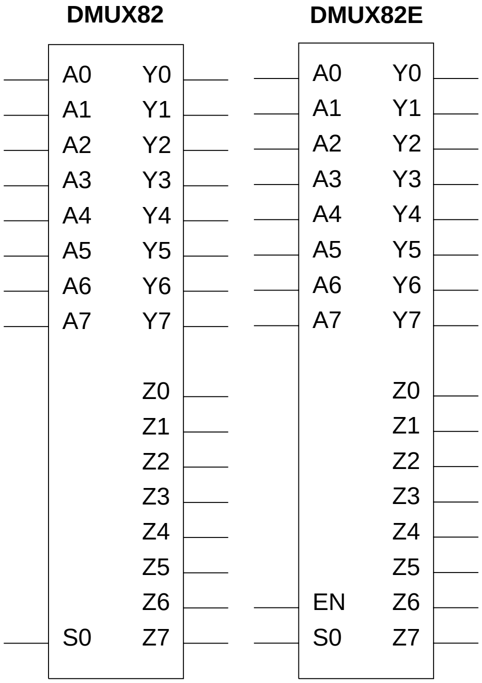
Truth Table:

Gray areas (EN) apply only to DMUX44E.

Input			Output															
EN	**S1**	**S0**	**W0**	**W1**	**W2**	**W3**	**X0**	**X1**	**X2**	**X3**	**Y0**	**Y1**	**Y2**	**Y3**	**Z0**	**Z1**	**Z2**	**Z3**
1	0	0	A0	A1	A2	A3	0	0	0	0	0	0	0	0	0	0	0	0
1	0	1	0	0	0	0	A0	A1	A2	A3	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	0	A0	A1	A2	A3	0	0	0	0
1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	A0	A1	A2	A3
0	x	x	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

A0..A_{n-1} = inputs, x = don’t care.

DMUX82 and DMUX82E



Function:

DMUX82: Octal 1 of 2 output demux with common select line.
DMUX82E: Octal 1 of 2 output demux with common select line and enable.

Availability:

Both DMUX82 and DMUX82E can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Soft

Macro Port Definition:

```
DMUX82 ([Y0..Y7],[Z0..Z7],[A0..A7],S0);
  DMUX82_1 (Y0,Y1,Z0,Z1,A0,A1,S0);
  DMUX82_2 (Y2,Y3,Z2,Z3,A2,A3,S0);
  DMUX82_3 (Y4,Y5,Z4,Z5,A4,A5,S0);
  DMUX82_4 (Y6,Y7,Z6,Z7,A6,A7,S0);
DMUX82E ([Y0..Y7],[Z0..Z7],[A0..A7],EN,S0);
  DMUX82E_1 (Y0,Y1,Z0,Z1,A0,A1,EN,S0);
  DMUX82E_2 (Y2,Y3,Z2,Z3,A2,A3,EN,S0);
  DMUX82E_3 (Y4,Y5,Z4,Z5,A4,A5,EN,S0);
  DMUX82E_4 (Y6,Y7,Z6,Z7,A6,A7,EN,S0);
```

Truth Table:

Gray areas (EN) apply only to DMUX82E.

Input		Output															
EN	**S0**	**Y0**	**Y1**	**Y2**	**Y3**	**Y4**	**Y5**	**Y6**	**Y7**	**Z0**	**Z1**	**Z2**	**Z3**	**Z4**	**Z5**	**Z6**	**Z7**
1	0	A0	A1	A2	A3	A4	A5	A6	A7	0	0	0	0	0	0	0	0
1	1	0	0	0	0	0	0	0	0	A0	A1	A2	A3	A4	A5	A6	A7
0	x	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

A0..A_{n-1} = inputs, x = don't care.

Registers

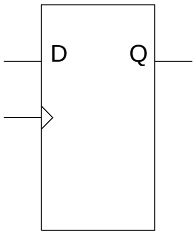
This chapter contains information on the following macros:

- D Flip-Flops
- JK Flip-Flops
- Toggle Flip-Flops
- D Latches
- SR Latches
- Shift Registers

D Flip-flops

FD11, FD14, and FD18

FD11



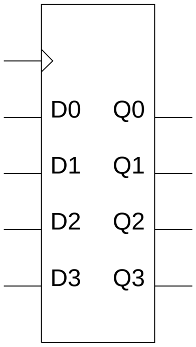
Function:

FD11: 1-bit D flip-flop.
FD14: 4-bit D flip-flop.
FD18: 8-bit D flip-flop.

Availability:

FD11, FD14, and FD18 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

FD14



Type:

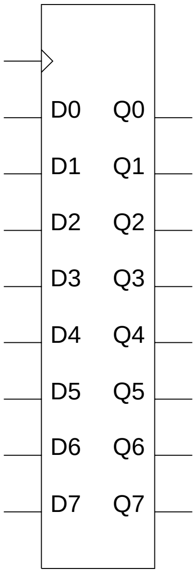
Logic Primitive: FD11
Soft: FD14 and FD18

Logic Resources:

Macro	PT	GLB	Output	Level
FD11	1*	.25	1	1

* Add 1 PT per GLB if Product Term Clock is used.

FD18



Macro Port Definition:

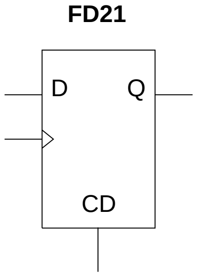
```
FD11 (Q0,D0,CLK);
FD14 ([Q0..Q3],[D0..D3],CLK);
FD18 ([Q0..Q7],[D0..D7],CLK);
```

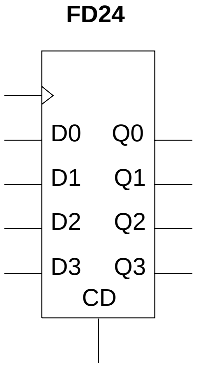
Truth Table:

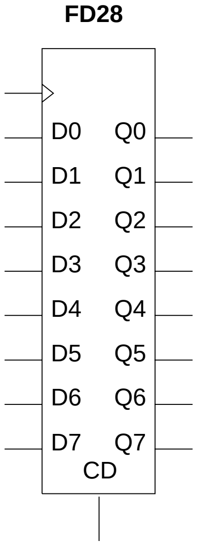
Input		Output
D0~D$_{n-1}$	**CLK**	**Q0~Q$_{n-1}$**
d	↑	d
x	0	Q0'~Qn'
x	1	Q0'~Qn'

d = any pattern of 1s and 0s in an input or set of inputs,
Q0'~Qn' = previous output of flip-flop or latch,
x = don't care, ↑ = rising clock edge.

FD21, FD24, and FD28







Function:

FD21:	1-bit D flip-flop with asynchronous clear.
FD24:	4-bit D flip-flop with asynchronous clear.
FD28:	8-bit D flip-flop with asynchronous clear.

Availability:

FD21, FD24, and FD28 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type:

Logic Primitive:	FD21
Soft:	FD24 and FD28

Logic Resources:

Macro	PT	GLB	Output	Level
FD21	1*	.25	1	1

* Add 1 PT per GLB for CD and 1 per GLB if Product Term Clock is used.

Macro Port Definition:

```
FD21 (Q0,D0,CLK,CD);
FD24 ([Q0..Q3],[D0..D3],CLK,CD);
FD28 ([Q0..Q7],[D0..D7],CLK,CD);
```

Truth Table:

Input			Output
CD	D0~D$_{n-1}$	CLK	Q0~Q$_{n-1}$
1	x	x	0
0	d	↑	d
0	x	0	Q0'~Qn'
0	x	1	Q0'~Qn'

d = any pattern of 1s and 0s in an input or set of inputs,
Q0'~Qn' = previous output of flip-flop or latch, x = don't care,
↑ = rising clock edge.

FD31, FD34, and FD38

Function:

FD31:	1-bit D flip-flop with synchronous preset.
FD34:	4-bit D flip-flop with synchronous preset.
FD38:	8-bit D flip-flop with synchronous preset.

Availability:

FD31, FD34, and FD38 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Soft

Macro Port Definition:

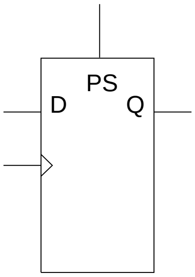
```
FD31 (Q0,D0,CLK,PS);
FD34 ([Q0..Q3],[D0..D3],CLK,PS);
FD38 ([Q0..Q7],[D0..D7],CLK,PS);
```

Truth Table:

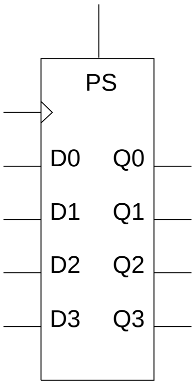
Input			Output
PS	**D0~D_{n-1}**	**CLK**	**Q0~Q_{n-1}**
1	x	↑	1
0	d	↑	d
x	x	0	Q0’~Qn’
x	x	1	Q0’~Qn’

d = any pattern of 1s and 0s in an input or set of inputs,
Q0’~Qn’ = previous output of flip-flop or latch,
x = don’t care, ↑ = rising clock edge.

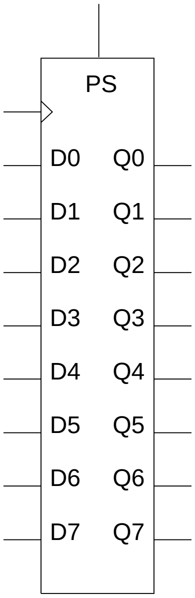
FD31



FD34

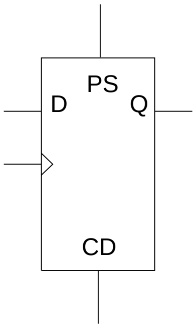


FD38



FD41, FD44, and FD48

FD41



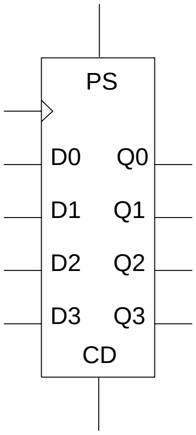
Function:

FD41: 1-bit D flip-flop with asynchronous clear dominant over synchronous preset.
FD44: 4-bit D flip-flop with asynchronous clear dominant over synchronous preset.
FD48: 8-bit D flip-flop with asynchronous clear dominant over synchronous preset.

Availability:

FD41, FD44, and FD48 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

FD44



Type: Soft

Macro Port Definition:

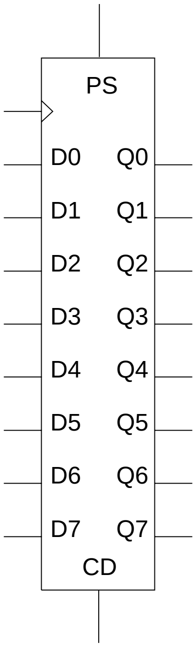
```
FD41 (Q0,D0,CLK,PS,CD);
FD44 ([Q0..Q3],[D0..D3],CLK,PS,CD);
FD48 ([Q0..Q7],[D0..D7],CLK,PS,CD);
```

Truth Table:

Input				Output
CD	**PS**	**D0~D_{n-1}**	**CLK**	**Q0~Q_{n-1}**
1	x	x	x	0
0	1	x	↑	1
0	0	d	↑	d
0	x	x	0	Q0’~Qn’
0	x	x	1	Q0’~Qn’

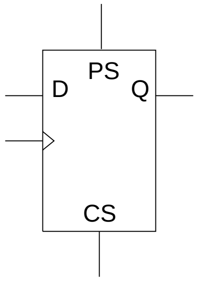
d = any pattern of 1s and 0s in an input or set of inputs,
Q0’~Qn’ = previous output of flip-flop or latch,
x = don’t care, ↑ = rising clock edge.

FD48



FD51, FD54, and FD58

FD51



Function:

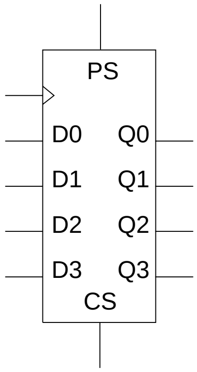
FD51: 1-bit D flip-flop with synchronous preset dominant over synchronous clear.
FD54: 4-bit D flip-flop with synchronous preset dominant over synchronous clear.
FD58: 8-bit D flip-flop with synchronous preset dominant over synchronous clear.

Availability:

FD51, FD54, and FD58 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Soft

FD54



Macro Port Definition:

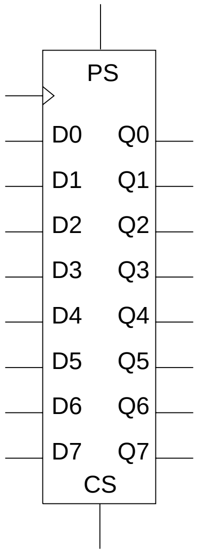
```
FD51 (Q0,D0,CLK,PS,CS);
FD54 ([Q0..Q3],[D0..D3],CLK,PS,CS);
FD58 ([Q0..Q7],[D0..D7],CLK,PS,CS);
```

Truth Table:

Input				Output
PS	**CS**	**D0~D$_{n-1}$**	**CLK**	**Q0~Q$_{n-1}$**
1	x	x	↑	1
0	1	x	↑	0
0	0	d	↑	d
x	x	x	0	Q0'~Qn'
x	x	x	1	Q0'~Qn'

d = any pattern of 1s and 0s in an input or set of inputs,
Q0'~Qn' = previous output of flip-flop or latch,
x = don't care, ↑ = rising clock edge.

FD58



FD61, FD64, and FD68

Function:

FD61: 1-bit D flip-flop with scan.
FD64: 4-bit D flip-flop with scan.
FD68: 8-bit D flip-flop with scan.

Availability:

FD61, FD64, and FD68 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Soft

Macro Port Definition:

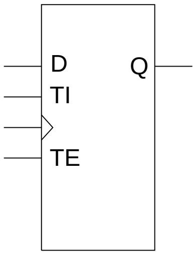
```
FD61 (Q0,D0,TI0,CLK,TE);
FD64 ([Q0..Q3],[D0..D3],[TI0..TI3],CLK,TE);
FD68 ([Q0..Q7],[D0..D7],[TI0..TI7],CLK,TE);
```

Truth Table:

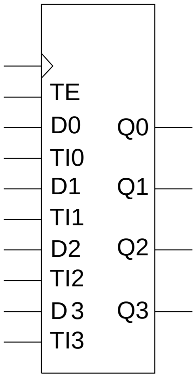
Input				Output
TE	**TI0~TI$_{n-1}$**	**D0~D$_{n-1}$**	**CLK**	**Q0~Q$_{n-1}$**
0	x	d	↑	d
1	d	x	↑	d
x	x	x	0	Q0'~Qn'
x	x	x	1	Q0'~Qn'

d = any pattern of 1s and 0s in an input or set of inputs,
Q0'~Qn' = previous output of flip-flop or latch,
x = don't care, ↑ = rising clock edge.

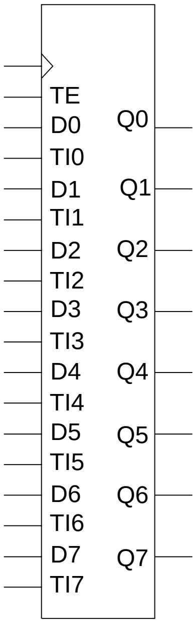
FD61



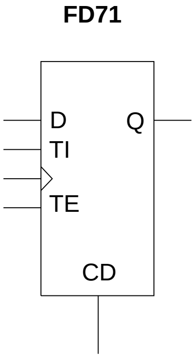
FD64



FD68



FD71, FD74, and FD78



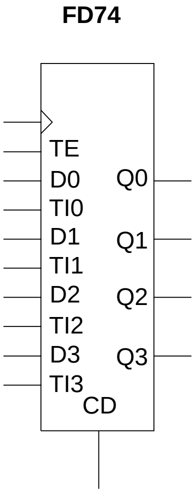
Function:

FD71: 1-bit D flip-flop with scan and asynchronous clear.
FD74: 4-bit D flip-flop with scan and asynchronous clear.
FD78: 8-bit D flip-flop with scan and asynchronous clear.

Availability:

FD71, FD74, and FD78 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Soft



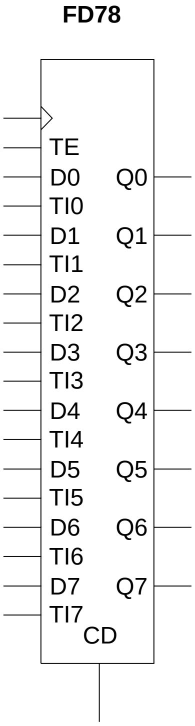
Macro Port Definition:

```
FD71 (Q0,D0,TI0,CLK,CD,TE);
FD74 ([Q0..Q3],[D0..D3],[TI0..TI3],CLK,CD,TE);
FD78 ([Q0..Q7],[D0..D7],[TI0..TI7],CLK,CD,TE);
```

Truth Table:

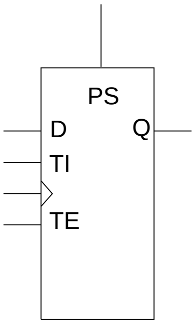
Input					Output
CD	TE	TI0~TI$_{n-1}$	D0~D$_{n-1}$	CLK	Q0~Q$_{n-1}$
1	x	x	x	x	0
0	0	x	d	↑	d
0	1	d	x	↑	d
0	x	x	x	0	Q0’~Qn’
0	x	x	x	1	Q0’~Qn’

d = any pattern of 1s and 0s in an input or set of inputs,
Q0’~Qn’ = previous output of flip-flop or latch, x = don’t care,
↑ = rising clock edge.



FD81, FD84, and FD88

FD81



Function:

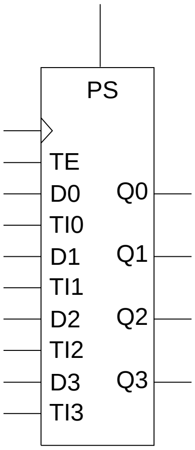
FD81: 1-bit D flip-flop with scan and synchronous preset.
FD84: 4-bit D flip-flop with scan and synchronous preset.
FD88: 8-bit D flip-flop with scan and synchronous preset.

Availability:

FD81, FD84, and FD88 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Soft

FD84



Macro Port Definition:

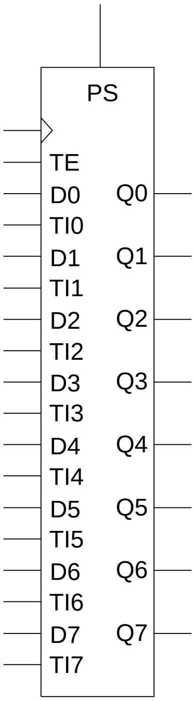
```
FD81 (Q0,D0,TI0,CLK,PS,TE);
FD84 ([Q0..Q3],[D0..D3],[TI0..TI3],CLK,PS,TE);
FD88 ([Q0..Q7],[D0..D7],[TI0..TI7],CLK,PS,TE);
```

Truth Table:

Input					Output
PS	**TE**	**TI0~TI$_{n-1}$**	**D0~D$_{n-1}$**	**CLK**	**Q0~Q$_{n-1}$**
1	x	x	x	↑	1
0	0	x	d	↑	d
0	1	d	x	↑	d
x	x	x	x	0	Q0’~Qn’
x	x	x	x	1	Q0’~Qn’

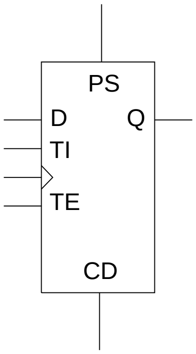
d = any pattern of 1s and 0s in an input or set of inputs,
Q0’~Qn’ = previous output of flip-flop or latch, x = don’t care,
↑ = rising clock edge.

FD88

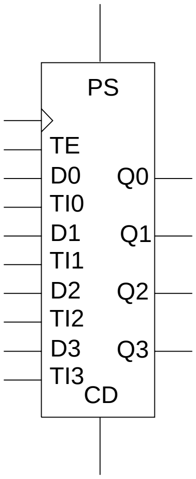


FD91, FD94, and FD98

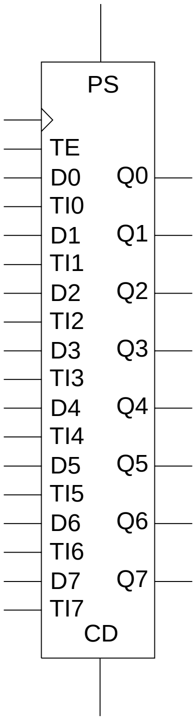
FD91



FD94



FD98



Function:

FD91: 1-bit D flip-flop with scan and asynchronous clear dominant over synchronous preset.
FD94: 4-bit D flip-flop with scan and asynchronous clear dominant over synchronous preset.
FD98: 8-bit D flip-flop with scan and asynchronous clear dominant over synchronous preset.

Availability:

FD91, FD94, and FD98 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Soft

Macro Port Definition:

```
FD91 (Q0,D0,TI0,CLK,PS,CD,TE);
FD94 ([Q0..Q3],[D0..D3],[TI0..TI3],CLK,PS,CD,TE);
FD98 ([Q0..Q7],[D0..D7],[TI0..TI7],CLK,PS,CD,TE);
```

Truth Table:

Input						Output
CD	**PS**	**TE**	**TI0~TI$_{n-1}$**	**D0~D$_{n-1}$**	**CLK**	**Q0~Q$_{n-1}$**
1	x	x	x	x	x	0
0	1	x	x	x	↑	1
0	0	0	x	d	↑	d
0	0	1	d	x	↑	d
0	x	x	x	x	0	Q0'~Qn'
0	x	x	x	x	1	Q0'~Qn'

d = any pattern of 1s and 0s on an input or set of inputs,
Q0'~Qn' = previous output of flip-flop or latch,
x = don't care, ↑ = rising clock edge.

FDA1, FDA4, and FDA8

Function:

FDA1: 1-bit D flip-flop with scan and synchronous preset dominant over synchronous clear.
FDA4: 4-bit D flip-flop with scan and synchronous preset dominant over synchronous clear.
FDA8: 8-bit D flip-flop with scan and synchronous preset dominant over synchronous clear.

Availability:

FDA1, FDA4, and FDA8 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Soft

Macro Port Definition:

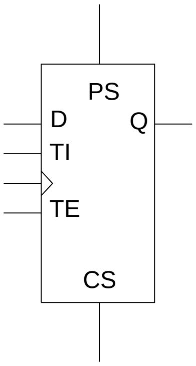
```
FDA1 (Q0,D0,TI0,CLK,PS,CS,TE);
FDA4 ([Q0..Q3],[D0..D3],[TI0..TI3],CLK,PS,CS,TE);
FDA8 ([Q0..Q7],[D0..D7],[TI0..TI7],CLK,PS,CS,TE);
```

Truth Table:

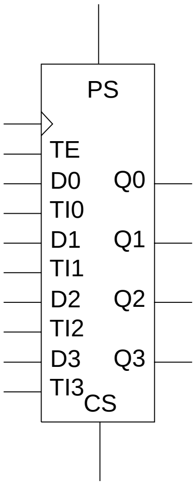
Input						Output
PS	**CS**	**TE**	**TI0~TI$_{n-1}$**	**D0~D$_{n-1}$**	**CLK**	**Q0~Q$_{n-1}$**
1	x	x	x	x	↑	1
0	1	x	x	x	↑	0
0	0	0	x	d	↑	d
0	0	1	d	x	↑	d
x	x	x	x	x	0	Q0'~Qn'
x	x	x	x	x	1	Q0'~Qn'

d = any pattern of 1s and 0s on an input or set of inputs,
Q0'~Qn' = previous output of flip-flop or latch,
x = don't care, ↑ = rising clock edge.

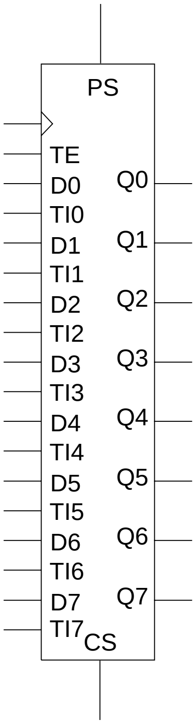
FDA1



FDA4



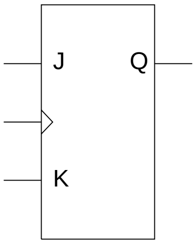
FDA8



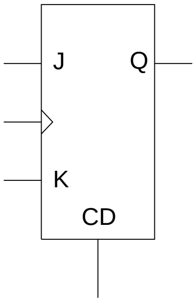
JK Flip-flops

FJK11 and FJK21

FJK11



FJK21



Function:

FJK11: JK flip-flop.
FJK21: JK flip-flop with asynchronous clear.

Availability:

Both FJK11 and FJK21 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Soft

Macro Port Definition:

```
FJK11 (Q0,J0,K0,CLK);
FJK21 (Q0,J0,K0,CLK,CD);
```

Truth Table:

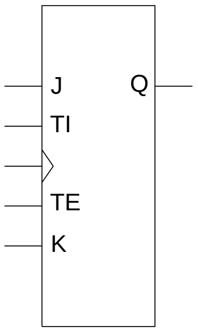
Gray areas (CD) apply only to FJK21.

Input				Output
CD	**J0**	**K0**	**CLK**	**CD**
1	x	x	x	0
0	0	0	↑	Q0’
0	0	1	↑	0
0	1	0	↑	1
0	1	1	↑	$\overline{\text{Q0’}}$
0	x	x	0	Q0’
0	x	x	1	Q0’

Q0’ = previous output of flip-flop or latch,
$\overline{\text{Q0’}}$ = inverse of Q0’, x = don’t care, ↑ = rising clock edge.

FJK31 and FJK41

FJK31



Function:

FJK31: JK flip-flop with scan.
FJK41: JK flip-flop with scan and asynchronous clear.

Availability:

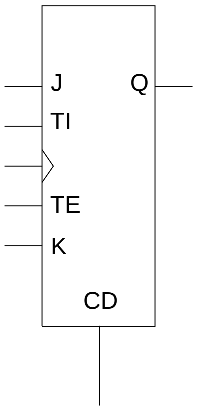
Both FJK31 and FJK41 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Soft

Macro Port Definition:

```
FJK31 (Q0,J0,K0,TI0,CLK,TE);
FJK41 (Q0,J0,K0,TI0,CLK,CD,TE);
```

FJK41



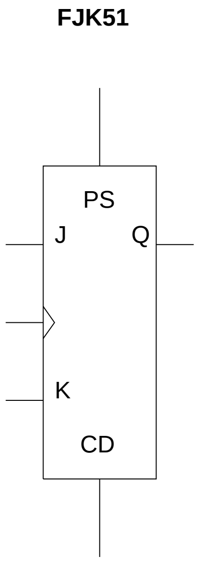
Truth Table:

Gray areas (CD) apply only to FJK41.

Input						Output
CD	**TE**	**TI0**	**J0**	**K0**	**CLK**	**Q0**
1	x	x	x	x	x	0
0	0	x	0	0	↑	Q0’
0	0	x	0	1	↑	0
0	0	x	1	0	↑	1
0	0	x	1	1	↑	$\overline{\text{Q0'}}$
0	1	d	x	x	↑	d
0	x	x	x	x	0	Q0’
0	x	x	x	x	1	Q0’

d = any pattern of 1s and 0s on an input or set of inputs,
Q0’ = previous output of flip-flop or latch, $\overline{\text{Q0'}}$ = inverse of Q0’,
x = don’t care, ↑ = rising clock edge.

FJK51



Function:

JK flip-flop with asynchronous clear and synchronous preset.

Availability:

FJK51 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Soft

Macro Port Definition:

```
FJK51 (Q0,J0,K0,CLK,PS,CD);
```

Truth Table:

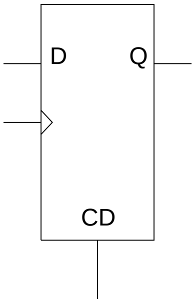
Input					Output
CD	**PS**	**J0**	**K0**	**CLK**	**Q0**
1	x	x	x	x	0
0	1	x	x	↑	1
0	0	0	0	↑	Q0’
0	0	0	1	↑	0
0	0	1	0	↑	1
0	0	1	1	↑	$\overline{\text{Q0'}}$
0	x	x	x	0	Q0’
0	x	x	x	1	Q0’

Q0’ = previous output of flip-flop or latch,
$\overline{\text{Q0'}}$ = inverse of Q0’, x = don’t care, ↑ = rising clock edge.

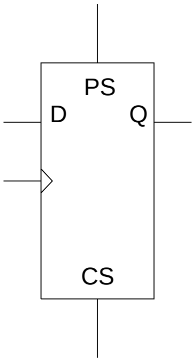
Toggle Flip-flops

FT11 and FT21

FT11



FT21



Function:

FT11: Toggle flip-flop with asynchronous clear.
FT21: Toggle flip-flop with synchronous clear and preset, preset dominant.

Availability:

Both FT11 and FT21 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Soft

Macro Port Definition:

```
FT11 (Q0,D0,CLK,CD);
FT21 (Q0,D0,CLK,PS,CS);
```

Truth Table:

FT11

Input			Output
CD	**D0**	**CLK**	**Q**
1	x	x	0
0	0	↑	Q0’
0	1	↑	$\overline{\text{Q0’}}$
0	x	0	Q0’
0	x	1	Q0’

FT21

Input				Output
PS	**CS**	**D0**	**CLK**	**Q**
1	x	x	↑	1
0	1	x	↑	0
0	0	0	↑	Q0’
0	0	1	↑	$\overline{\text{Q0’}}$
x	x	x	0	Q0’
x	x	x	1	Q0’

Q0’ = previous output of flip-flop or latch,
$\overline{\text{Q0’}}$ = inverse of Q0’, x = don’t care, ↑ = rising clock edge.

D Latches

LD11, LD14, and LD18

Function:

LD11: 1-bit D latch.
LD14: 4-bit D latch.
LD18: 8-bit D latch.

Availability:

LD11, LD14, and LD18 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Hard

Logic Resources:

Macro	PT	GLB	Output	Level
LD11	3	1	1	1
LD14	3/out	1	4	1
LD18	3/out	2	8	1

Macro Port Definition:

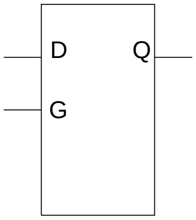
```
LD11 (Q0,D0,G);
LD14 ([Q0..Q3],[D0..D3],G);
LD18 ([Q0..Q7],[D0..D7],G);
```

Truth Table:

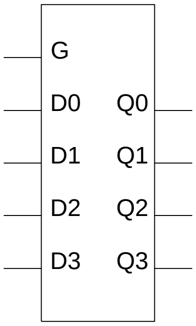
Input		Output
D0~D$_{n-1}$	**G**	**Q0~Q$_{n-1}$**
d	1	d
x	0	Q0'~Qn'

d = any pattern of 1s and 0s on an input or set of inputs,
Q0'~Qn' = previous output of flip-flop or latch, x = don't care.

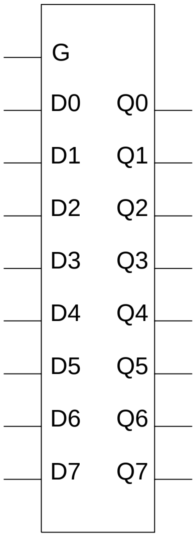
LD11



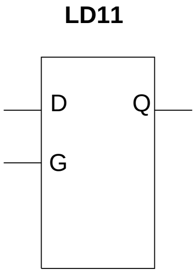
LD14



LD18



LD21, LD24, and LD28



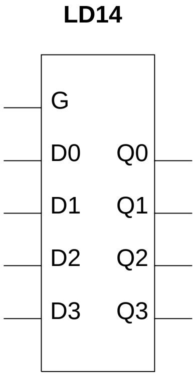
Function:

LD21: 1-bit D latch with asynchronous clear.
LD24: 4-bit D latch with asynchronous clear.
LD28: 8-bit D latch with asynchronous clear.

Availability:

LD21, LD24, and LD28 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Hard

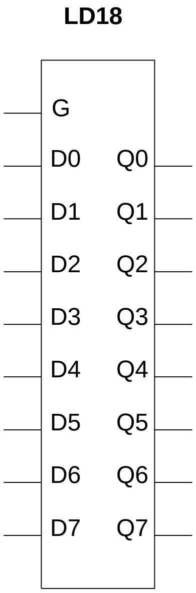


Logic Resources:

Macro	PT	GLB	Output	Level
LD21	3	1	1	1
LD24	3/out	1	4	1
LD28	3/out	2	8	1

Macro Port Definition:

```
LD21 (Q0,D0,G,CD);
LD24 ([Q0..Q3],[D0..D3],G,CD);
LD28 ([Q0..Q7],[D0..D7],G,CD);
```



Truth Table:

Input			Output
CD	**D0~D$_{n-1}$**	**G**	**Q0~Q$_{n-1}$**
1	x	x	0
0	d	1	d
0	x	0	Q0'~Qn'

d = any pattern of 1s and 0s on input or set of inputs,
Q0'~Qn' = previous output of flip-flop or latch, x = don't care.

LD31, LD34, and LD38

Function:

LD31: 1-bit D latch with asynchronous preset.
LD34: 4-bit D latch with asynchronous preset.
LD38: 8-bit D latch with asynchronous preset.

Availability:

LD31, LD34, and LD38 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Hard

Logic Resources:

Macro	PT	GLB	Output	Level
LD31	4	1	1	1
LD34	4/out	2	4	1
LD38	4/out	2	8	1

Macro Port Definition:

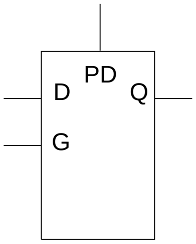
```
LD31 (Q0,D0,G,PD);
LD34 ([Q0..Q3],[D0..D3],G,PD);
LD38 ([Q0..Q7],[D0..D7],G,PD);
```

Truth Table:

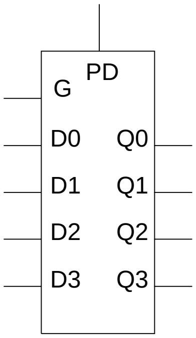
Input			Output
PD	**D0~D$_{n-1}$**	**G**	**Q0~Q$_{n-1}$**
1	x	x	1
0	d	1	d
0	x	0	Q0’~Qn’

d = any pattern of 1s and 0s on an input or set of inputs,
Q0’~Qn’ = previous output of flip-flop or latch, x = don’t care.

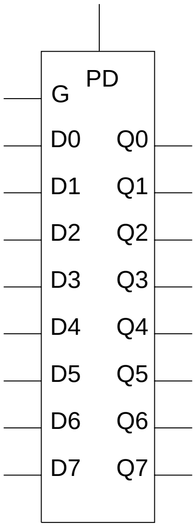
LD31



LD34

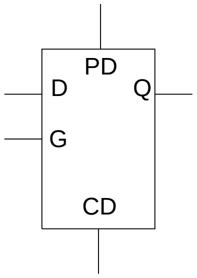


LD38

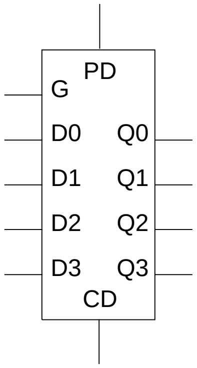


LD41, LD44, and LD48

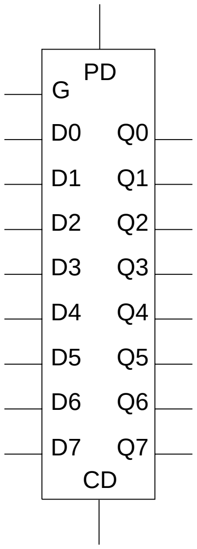
LD41



LD44



LD48



Function:

LD41: 1-bit D latch with asynchronous clear dominant over asynchronous preset.
LD44: 4-bit D latch with asynchronous clear dominant over asynchronous preset.
LD48: 8-bit D latch with asynchronous clear dominant over asynchronous preset.

Availability:

LD41, LD44, and LD48 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Hard

Logic Resources:

Macro	PT	GLB	Output	Level
LD41	4	1	1	1
LD44	4/out	2	4	1
LD48	4/out	2	8	1

Macro Port Definition:

```
LD41 (Q0,D0,G,PD,CD);
LD44 ([Q0..Q3],[D0..D3],G,PD,CD);
LD48 ([Q0..Q7],[D0..D7],G,PD,CD);
```

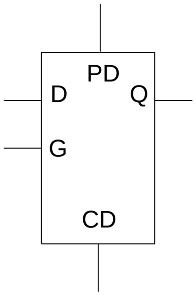
Truth Table:

Input				Output
CD	**PD**	**D0~D$_{n-1}$**	**G**	**Q0~Q$_{n-1}$**
1	x	x	x	0
0	1	x	x	1
0	0	d	1	d
0	0	x	0	Q0’~Qn’

d = any pattern of 1s and 0s on an input or set of inputs,
Q0’~Qn’ = previous output of flip-flop or latch, x = don’t care.

LD51, LD54, and LD58

LD51



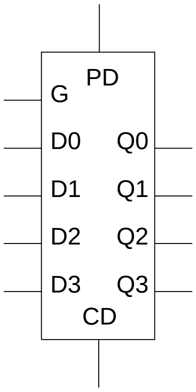
Function:

LD51:	1-bit D latch with asynchronous preset dominant over asynchronous clear.
LD54:	4-bit D latch with asynchronous preset dominant over asynchronous clear.
LD58:	8-bit D latch with asynchronous preset dominant over asynchronous clear.

Availability:

LD51, LD54, and LD58 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

LD54



Type: Hard

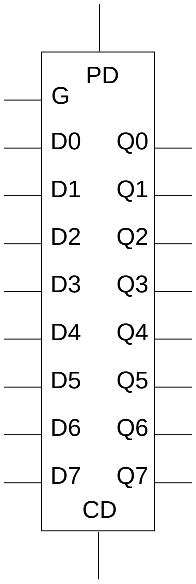
Logic Resources:

Macro	PT	GLB	Output	Level
LD51	4	1	1	1
LD54	4/out	2	4	1
LD58	4/out	2	8	1

Macro Port Definition:

```
LD51 (Q0,D0,G,PD,CD);
LD54 ([Q0..Q3],[D0..D3],G,PD,CD);
LD58 ([Q0..Q7],[D0..D7],G,PD,CD);
```

LD58



Truth Table:

Input				Output
PD	**CD**	**D0~D$_{n-1}$**	**G**	**Q0~Q$_{n-1}$**
1	x	x	x	1
0	1	x	x	0
0	0	d	1	d
0	0	x	0	Q0’~Qn’

d = any pattern of 1s and 0s on an input or set of inputs,
Q0’~Qn’ = previous output of flip-flop or latch, x = don’t care.

LD61, LD64, and LD68

Function:

LD61: 1-bit D latch with scan.
LD64: 4-bit D latch with scan.
LD68: 8-bit D latch with scan.

Availability:

LD61, LD64, and LD68 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Soft

Macro Port Definition:

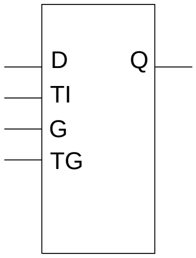
```
LD61 (Q0,D0,TI0,G,TG);
LD64 ([Q0..Q3],[D0..D3],[TI0..TI3],G,TG);
LD68 ([Q0..Q7],[D0..D7],[TI0..TI7],G,TG);
```

Truth Table:

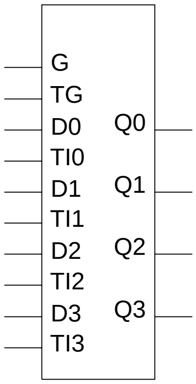
Input				Output
$D0\sim D_{n-1}$	**G**	**$TI0\sim TI_{n-1}$**	**TG**	**$Q0\sim Q_{n-1}$**
x	0	x	0	Q0'~Qn'
x	0	d	1	d
d	1	x	0	d
1	1	x	1	1*
x	1	1	1	1*
0	1	0	1	0*

* In proper operation, G and TG should NOT both be 1 at the same time.
d = any pattern of 1s and 0s on an input or set of inputs,
Q0'~Qn' = previous output of flip-flop or latch, x = don't care.

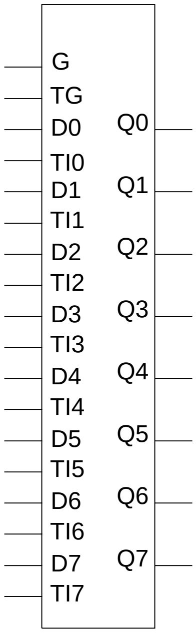
FD61



FD64



FD68



LD71, LD74, and LD78

Function:

LD71: 1-bit D latch with scan and asynchronous clear.
LD74: 4-bit D latch with scan and asynchronous clear.
LD78: 8-bit D latch with scan and asynchronous clear.

Availability:

LD71, LD74, and LD78 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Soft

Macro Port Definition:

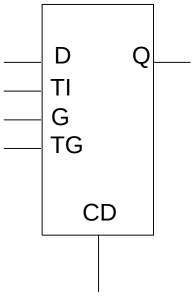
```
LD71 (Q0,D0,TI0,G,CD,TG);
LD74 ([Q0..Q3],[D0..D3],[TI0..TI3],G,CD,TG);
LD78 ([Q0..Q7],[D0..D7],[TI0..TI7],G,CD,TG);
```

Truth Table:

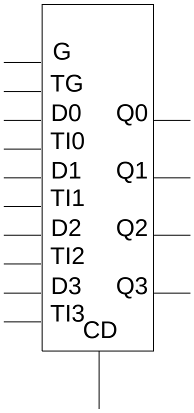
Input					Output
CD	**D0~D$_{n-1}$**	**G**	**TI0~TI$_{n-1}$**	**TG**	**Q0~Q$_{n-1}$**
1	x	x	x	x	0
0	x	0	x	0	Q0’~Qn’
0	x	0	d	1	d
0	d	1	x	0	d
0	1	1	x	1	1*
0	x	1	1	1	1*
0	0	1	0	1	0*

* In proper operation, G and TG should NOT both be 1 at the same time.
d = any pattern of 1s and 0s on an input or set of inputs,
Q0’~Qn’ = previous output of flip-flop or latch, x = don’t care.

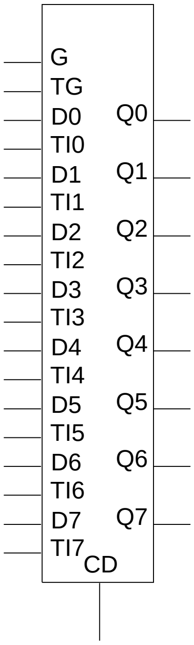
LD71



LD74



LD78



LD81, LD84, and LD88

Function:

LD81: 1-bit D latch with scan and asynchronous preset.
LD84: 4-bit D latch with scan and asynchronous preset.
LD88: 8-bit D latch with scan and asynchronous preset.

Availability:

LD81, LD84, and LD88 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Soft

Macro Port Definition:

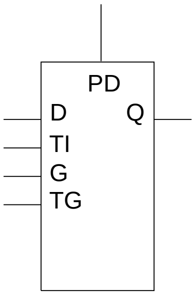
```
LD81 (Q0,D0,TI0,G,PD,TG);
LD84 ([Q0..Q3],[D0..D3],[TI0..TI3],G,PD,TG);
LD88 ([Q0..Q7],[D0..D7],[TI0..TI7],G,PD,TG);
```

Truth Table:

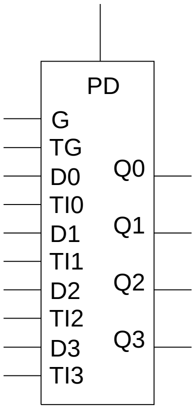
Input					Output
PD	**D0~D_{n-1}**	**G**	**TI0~TI_{n-1}**	**TG**	**Q0~Q_{n-1}**
1	x	x	x	x	1
0	x	0	x	0	Q0'~Qn'
0	x	0	d	1	d
0	d	1	x	0	d
0	1	1	x	1	1*
0	x	1	1	1	1*
0	0	1	0	1	0*

* In proper operation, G and TG should NOT both be 1 at the same time.
d = any pattern of 1s and 0s on an input or set of inputs,
Q0'~Qn' = previous output of flip-flop or latch, x = don't care.

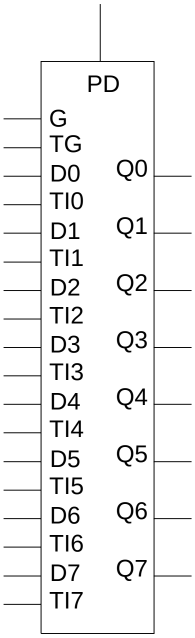
LD81



LD84



LD88



LD91, LD94, and LD98

Function:

LD91:	1-bit D latch with scan and asynchronous clear dominant over asynchronous preset.
LD94:	4-bit D latch with scan and asynchronous clear dominant over asynchronous preset.
LD98:	8-bit D latch with scan and asynchronous clear dominant over asynchronous preset.

Availability:

LD91, LD94, and LD98 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Soft

Macro Port Definition:

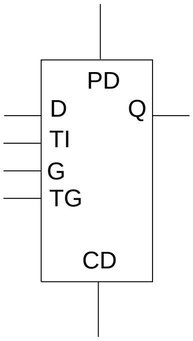
```
LD91 (Q0,D0,TI0,G,PD,CD,TG);
LD94 ([Q0..Q3],[D0..D3],[TI0..TI3],G,PD,CD,TG);
LD98 ([Q0..Q7],[D0..D7],[TI0..TI7],G,PD,CD,T
```

Truth Table:

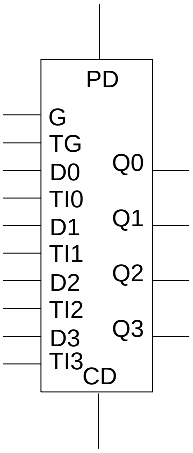
Input						Output
CD	**PD**	**D0~D$_{n-1}$**	**G**	**TI0~TI$_{n-1}$**	**TG**	**Q0~Q$_{n-1}$**
1	x	x	x	x	x	0
0	1	x	x	x	x	1
0	0	x	0	x	0	Q0’~Qn’
0	0	x	0	d	1	d
0	0	d	1	x	0	d
0	0	1	1	x	1	1*
0	0	x	1	1	1	1*
0	0	0	1	0	1	0*

* In proper operation, G and TG should NOT both be 1 at the same time.
d = any pattern of 1s and 0s on an input or set of inputs,
Q0’~Qn’ = previous output of flip-flop or latch, x = don’t care.

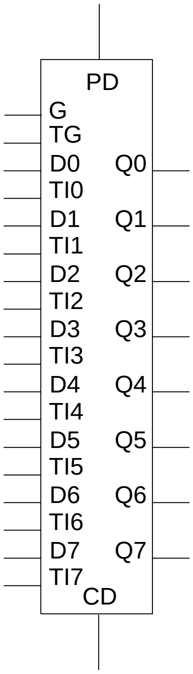
LD91



LD94



LD98



LDA1, LDA4, and LDA8

Function:

LDA1:	1-bit D latch with scan and asynchronous preset dominant over asynchronous clear.
LDA4:	4-bit D latch with scan and asynchronous preset dominant over asynchronous clear.
LDA8:	8-bit D latch with scan and asynchronous preset dominant over asynchronous clear.

Availability:

LDA1, LDA4, and LDA8 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Soft

Macro Port Definition:

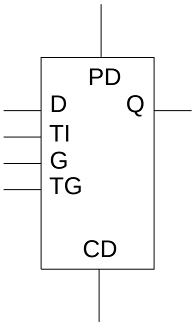
```
LDA1 (Q0,D0,TI0,G,PD,CD,TG);
LDA4 ([Q0..Q3],[D0..D3],[TI0..TI3],G,PD,CD,TG);
LDA8 ([Q0..Q7],[D0..D7],[TI0..TI7],G,PD,CD,TG);
```

Truth Table:

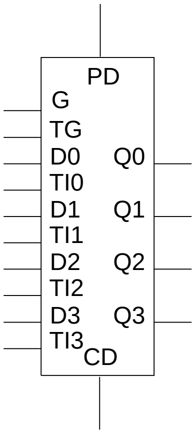
Input						Output
PD	**CD**	**D0~D$_{n-1}$**	**G**	**TI0~TI$_{n-1}$**	**TG**	**Q0~Q$_{n-1}$**
1	x	x	x	x	x	1
0	1	x	x	x	x	0
0	0	x	0	x	0	Q0'~Qn'
0	0	x	0	d	1	d
0	0	d	1	x	0	d
0	0	1	1	x	1	1*
0	0	x	1	1	1	1*
0	0	0	1	0	1	0*

* In proper operation, G and TG should NOT both be 1 at the same time.
d = any pattern of 1s and 0s on an input or set of inputs,
Q0'~Qn' = previous output of flip-flop or latch, x = don't care.

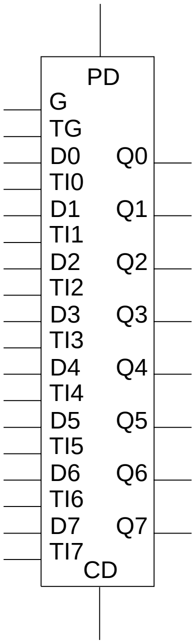
LDA1



LDA4



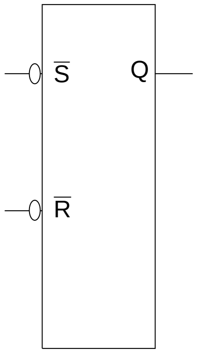
LDA8



SR Latches

LSR1 and LSR2

LSR1



Function:

LSR1: Simple $\overline{SR}$ latch.
LSR2: SR latch with OR on S and R inputs.

Availability:

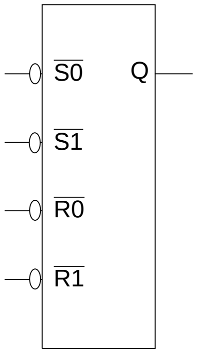
Both LSR1 and LSR2 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Type: Soft

Macro Port Definition:

```
LSR1 (Q0,S0,R0);
LSR2 (Q0,S0,S1,R0,R1);
```

LSR2



Truth Tables:

LSR1

Input		Output
S0	**R0**	**Q0**
1	1	Q0
0	1	1
1	0	0
0	0	1*

LSR2

Input		Output
S**	**R****	**Q0**
1	1	Q0
0	1	1
1	0	0
0	0	1*

* These outputs are not entirely stable. They may not remain when both S and R return to 1.

** S = 1 when S0 or S1 = 1. S = 0 when S0 and S1 = 0.
R = 1 when R0 or R1 = 1. R=0 when R0 and R1 = 0.
Q0 = output of flip-flop or latch.

Shift Registers

SRR11, SRR14, and SRR18

Function:

SRR11: 1-bit right shift register with asynchronous reset.
SRR14: 4-bit right shift register with asynchronous reset.
SRR18: 8-bit right shift register with asynchronous reset.

Availability:

SRR11, SRR14, and SRR18 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Schematics appear on the following pages.

Type: Soft

Macro Port Definition:

```
SRR11 (Q0,CAI,CLK,CD);
SRR14 ([Q0..Q3],CAI,CLK,CD);
SRR18 ([Q0..Q7],CAI,CLK,CD);
  SRR18_1 ([Q0..Q3],CAI,CLK,CD);
  SRR18_2 ([Q4..Q7],Q3,CLK,CD);
```

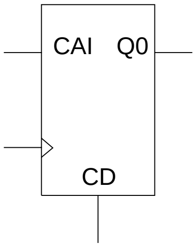
Truth Table:

The SRR11 has only Q0 as an output. The SRR14 has Q0 to Q3. The SRR18 has Q0 to Q7.

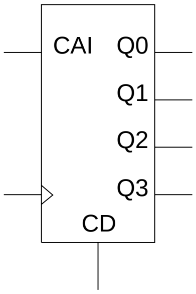
Input			Output							
CD	**CAI**	**CLK**	**Q0**	**Q1**	**Q2**	**Q3**	**Q4**	**Q5**	**Q6**	**Q7**
1	x	x	0	0	0	0	0	0	0	0
0	d	↑	d	Q0’	Q1’	Q2’	Q3’	Q4’	Q5’	Q6’
0	x	0	Q0’	Q1’	Q2’	Q3’	Q4’	Q5’	Q6’	Q7’
0	x	1	Q0’	Q1’	Q2’	Q3’	Q4’	Q5’	Q6’	Q7’

d = any pattern of 1s and 0s on an input or set of inputs,
Q0’ = previous output of flip-flop or latch, x = don’t care,
↑ = rising clock edge.

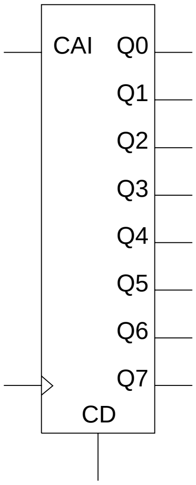
SRR11



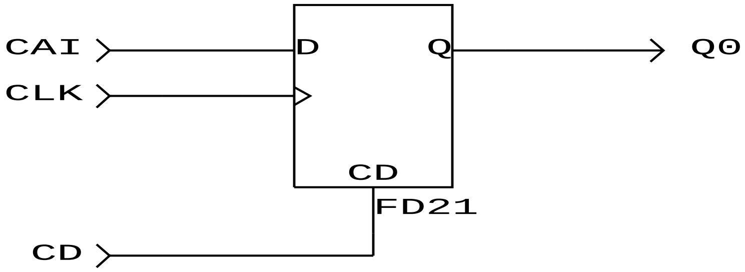
SRR14



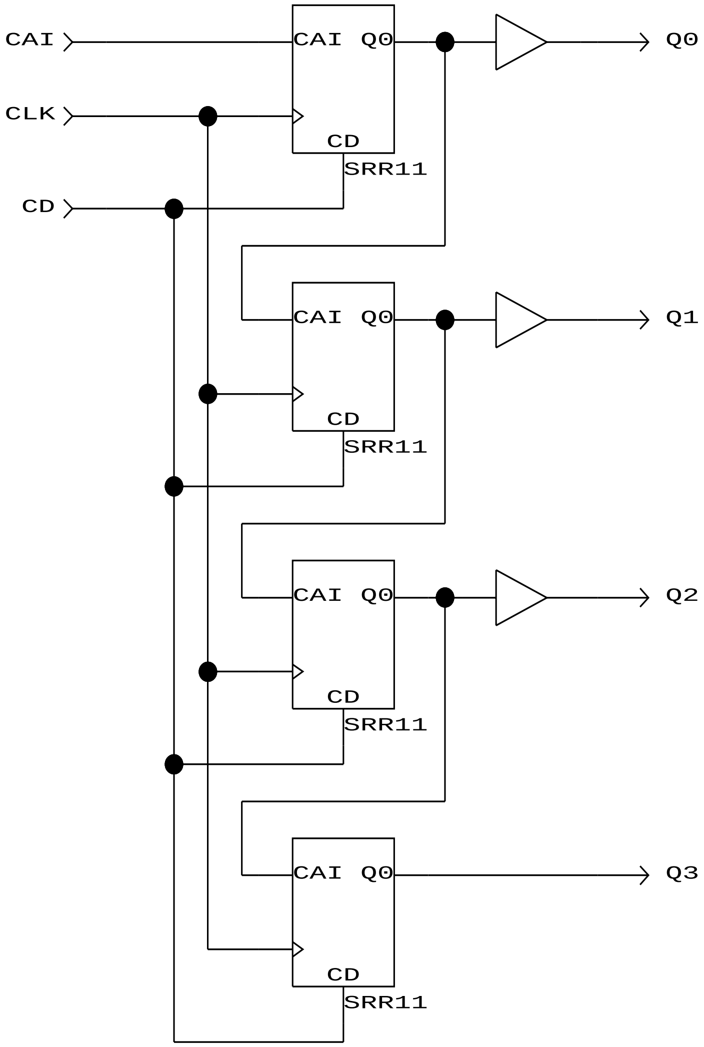
SRR18



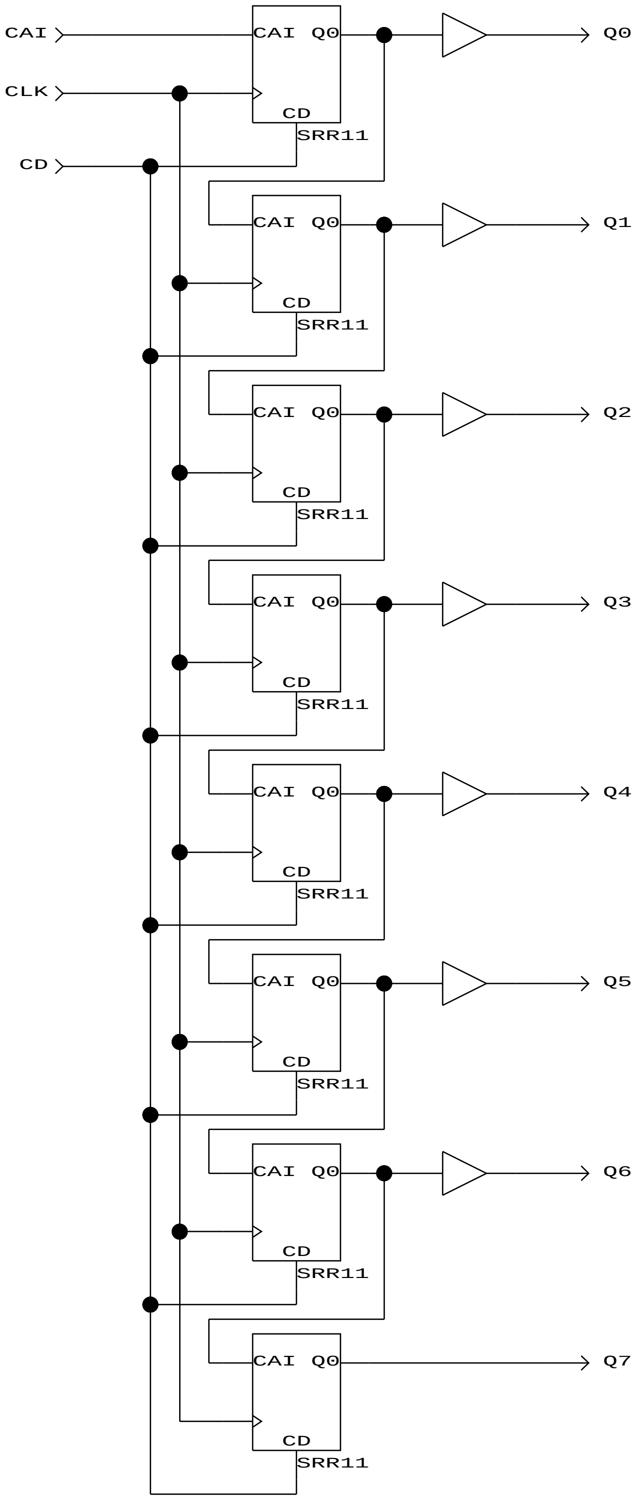
SRR11



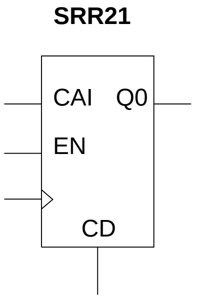
SRR14


CAI
CLK
CD
CAI Q0
CD
SRR11
Q0
CAI Q0
CD
SRR11
Q1
CAI Q0
CD
SRR11
Q2
CAI Q0
CD
SRR11
Q3

SRR11



SRR21, SRR24, and SRR28



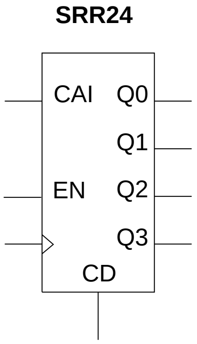
Function:

SRR21: 1-bit right shift register with asynchronous reset and enable.
SRR24: 4-bit right shift register with asynchronous reset and enable.
SRR28: 8-bit right shift register with asynchronous reset and enable.

Availability:

SRR21, SRR24, and SRR28 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

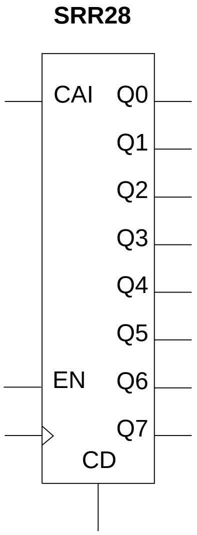
Schematics appear on the following pages.



Type: Soft

Macro Port Definition:

```
SRR21 (Q0,CAI,CLK,EN,CD);
SRR24 ([Q0..Q3],CAI,CLK,EN,CD);
SRR28 ([Q0..Q7],CAI,CLK,EN,CD);
  SRR28_1 ([Q0..Q3],CAI,CLK,EN,CD);
  SRR28_2 ([Q4..Q7],Q3,CLK,EN,CD);
```



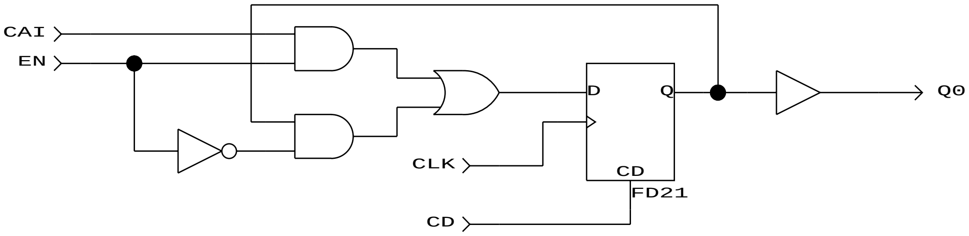
Truth Table:

The SRR21 has only Q0 as an output. The SRR24 has Q0 to Q3. The SRR28 has Q0 to Q7.

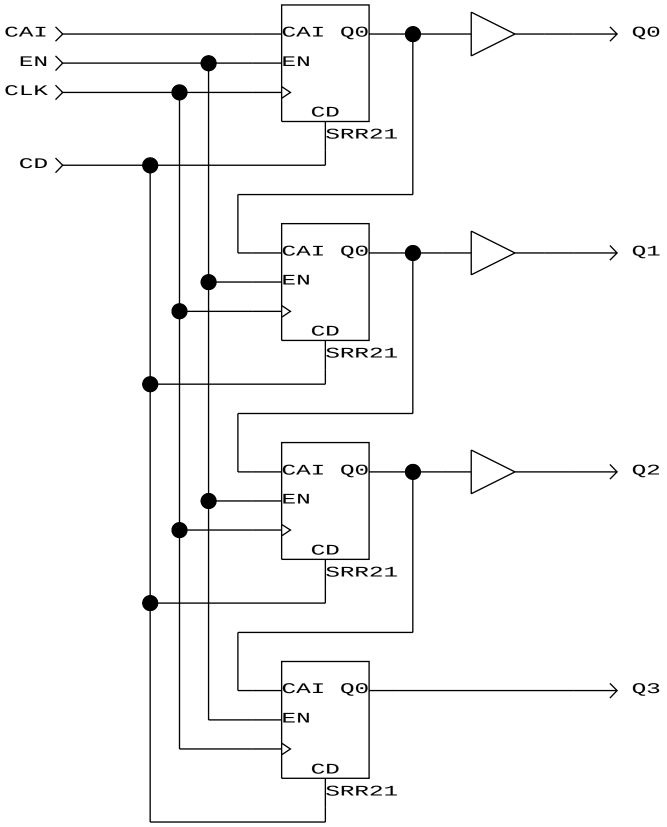
Input				Output							
CD	**EN**	**CAI**	**CLK**	**Q0**	**Q1**	**Q2**	**Q3**	**Q4**	**Q5**	**Q6**	**Q7**
1	x	x	x	0	0	0	0	0	0	0	0
0	1	d	↑	d	Q0’	Q1’	Q2’	Q3’	Q4’	Q5’	Q6’
0	0	x	↑	Q0’	Q1’	Q2’	Q3’	Q4’	Q5’	Q6’	Q7’
0	x	x	0	Q0’	Q1’	Q2’	Q3’	Q4’	Q5’	Q6’	Q7’
0	x	x	1	Q0’	Q1’	Q2’	Q3’	Q4’	Q5’	Q6’	Q7’

d = any pattern of 1s and 0s on an input or set of inputs,
Q0’ = previous output of flip-flop or latch, x = don’t care,
↑ = rising clock edge.

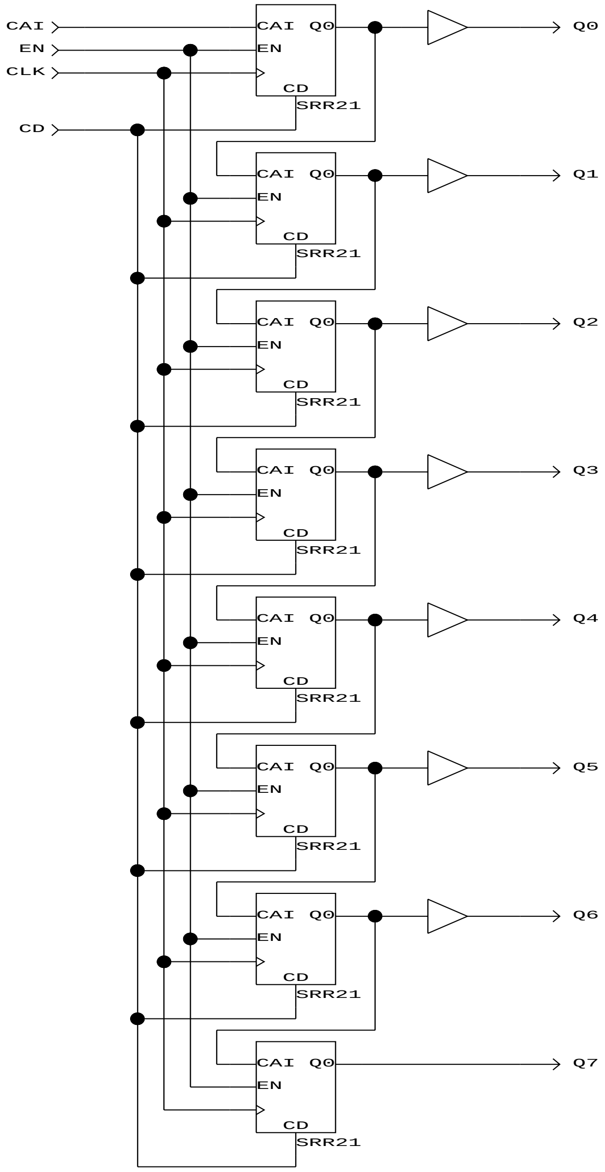
SRR21



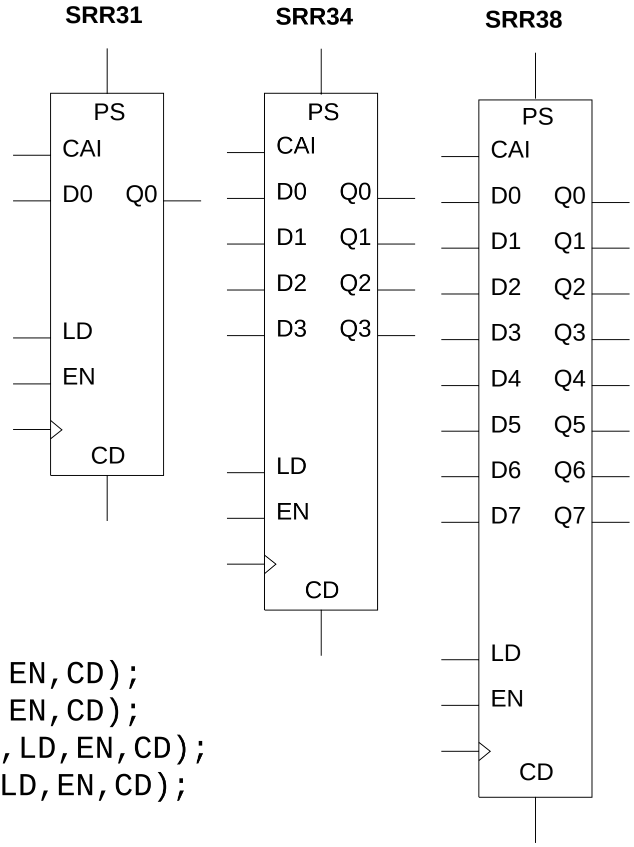
SRR24



SRR28



SRR31, SRR34, and SRR38



Function:

1-, 4-, and 8-bit right shift registers with asynchronous reset, enable, parallel data load, and synchronous preset.

Availability:

SRR31, SRR34, and SRR38 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Schematics appear on the following pages.

Type: Soft

Macro Port Definition:

```
SRR31 (Q0,D0,CAI,CLK,PS,LD,EN,CD);
SRR34 ([Q0..Q3],[D0..D3],CAI,CLK,PS,LD,EN,CD);
SRR38 ([Q0..Q7],[D0..D7],CAI,CLK,PS,LD,EN,CD);
  SRR38_1 ([Q0..Q3],[D0..D3],CAI,CLK,PS,LD,EN,CD);
  SRR38_2 ([Q4..Q7],[D4..D7],Q3,CLK,PS,LD,EN,CD);
```

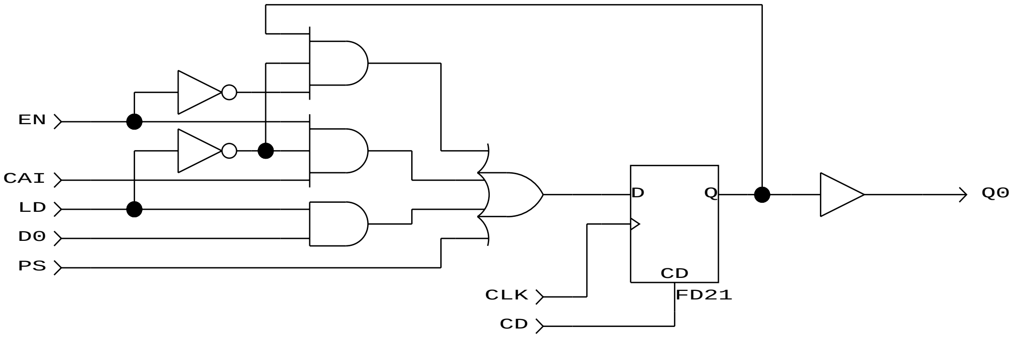
Truth Table:

The SRR31 has only Q0 as an output. The SRR34 has Q0 to Q3. The SRR38 has Q0 to Q7.

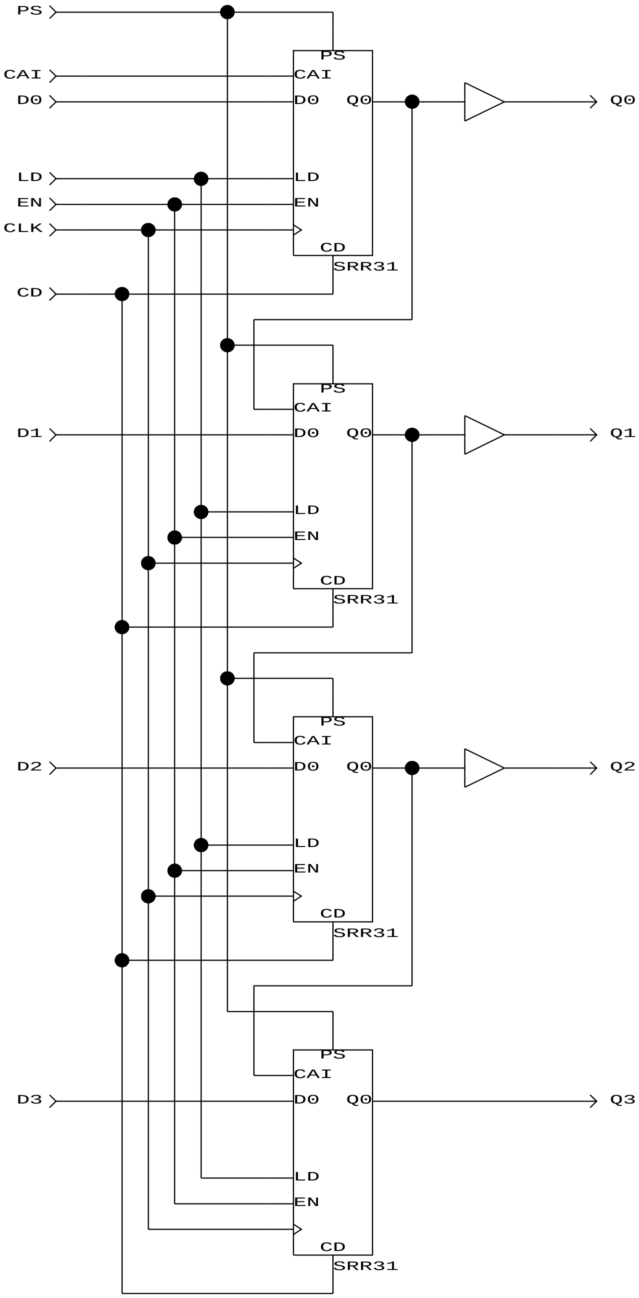
Input							**Output**					
CD	**PS**	**LD**	**D0~D7**	**EN**	**CAI**	**CLK**	**Q0**	**Q1**	**Q2**	**Q3**	**Q4**	**Q5**
1	x	x	x	x	x	x	0	0	0	0	0	0
0	1	x	x	x	x	↑	1	1	1	1	1	1
0	0	1	d	x	x	↑	D0	D1	D2	D3	D4	D5
0	0	0	x	1	d	↑	d	Q0’	Q1’	Q2’	Q3’	Q4’
0	0	0	x	0	x	↑	Q0’	Q1’	Q2’	Q3’	Q4’	Q5’
0	x	x	x	x	x	0	Q0’	Q1’	Q2’	Q3’	Q4’	Q5’
0	x	x	x	x	x	1	Q0’	Q1’	Q2’	Q3’	Q4’	Q5’

d = any pattern of 1s and 0s on an input or set of inputs,
D0..D_{n-1} = load inputs for counters and shift registers,
Q0’ = previous output of flip-flop or latch, x = don’t care,
↑ = rising clock edge.

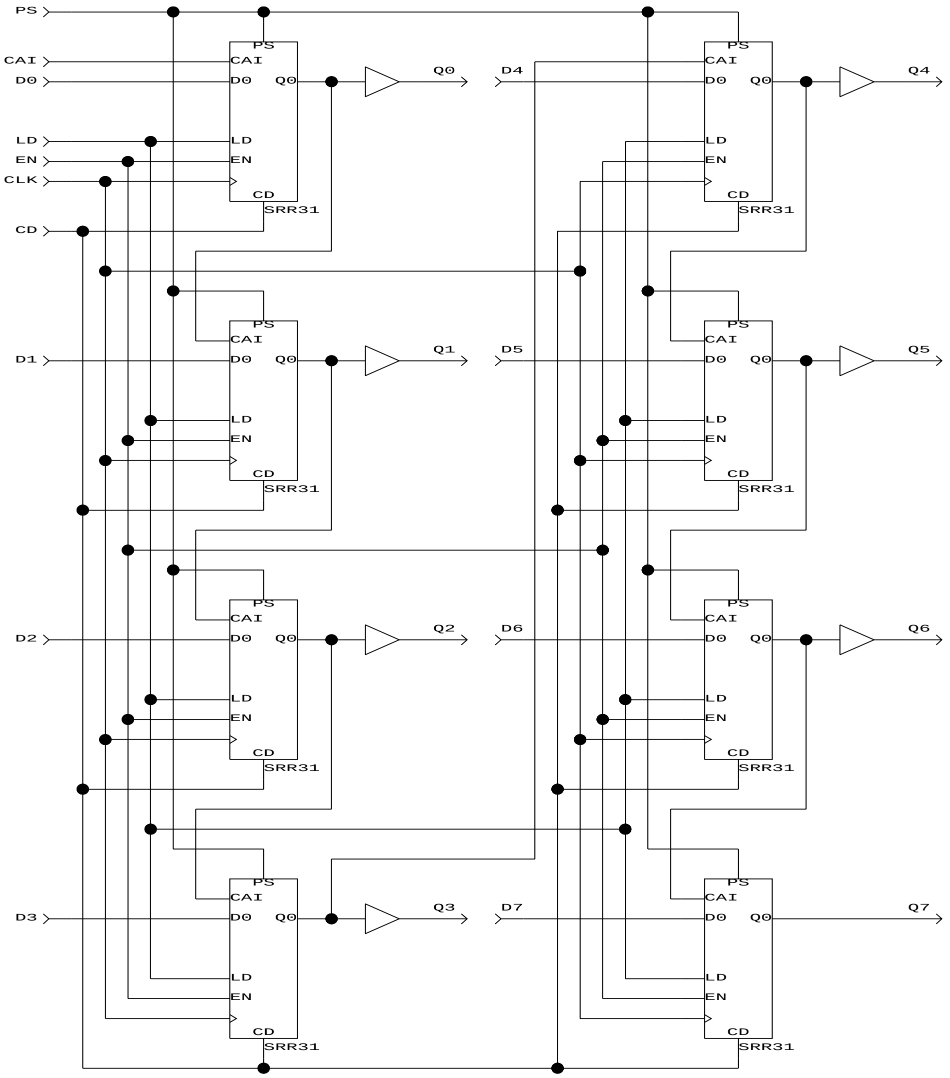
SRR31



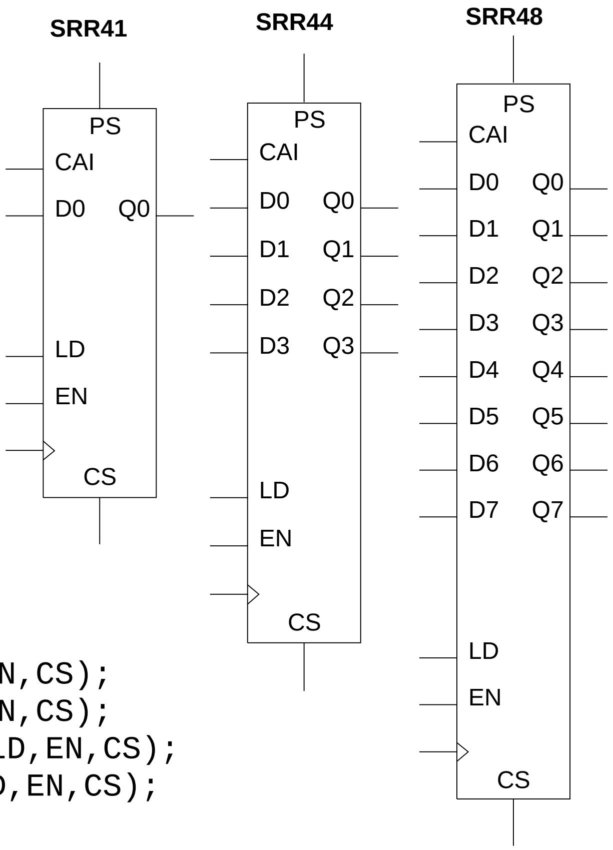
SRR34.


PS
CAI
D0
LD
EN
CLK
CD
D1
D2
D3
PS
CAI
D0
Q0
LD
EN
CD
SRR31
Q0
Q1
Q2
Q3

SRR38


PS
CAI
D0
LD
EN
CLK
CD
PS
CAI
D0
Q0
LD
EN
CD
SRR31
Q0
D4
PS
CAI
D0
Q0
LD
EN
CD
SRR31
Q4
D1
PS
CAI
D0
Q0
LD
EN
CD
SRR31
Q1
D5
PS
CAI
D0
Q0
LD
EN
CD
SRR31
Q5
D2
PS
CAI
D0
Q0
LD
EN
CD
SRR31
Q2
D6
PS
CAI
D0
Q0
LD
EN
CD
SRR31
Q6
D3
PS
CAI
D0
Q0
LD
EN
CD
SRR31
Q3
D7
PS
CAI
D0
Q0
LD
EN
CD
SRR31
Q7

SRR41, SRR44, and SRR48



Function:

1-, 4-, and 8-bit right shift registers with synchronous reset, enable, parallel data load, and synchronous preset.

Availability:

SRR41, SRR44, and SRR48 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

Schematics appear on the following pages.

Type: Soft

Macro Port Definition:

```
SRR41 (Q0,D0,CAI,CLK,PS,LD,EN,CS);
SRR44 ([Q0..Q3],[D0..D3],CAI,CLK,PS,LD,EN,CS);
SRR48 ([Q0..Q7],[D0..D7],CAI,CLK,PS,LD,EN,CS);
  SRR48_1 ([Q0..Q3],[D0..D3],CAI,CLK,PS,LD,EN,CS);
  SRR48_2 ([Q4..Q7],[D4..D7],Q3,CLK,PS,LD,EN,CS);
```

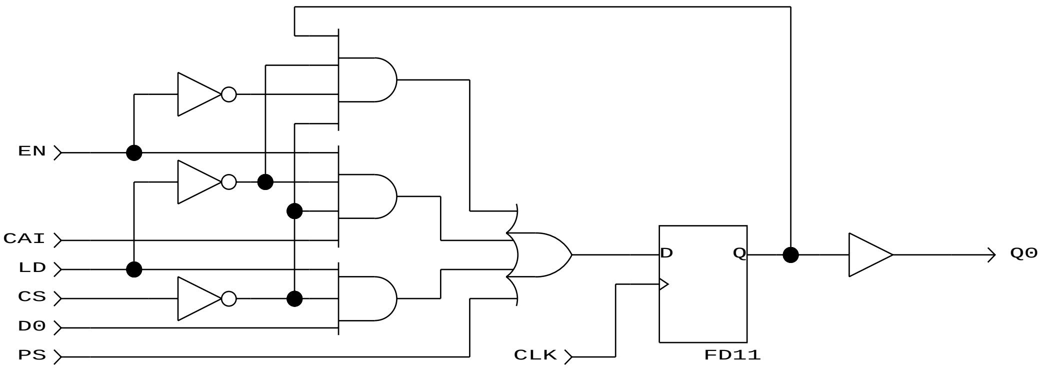
Truth Table:

The SRR41 has only Q0 as an output. The SRR44 has Q0 to Q3. The SRR48 has Q0 to Q7.

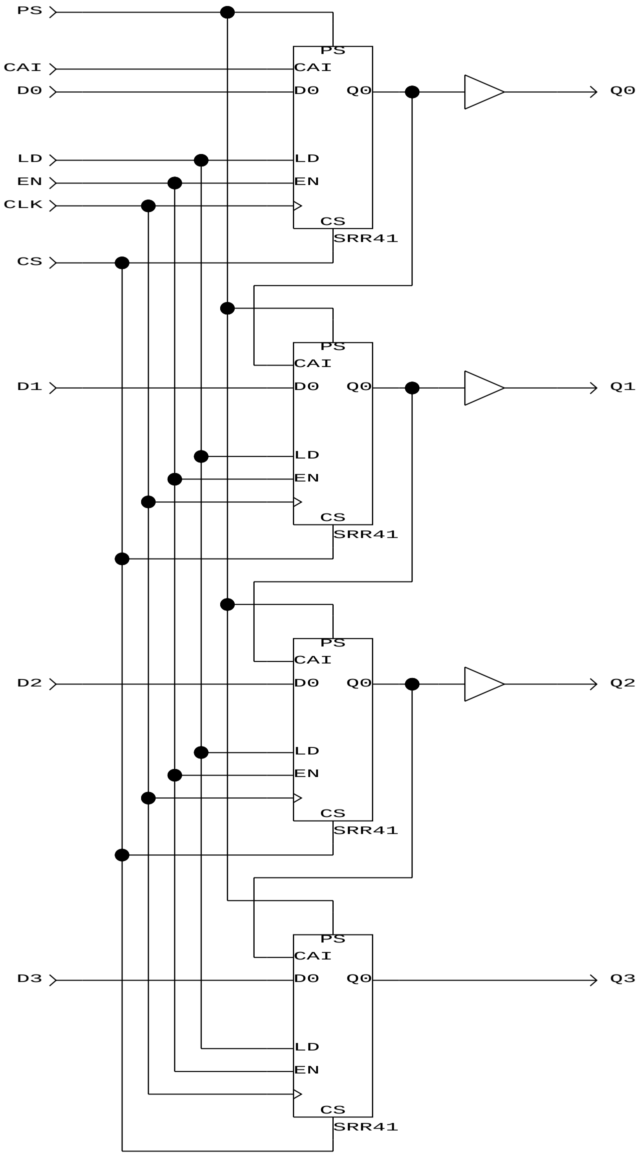
Input							Output						
PS	**CS**	**LD**	**D0~D7**	**EN**	**CAI**	**CLK**	**Q0**	**Q1**	**Q2**	**Q3**	**Q4**	**Q5**	**Q6**
1	x	x	x	x	x	↑	1	1	1	1	1	1	1
0	1	x	x	x	x	↑	0	0	0	0	0	0	0
0	0	1	d	x	x	↑	D0	D1	D2	D3	D4	D5	D6
0	0	0	x	1	d	↑	d	Q0’	Q1’	Q2’	Q3’	Q4’	Q5’
0	0	0	x	0	x	↑	Q0’	Q1’	Q2’	Q3’	Q4’	Q5’	Q6’
x	x	x	x	x	x	0	Q0’	Q1’	Q2’	Q3’	Q4’	Q5’	Q6’
x	x	x	x	x	x	1	Q0’	Q1’	Q2’	Q3’	Q4’	Q5’	Q6’

d = any pattern of 1s and 0s on an input or set of inputs,
D0..D_{n-1} = load inputs for shift registers,
Q0’ = previous output of flip-flop, x = don’t care,
↑ = rising clock edge.

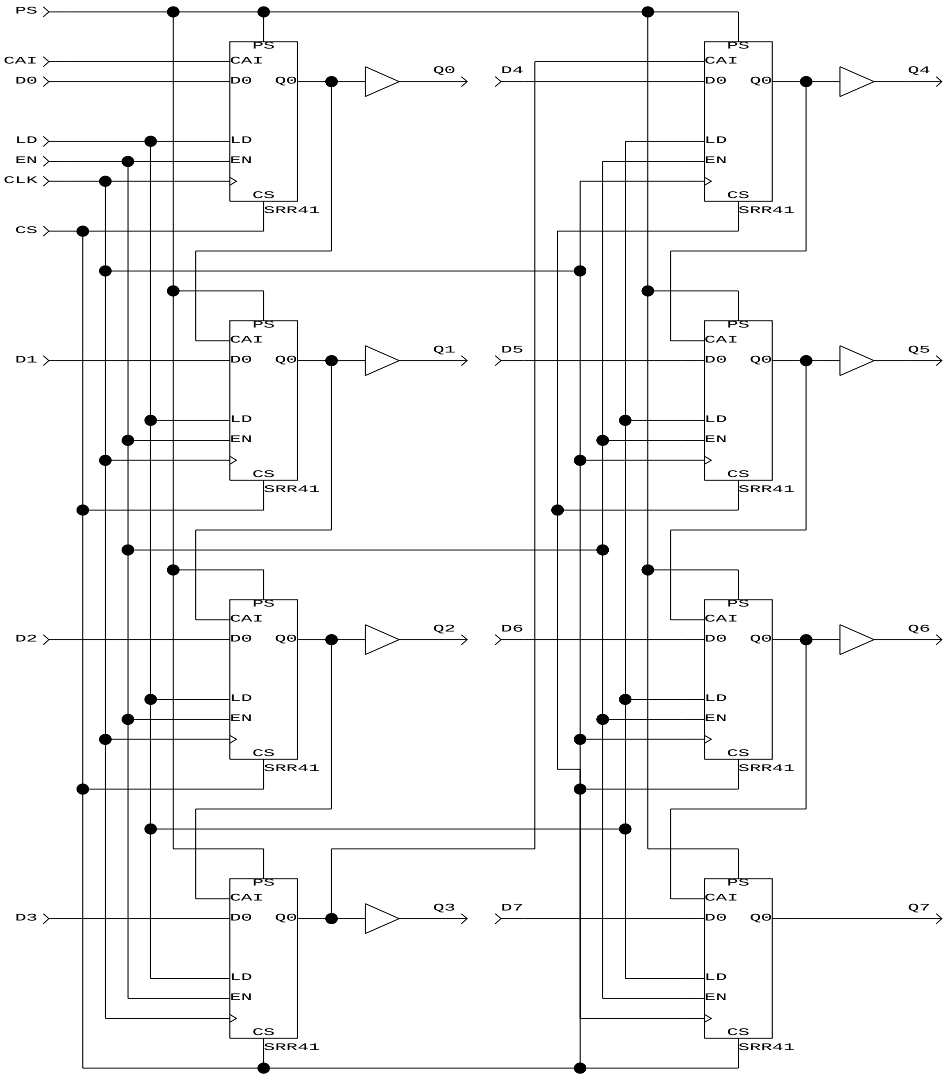
SRR41



SRR44

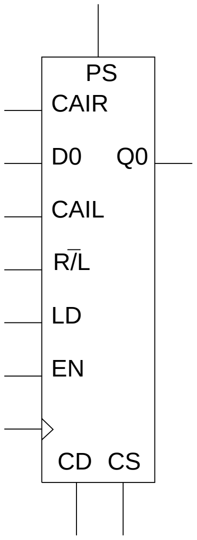

PS
CAI
D0
LD
EN
CLK
CS
D1
D2
D3
PS
CAI
D0
Q0
LD
EN
CS
SRR41
Q0
Q1
Q2
Q3

SRR48

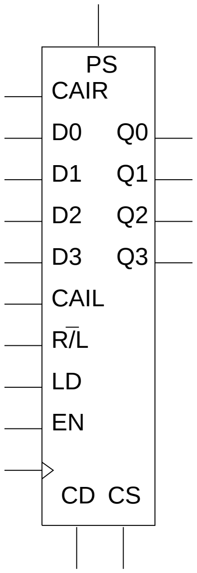

PS
CAI
D0
LD
EN
CLK
CS
D1
D2
D3
Q0
Q1
Q2
Q3
D4
D5
D6
D7
Q4
Q5
Q6
Q7
PS
CAI
D0
Q0
LD
EN
CS
SRR41

SRRL1, SRRL4, and SRRL8

SRRL1



SRRL4



Function:

1-, 4-, and 8-bit right/left shift registers with asynchronous reset, enable, parallel data load, synchronous preset, and synchronous reset.

Availability:

SRRL1, SRRL4, and SRRL8 can be used with 1000, 2000, 3000, 5000, and 8000 devices.

An additional symbol and schematics appear on the following pages.

Type: Soft

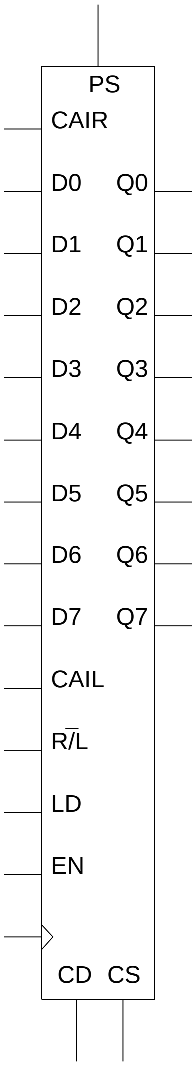
Macro Port Definition:

```
SRRL1 (Q0,D0,CAIR,CAIL,CLK,PS,LD,EN,RL,CD,CS);
SRRL4 ([Q0..Q3],[D0..D3],CAIR,CAIL,CLK,PS,LD,EN,RL,CD,CS);
  SRRL4_1 (Q0,Q1,D0,D1,CAIR,Q2,CLK,PS,LD,EN,RL,CD,CS);
  SRRL4_2 (Q2,Q3,D2,D3,Q1,CAIL,CLK,PS,LD,EN,RL,CD,CS);
SRRL8 ([Q0..Q7],[D0..D7],CAIR,CAIL,CLK,PS,LD,EN,RL,CD,CS);
  SRRL8_1 ([Q0..Q2],[D0..D2],CAIR,Q3,CLK,PS,LD,EN,RL,CD,CS);
  SRRL8_2 ([Q3..Q5],[D3..D5],Q2,Q6,CLK,PS,LD,EN,RL,CD,CS);
  SRRL8_3 (Q6,Q7,D6,D7,Q5,CAIL,CLK,PS,LD,EN,RL,CD,CS);
```

Truth Table:

The SRRL1 has only Q0 as an output. The SRRL4 has Q0 to Q3.
The SRRL8 has Q0 to Q7.

SRRL8

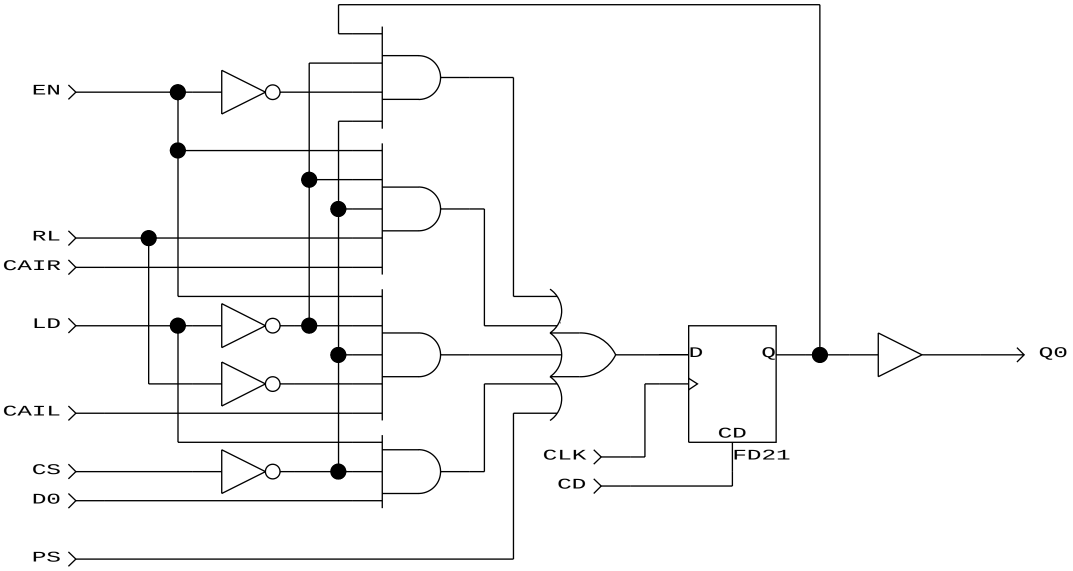


Input									
CD	**PS**	**CS**	**LD**	**D0~D7**	**RL**	**EN**	**CAIR**	**CAIL**	**CLK**
1	x	x	x	x	x	x	x	x	x
0	1	x	x	x	x	x	x	x	↑
0	0	1	x	x	x	x	x	x	↑
0	0	0	1	d	x	x	x	x	↑
0	0	0	0	x	0	1	x	d	↑
0	0	0	0	x	1	1	d	x	↑
0	0	0	0	x	x	0	x	x	↑
0	x	x	x	x	x	x	x	x	0
0	x	x	x	x	x	x	x	x	1

Output							
Q0	**Q1**	**Q2**	**Q3**	**Q4**	**Q5**	**Q6**	**Q7**
0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	1
0	0	0	0	0	0	0	0
D0	D1	D2	D3	D4	D5	D6	D7
Q1	Q2	Q3	Q4	Q5	Q6	Q7	CAIL
CAIR	Q0	Q1	Q2	Q3	Q4	Q5	Q6
Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7
Q0	Q1	Q2	Q3	Q4	Q5	Q6	Q7

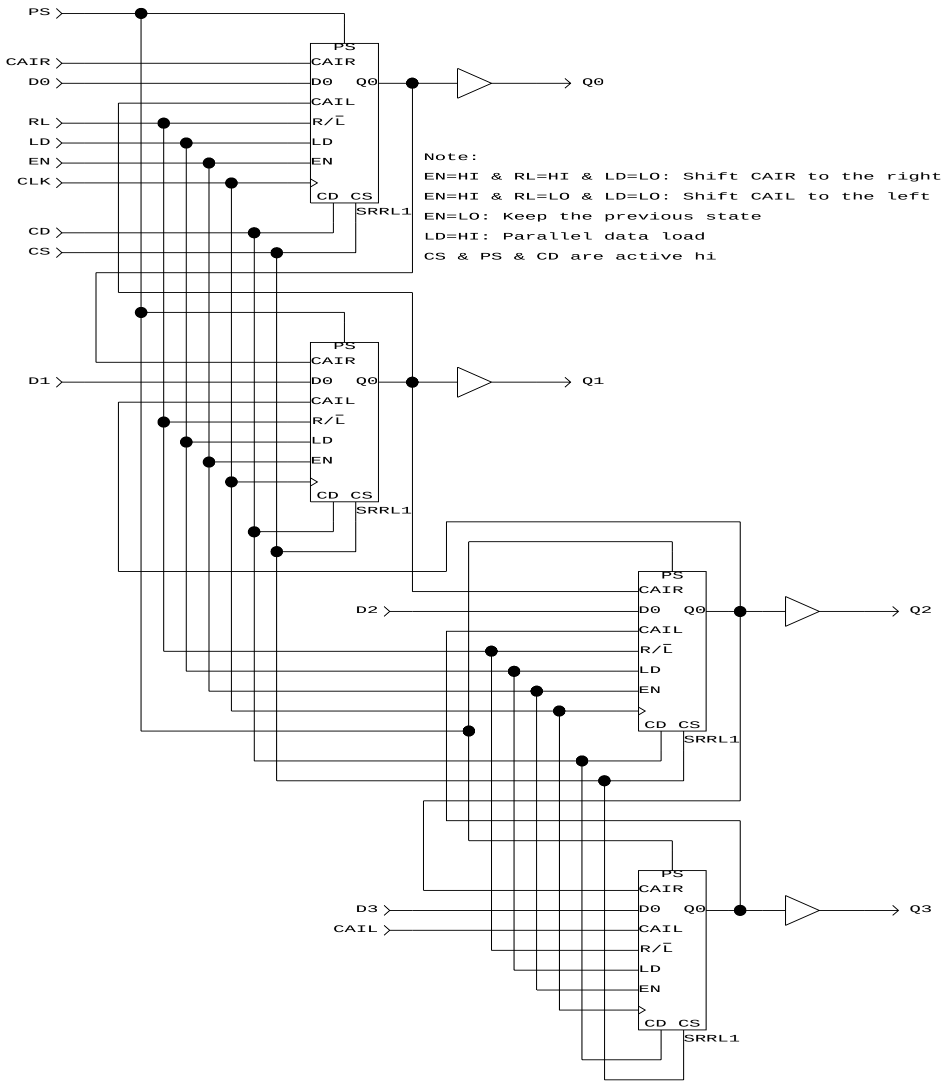
CAIL = shift left serial input, CAIR = shift right serial input,
d = any pattern of 1s and 0s on an input or set of inputs,
D0..D$_{n-1}$ = input to D or T flip-flop/latch; load inputs for counters and shift registers,
Q0’ = previous output of flip-flop or latch, x = don’t care, ↑ = rising clock edge.

SRRL1



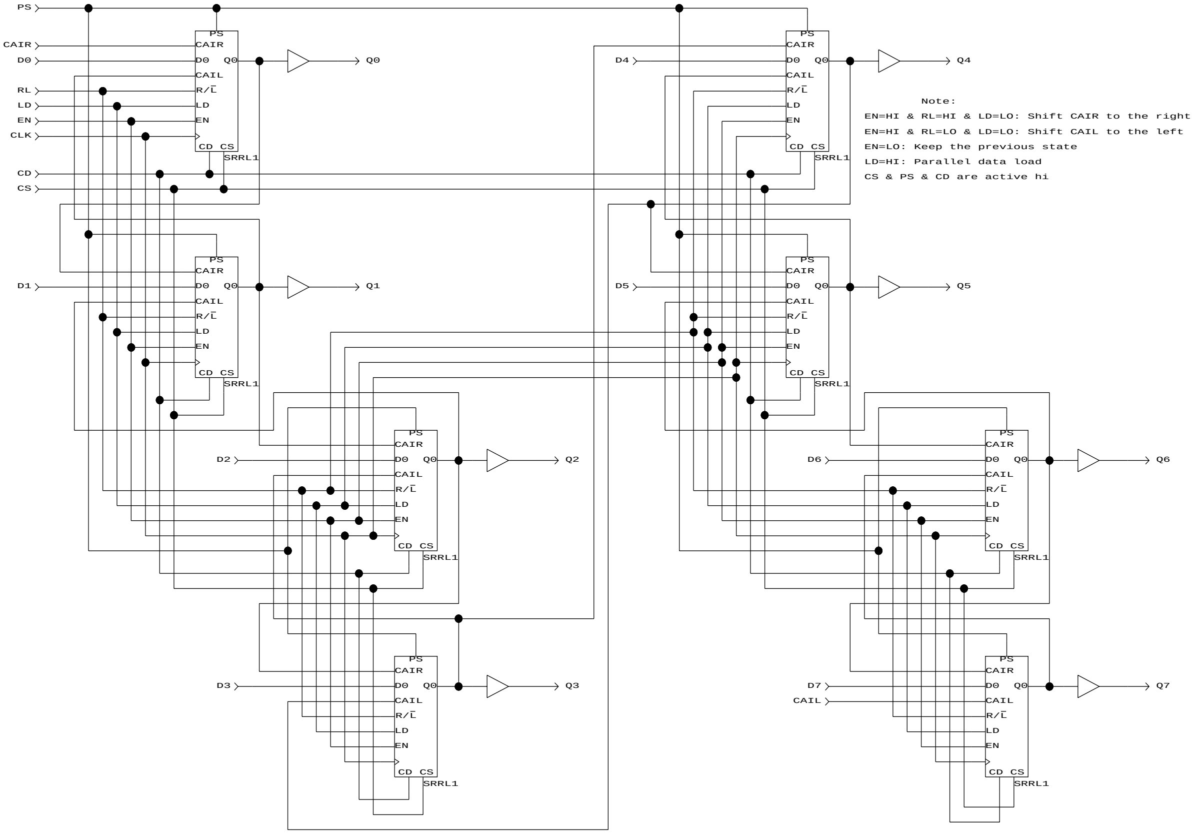
```
Note:
 . EN=HI & RL=HI & LD=LO : Shift CAIR to the right
 . EN=HI & RL=LO & LD=LO : Shift CAIL to the left
 . EN=LO : Keep the previous state
 . LD=HI : Parallel data load
 . CS & PS & CD are active hi
```

SRRL4



Note:
EN=HI & RL=HI & LD=LO: Shift CAIR to the right
EN=HI & RL=LO & LD=LO: Shift CAIL to the left
EN=LO: Keep the previous state
LD=HI: Parallel data load
CS & PS & CD are active hi

SRRL8



Note:
EN=HI & RL=HI & LD=LO: Shift CAIR to the right
EN=HI & RL=LO & LD=LO: Shift CAIL to the left
EN=LO: Keep the previous state
LD=HI: Parallel data load
CS & PS & CD are active hi

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