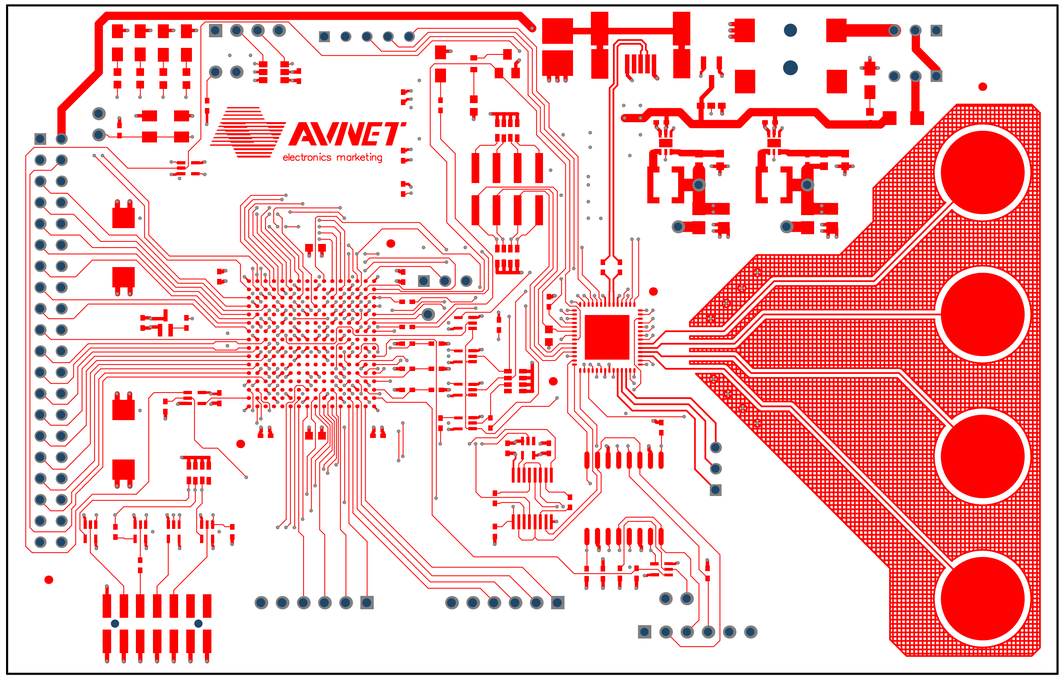
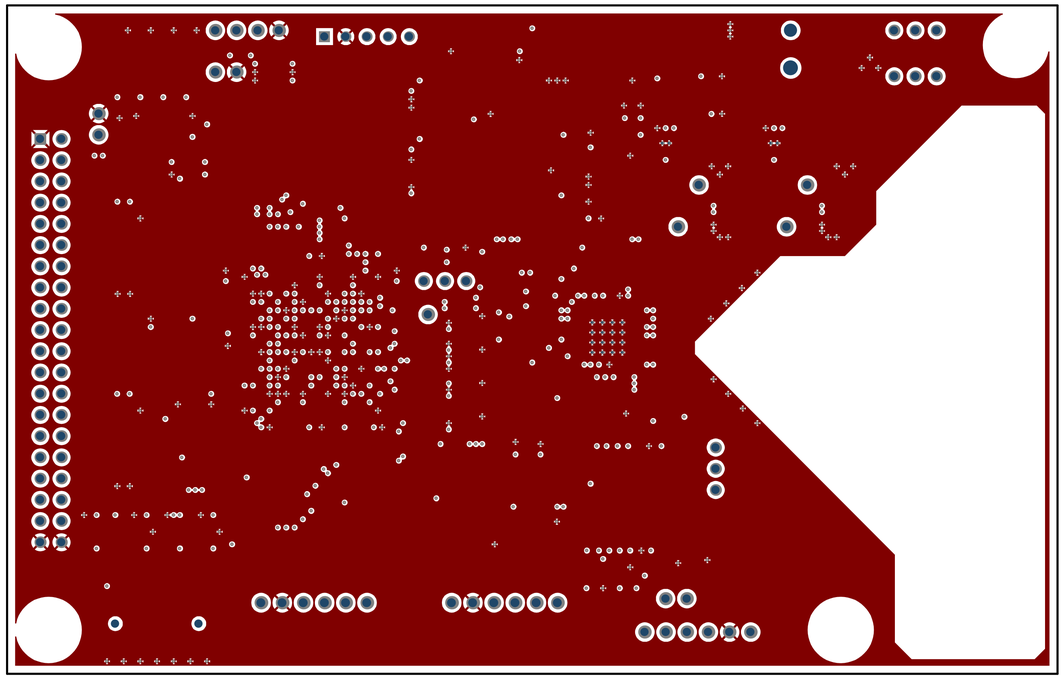
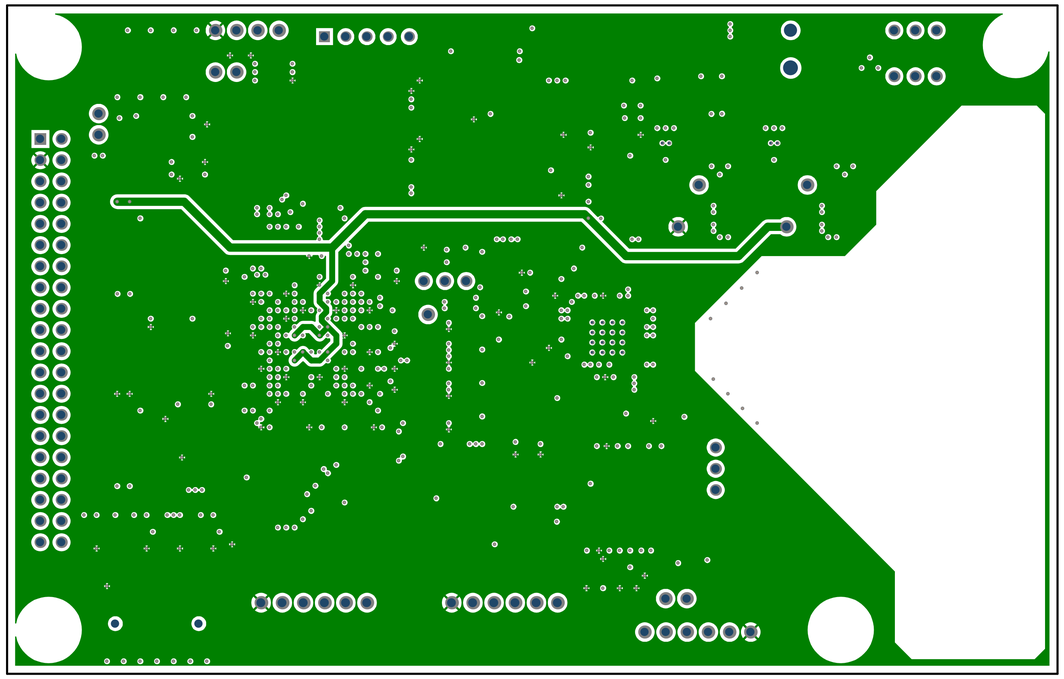


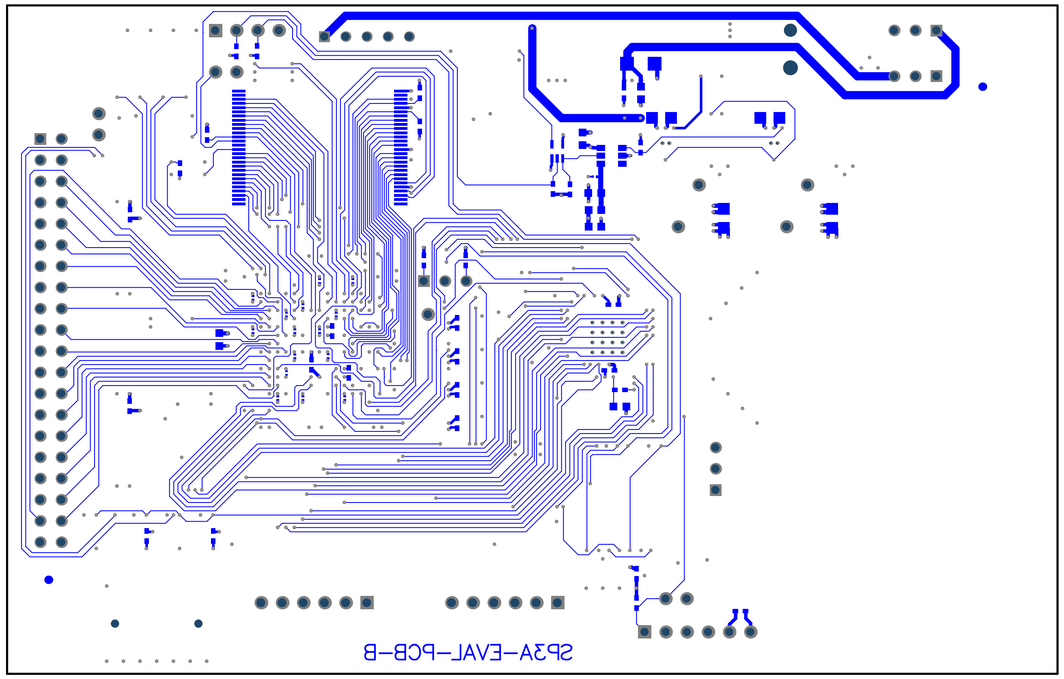
AES	CUSTOMER: AVNET ELECTRONICS MARKETING	DATE: 6/9/2008	
	TITLE: SPARTAN 3A EVALUATION BOARD	REV: B	
	LEVEL: PRIMARY COMPONENT – LAYER 1		



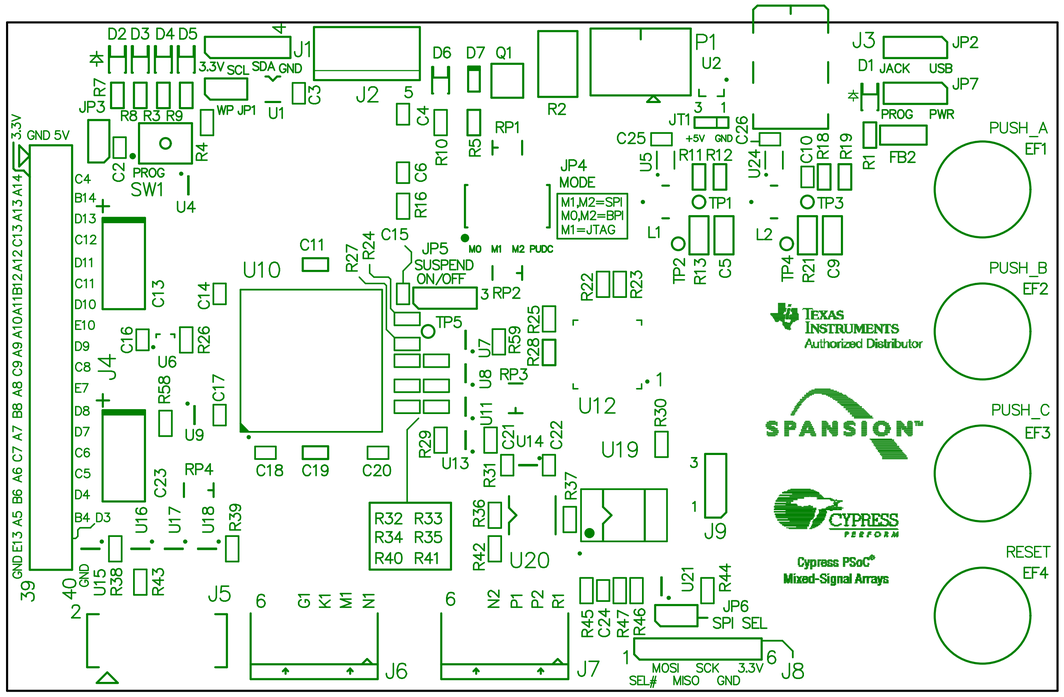
AES	CUSTOMER: AVNET ELECTRONICS MARKETING	DATE: 6/9/2008	
	TITLE: SPARTAN 3A EVALUATION BOARD	REV: B	
	LEVEL: GND PLANE – LAYER 2		



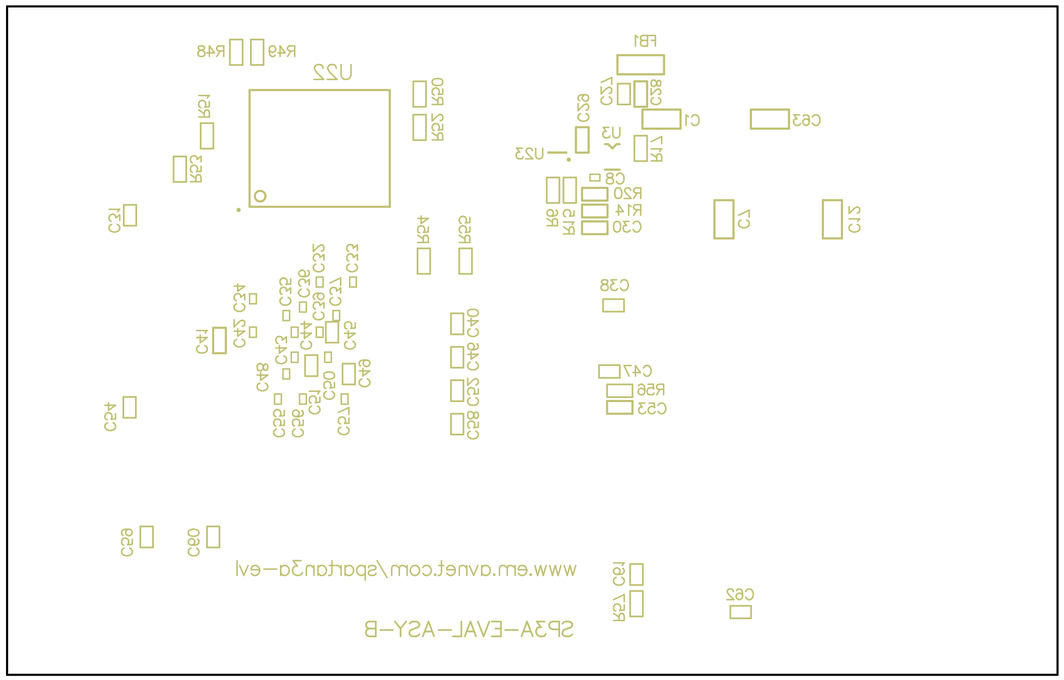
AES	CUSTOMER: AVNET ELECTRONICS MARKETING	DATE: 6/9/2008	
	TITLE: SPARTAN 3A EVALUATION BOARD	REV: B	
	LEVEL: PWR PLANE – LAYER 3		



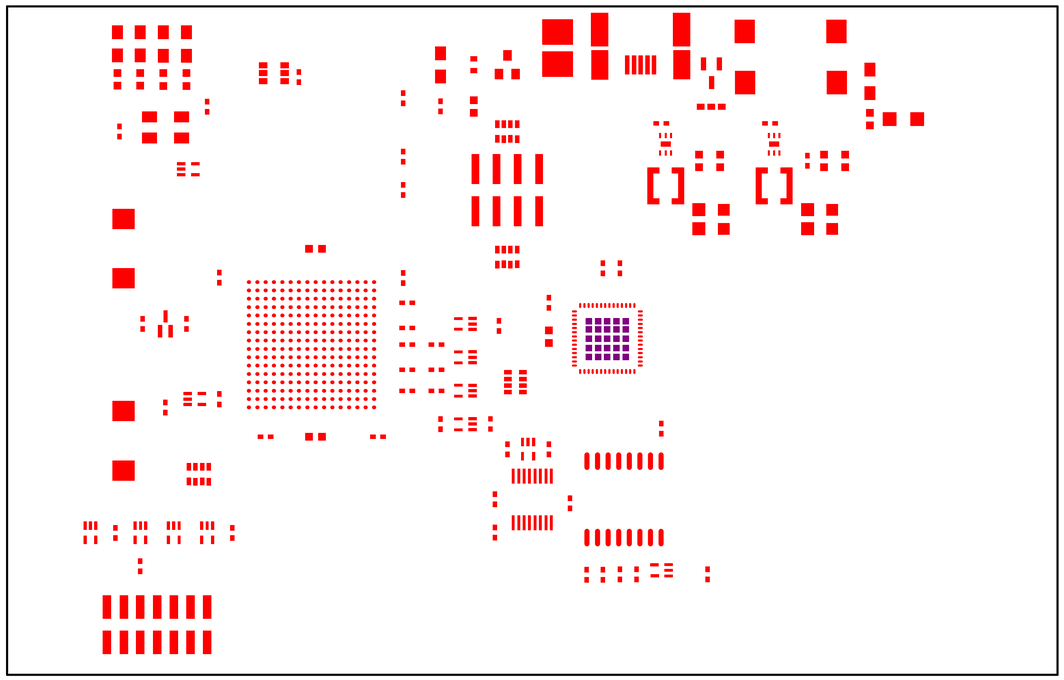
AES	CUSTOMER: AVNET ELECTRONICS MARKETING	DATE: 6/9/2008	
	TITLE: SPARTAN 3A EVALUATION BOARD	REV: B	
	LEVEL: SECONDARY COMPONENT – LAYER 4		



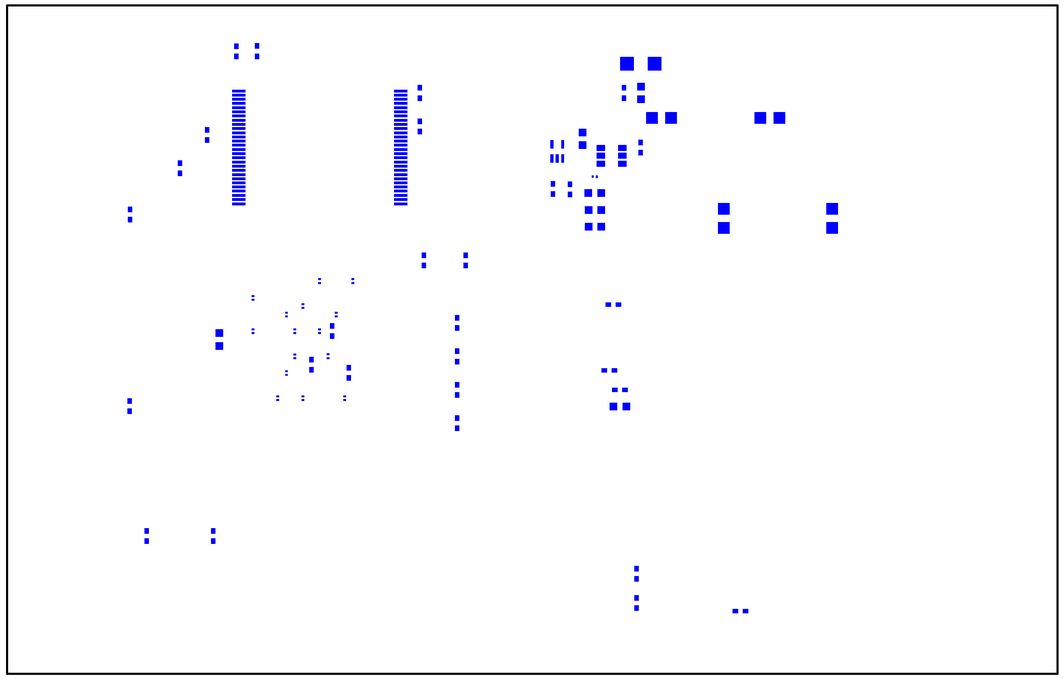
AES	CUSTOMER: AVNET ELECTRONICS MARKETING	DATE: 6/9/2008
	TITLE: SPARTAN 3A EVALUATION BOARD	REV: B
	LEVEL: PRIMARY SILKSCREEN	



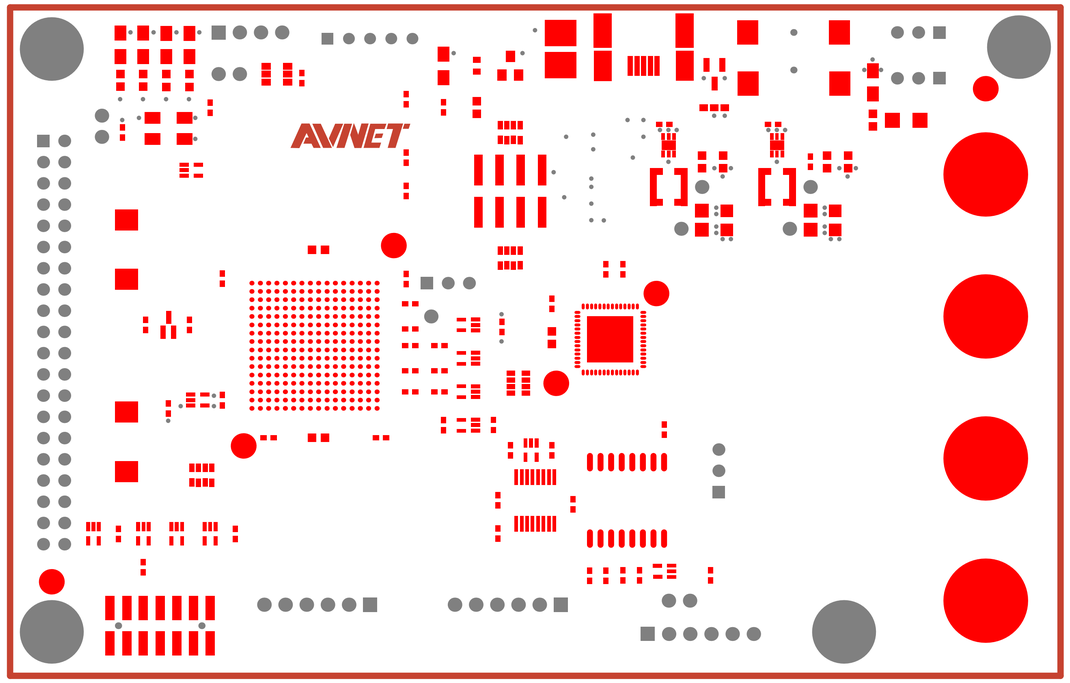
AES	CUSTOMER: AVNET ELECTRONICS MARKETING	DATE: 6/9/2008	
	TITLE: SPARTAN 3A EVALUATION BOARD	REV: B	
	LEVEL: SECONDARY SILKSCREEN		



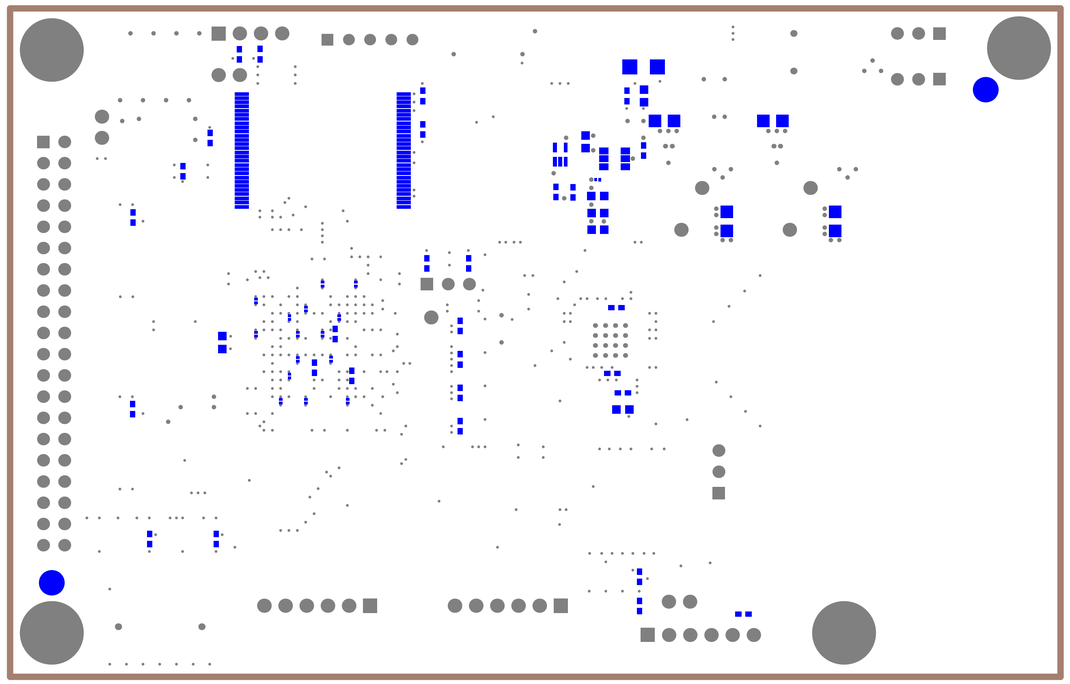
AES	CUSTOMER: AVNET ELECTRONICS MARKETING	DATE: 6/9/2008
	TITLE: SPARTAN 3A EVALUATION BOARD	REV: B
	LEVEL: PRIMARY SOLDER PASTE	



AES	CUSTOMER: AVNET ELECTRONICS MARKETING	DATE: 6/9/2008	
	TITLE: SPARTAN 3A EVALUATION BOARD	REV: B	
	LEVEL: SECONDARY SOLDER PASTE		



AES	CUSTOMER: AVNET ELECTRONICS MARKETING	DATE: 6/9/2008	
	TITLE: SPARTAN 3A EVALUATION BOARD	REV: B	
	LEVEL: PRIMARY SOLDER MASK		



AES	CUSTOMER: AVNET ELECTRONICS MARKETING	DATE:	6/9/2008
	TITLE: SPARTAN 3A EVALUATION BOARD	REV:	B
	LEVEL: SECONDARY SOLDER MASK		

Symbol	Hit Count	Tool Size	Plated	Hole Type
□	493	0.254mm (10mil)	PTH	Round
⊠	2	1.016mm (40mil)	NPTH	Round
○	78	1.016mm (40mil)	PTH	Round
▽	12	1.0922mm (43mil)	PTH	Round
⊠	1	1.6002mm (63mil)	NPTH	Round
⌖	1	1.8034mm (71mil)	NPTH	Round
☼	4	3.175mm (125mil)	NPTH	Round
	591 Total			

Layer	Description	Stack Up Detail		
1	Primary Component	core	e_r=4.8	0.32mm
2	GND plane	prepreg	e_r=4.8	0.787mm
3	Inner Signal/PWR Plane	core	e_r=4.8	0.32mm
4	Secondary Component			

AES	CUSTOMER: AVNET ELECTRONICS MARKETING		DATE: 6/9/2008
	TITLE: SPARTAN 3A EVALUATION BOARD		REV: B
	LEVEL: FAB / DRILL ID		

NOTES: UNLESS OTHERWISE SPECIFIED

1. BOARD SHALL BE FABRICATED – PERFORMANCE CLASS II AS PER IPC–6011 AND IPC–6012
2. VENDOR LOGO, VENDOR P/N, REVISION AND DATE CODE OF MANUFACTURING SHALL BE ETCHED ON THE SOLDER SIDE. THE DATE CODE SHALL BE IN THE FORMAT: "WWYY" WHERE WW=WEEK AND YY=YEAR
3. FABRICATE USING FILM "FAB/DRILL IDENT" FOR REFERENCE
4. PERMANENTLY MARK BARE BOARD WITH TEST STAMP USING NON–CONDUCTIVE, RoHS COMPLIANT INK
5. SILKSCREEN BOTH SIDES WITH NON–CONDUCTIVE, RoHS COMPLIANT INK, NOT ALLOWED ON COMPONENT PADS, COMPONENT MOUNTING HOLES, OR VIAS (COLOR = WHITE)
6. MATERIAL: PER IPC–4101A/24/26/29/99, COPPER CLAD, HIGH TEMPERATURE FR4 CLASS EPOXY GLASS RATED UL94V–0, 0.5 OZ COPPER FOR EXTERNAL LAYERS AND 0.5 OZ COPPER FOR INTERNAL LAYERS. MUST BE RoHS COMPLIANT AND SURVIVE A LEAD–FREE ASSEMBLY MAX REFLOW OF 260 DEG C (6 PASSES)
   - Td RATING: > 340 DEG C
   - Z AXIS CTE < 3.5%
   - Tg > 170 DEG C (MIN)
7. SOLDER MASK: SMOBC PER IPC–SM–840C, CLASS T, MUST BE RoHS COMPLIANT, TYPE LPI, 0.0002" MIN TO 0.0008" MAX MEASURED OVER COPPER PLATING, MUST CLEAR ALL LANDS AS INDICATED ON GERBER SOLDER MASK LAYERS, (COLOR = RED)
8. FINISH: ELECTRO–LESS NICKEL IMMERSION GOLD (ENIG), 2–8 MICRO INCHES GOLD OVER 150–250 MICRO INCHES NICKEL
9. SOLDERABILITY TEST: CATEGORY 2 OF J–STD–003
10. ALL TEST POINTS SHALL BE FREE OF SOLDERMASK AND SILKSCREEN
11. ALL HOLE SIZES ARE AFTER PLATING
12. VENDOR MAY USE TEAR DROPS TO IMPROVE ANNULAR RINGS AS LONG AS DRC RULES ARE FOLLOWED
13. FINISHED BOARDS SHALL NOT HAVE NICKS, SCRATCHES, VOIDS, EXPOSED COPPER, POOR PLATING OR MISDRILLED HOLES
14. TIE–BARS ON THERMAL PADS SHOULD BE 15 MILS MINIMUM WIDTH
15. MAKE ALL VIA CONNECTIONS TO POWER AND GROUND PLANES SOLID (IE: THERMALS WITH 25 MIL O.D. OR 45 MIL O.D. SHOULD BE REMOVED FROM INNER PLANE LAYERS)
16. VENDOR MAY ADD COPPER THIEVING AS NEEDED TO IMPROVE MANUFACTURABILITY, THIEVING TO BE 0.030" ROUND PADS AT 0.050" SPACING. THIEVING WILL HAVE A MINIMUM OF 0.100" CLEARANCE FROM EXISTING COPPER AND SHOULD NOT BE PLACED UNDER SURFACE MOUNT DEVICES
17. ALL UNCONNECTED PADS ON INNER SIGNAL LAYERS MUST BE REMOVED
18. ALL FINISHED BOARDS TO BE 100% ELECTRICALLY TESTED
19. UNLESS OTHERWISE INDICATED, ALL LINEAR TOLERANCES SHALL BE XX +/– .010 AND XXX +/– .005

ADDITIONAL NOTES:

21. FINISHED BOARD THICKNESS = 0.063"(+/– 0.007")
22. CONTROL DIFFERENTIAL IMPEDANCE TO 90 OHMS +/– 10% ON ALL EXTERNAL SIGNALS OF WIDTH 7.52 MILS
23. ALL VIAS ON PRIMARY COMPONENT SIDE (LAYER 1) ARE TO BE TENTED WITH APPROPRIATE, RoHS COMPLIANT, SOLDER MASK (SECONDARY OPERATION)