Spartan-3A Evaluation Board	
Avnet Design Services	
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U_Sp3A Eval Block Diagram
02 Sp3A Eval Block Diagram.SchDoc

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Title: Sheet 1 - Lead Sheet		
Size: B	Document Number: Doc #	Rev: B
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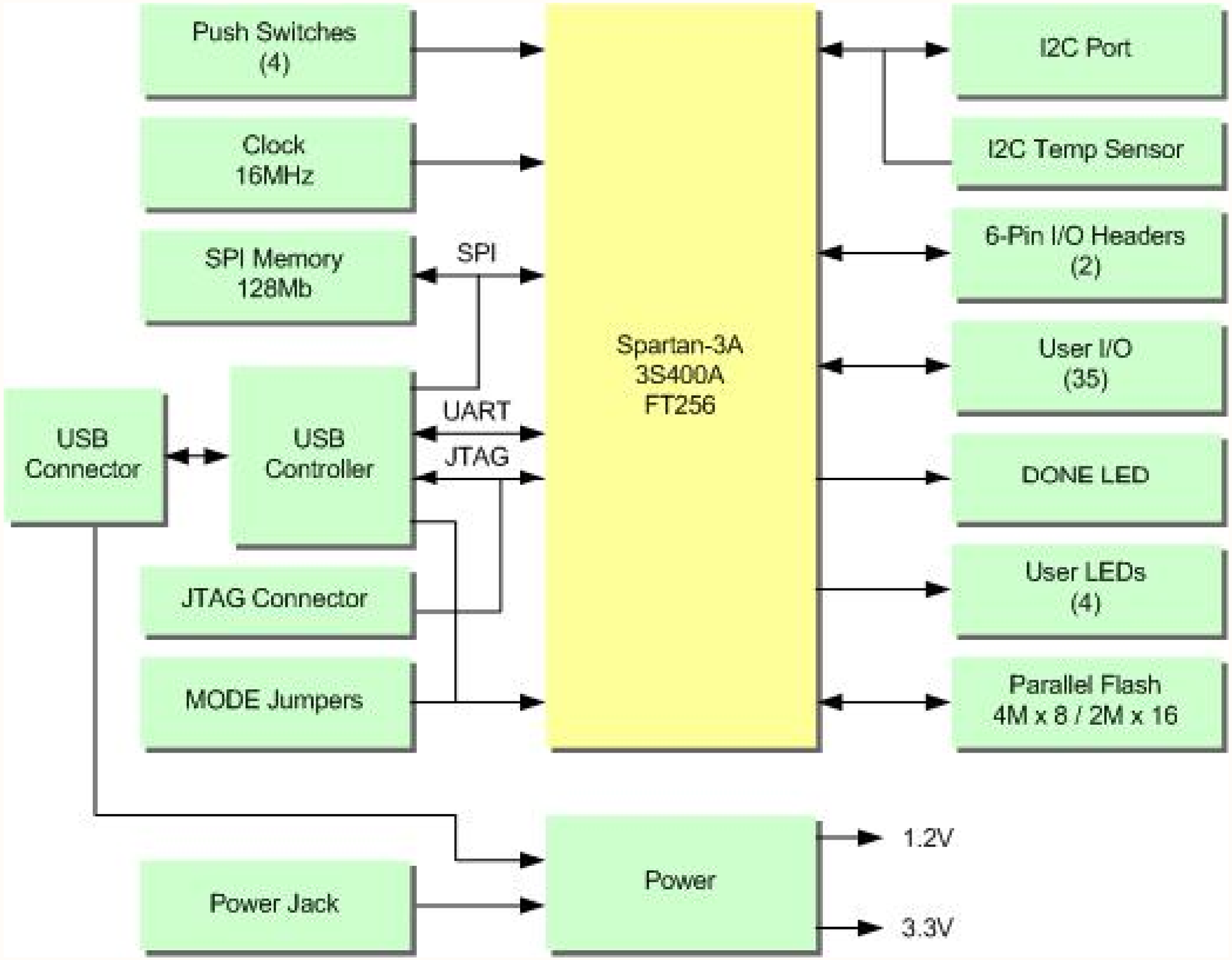
U_03 Sp3A Eval Architecture
03_Sp3A Eval Architecture.SchDoc



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Title: Sheet 2 - Block Diagram			
Size: B	Document Number: Doc #		Rev: B
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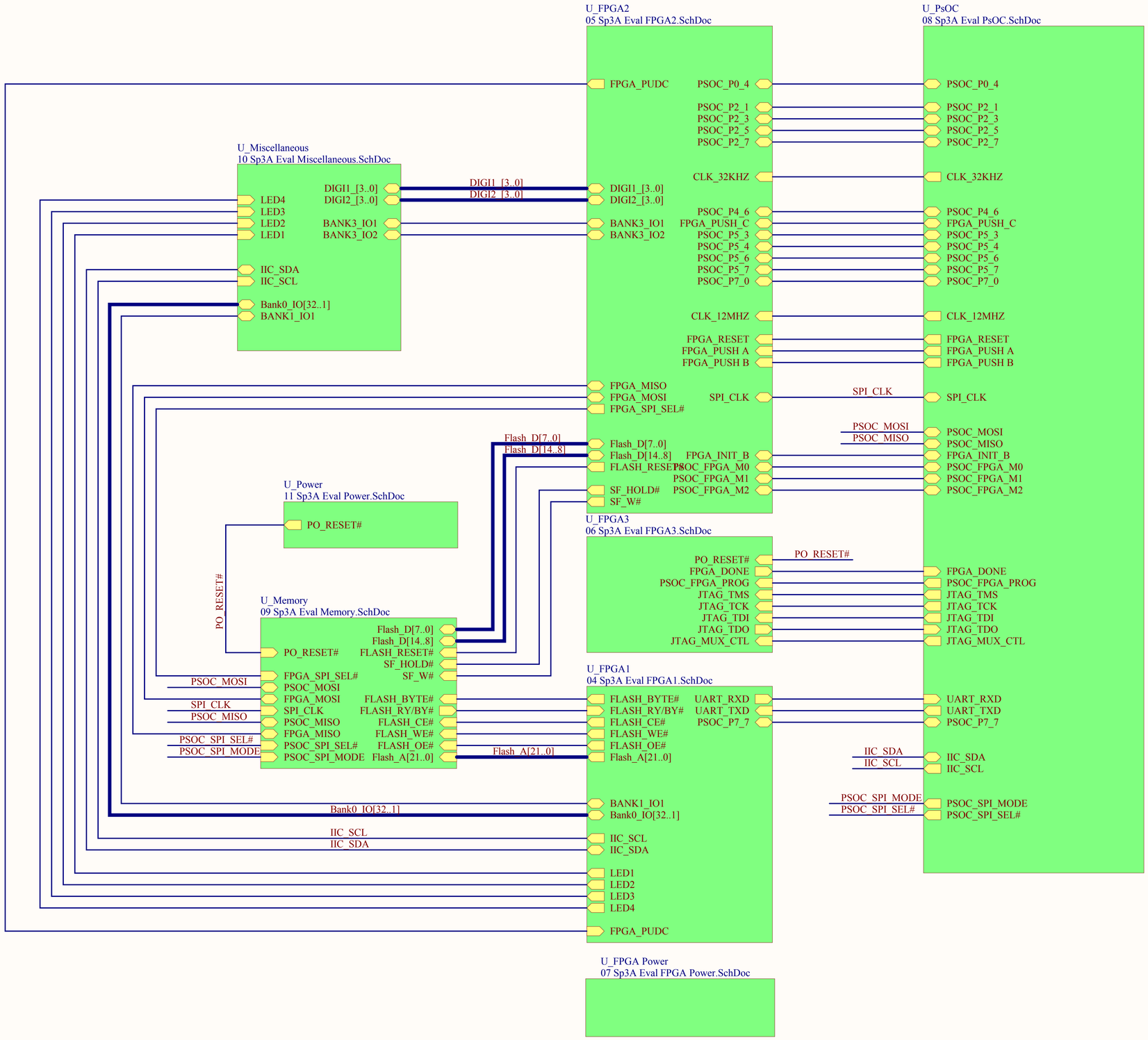

Avnet Engineering Services	
Title:	Sheet 3 - Spartan 3A Sample Board Hierarchy
Size: B	Document Number: Doc # Rev: B
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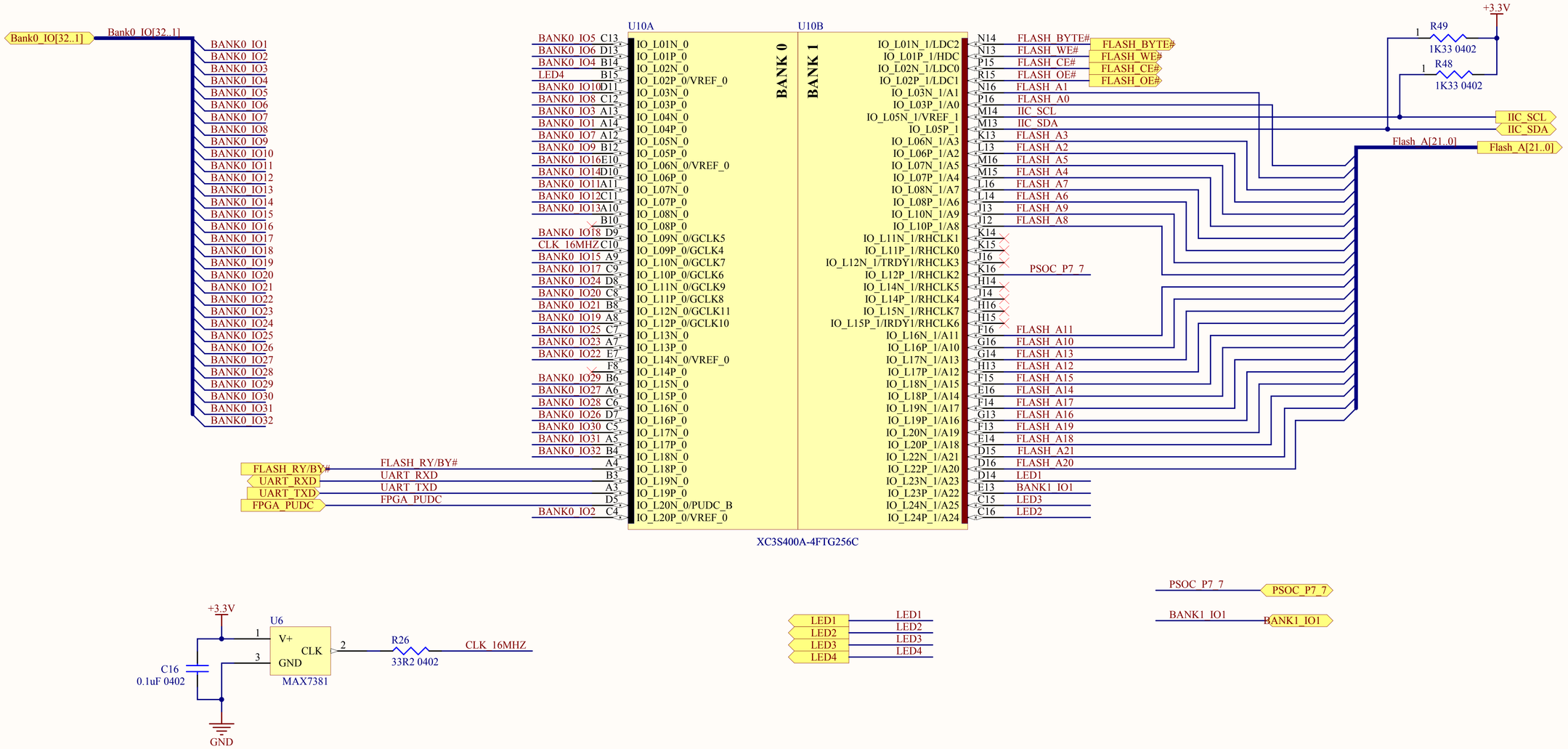

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Title:	Sheet 4 - FPGA1 (Banks 0 & 1)
Size: B	Document Number: Doc #
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M2	M1	M0	PUDC_B			
Configuration Mode:		PC Pull-up:	JP4 5:6	JP4 3:4	JP4 1:2	JP4 7:8
Master Serial		Yes	Closed	Closed	Closed	Closed
Master Serial		No	Closed	Closed	Closed	Open
Slave Serial		Yes	Open	Open	Open	Closed
Slave Serial		No	Open	Open	Open	Open
Master SPI		Yes	Closed	Closed	Open	Closed
Master SPI		No	Closed	Closed	Open	Open
BPI Up		Yes	Closed	Open	Closed	Closed
BPI Up		No	Closed	Open	Closed	Open
Slave Parallel		Yes	Open	Open	Closed	Closed
Slave Parallel		No	Open	Open	Closed	Open
JTAG		Yes	Open	Closed	Open	Closed
JTAG		No	Open	Closed	Open	Open

+3.3V
RP2
10K0
PSOC_FPGA_M0
PSOC_FPGA_M1
PSOC_FPGA_M2
FPGA_PUDC
FPGA_SPI_SEL#
RP1
1K0
JP4
GND
HEADER 4X2 SM
JP4 default settings: 3:4, 5:6 jumpered, 1:2, 7:8 open
U10C
U10D
BANK 2
BANK 3
FPGA_VS2
FPGA_VS0
FPGA_VS1
FLASH_D9
FLASH_D12
FLASH_D13
FLASH_D6
FLASH_D7
FLASH_D14
FLASH_D11
FLASH_D4
FLASH_D5
CLK_32KHZ
CLK_12MHZ
FPGA_MOSI
FLASH_RESET#
DOUT
AWAKE
FLASH_D10
FLASH_D8
FLASH_D3
FPGA_INIT_B
FLASH_D1
FLASH_D2
SF_HOLD#
SF_W#
SPI_CLK
FPGA_MISO
FLASH_D0
R40 1K0 0402
R41 DNP 0402
R34 1K0 0402
R35 DNP 0402
R32 1K0 0402
R33 DNP 0402
R27 49R9 0402
R24 49R9 0402
R10 1K0 0402
TP5 TEST PAD
D6 LED_Green
XC3S400A-4FTG256C

U10C		U10D	
P4	IO_L01N_2/M0	C1	IO_L01N_3
N4	IO_L01P_2/M1	C2	IO_L01P_3
T2	IO_L02N_2/CSO_B	D3	IO_L02N_3 BANK3_IO1
R2	IO_L02P_2/M2	D4	IO_L02P_3 BANK3_IO2
T3	IO_L03N_2/VS2	E1	IO_L03N_3
R3	IO_L03P_2/RDWR_B	D1	IO_L03P_3
P5	IO_L04N_2/VS0	E2	IO_L05N_3
N6	IO_L04P_2/VS1	E3	IO_L05P_3
R5	IO_L05N_2	G4	IO_L07N_3
T4	IO_L05P_2	F3	IO_L07P_3
T6	IO_L06N_2/D6	G1	IO_L08N_3/VREF_3 DIGI2_3
T5	IO_L06P_2/D7	F1	IO_L08P_3 PSOC_P2_1
P6	IO_L07N_2	H4	IO_L09N_3 FPGA_RESET
N7	IO_L07P_2	G3	IO_L09P_3
N8	IO_L08N_2/D4	H5	IO_L10N_3 FPGA_PUSH B
P7	IO_L08P_2/D5	H6	IO_L10P_3
T7	IO_L09N_2/GCLK13	H1	IO_L11N_3/LHCLK1 PSOC_P2_7
R7	IO_L09P_2/GCLK12	G2	IO_L11P_3/LHCLK0 PSOC_P2_3
T8	IO_L10N_2/GCLK15	J3	IO_L12N_3/IRDY2/LHCLK3
P8	IO_L10P_2/GCLK14	H3	IO_L12P_3/LHCLK2 PSOC_P2_5
P9	IO_L11N_2/GCLK1	J1	IO_L14N_3/LHCLK5 PSOC_P0_4
N9	IO_L11P_2/GCLK0	J2	IO_L14P_3/LHCLK4 PSOC_P4_6
T9	IO_L12N_2/GCLK3	K1	IO_L15N_3/LHCLK7 DIGI2_2
R9	IO_L12P_2/GCLK2	K3	IO_L15P_3/TRDY2/LHCLK6 FPGA_PUSH A
M10	IO_L13N_2	L2	IO_L16N_3 PSOC_P5_3
N10	IO_L13P_2	L1	IO_L16P_3/VREF_3 PSOC_P5_7
P10	IO_L14N_2/MOSI/CSI_B	J6	IO_L17N_3
T10	IO_L14P_2	J4	IO_L17P_3
R11	IO_L15N_2/DOUT	L3	IO_L18N_3 FPGA_PUSH C
T11	IO_L15P_2/AWAKE	K4	IO_L18P_3
N11	IO_L16N_2	L4	IO_L19N_3
P11	IO_L16P_2	M3	IO_L19P_3 PSOC_P5_4
P12	IO_L17N_2/D3	N1	IO_L20N_3 DIGI2_0
T12	IO_L17P_2/INIT_B	M1	IO_L20P_3 DIGI2_1
R13	IO_L18N_2/D1	P1	IO_L22N_3 DIGI1_2
T13	IO_L18P_2/D2	N2	IO_L22P_3 DIGI1_3
P13	IO_L19N_2	P2	IO_L23N_3 DIGI1_1
N12	IO_L19P_2	R1	IO_L23P_3 DIGI1_0
R14	IO_L20N_2/CCLK	M4	IO_L24N_3 PSOC_P5_6
T14	IO_L20P_2/D0/DIN/MISO	N3	IO_L24P_3 PSOC_P7_0

Flash_D[7..0]
FLASH_D0
FLASH_D1
FLASH_D2
FLASH_D3
FLASH_D4
FLASH_D5
FLASH_D6
FLASH_D7

Flash_D[14..8]
FLASH_D8
FLASH_D9
FLASH_D10
FLASH_D11
FLASH_D12
FLASH_D13
FLASH_D14

Note: Flash data bit D15 is on Flash_A0

FPGA_RESET
FPGA_PUSH A
FPGA_PUSH B
FPGA_PUSH C

BANK3_IO1
BANK3_IO2

PSOC_P0_4
PSOC_P2_7
PSOC_P2_5
PSOC_P2_3
PSOC_P2_1

PSOC_P7_0
PSOC_P5_7
PSOC_P5_6
PSOC_P5_4
PSOC_P5_3

PSOC_P4_6

DIGI1_[3..0]
DIGI1_0
DIGI1_1
DIGI1_2
DIGI1_3

DIGI2_[3..0]
DIGI2_0
DIGI2_1
DIGI2_2
DIGI2_3

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Title: Sheet 5 - FPGA2 (Banks 2 & 3)		
Size: B	Document Number: Doc #	Rev: B
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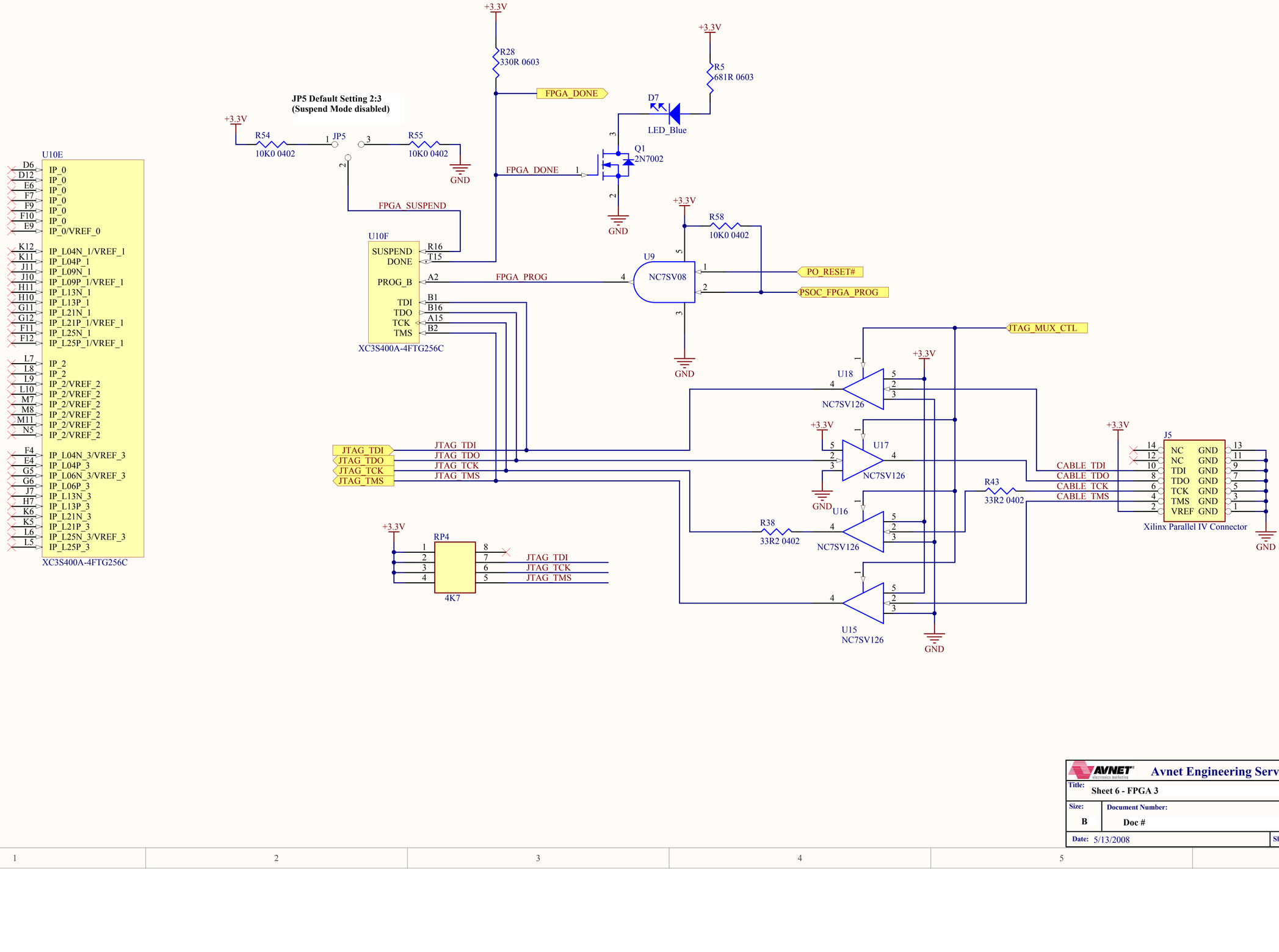
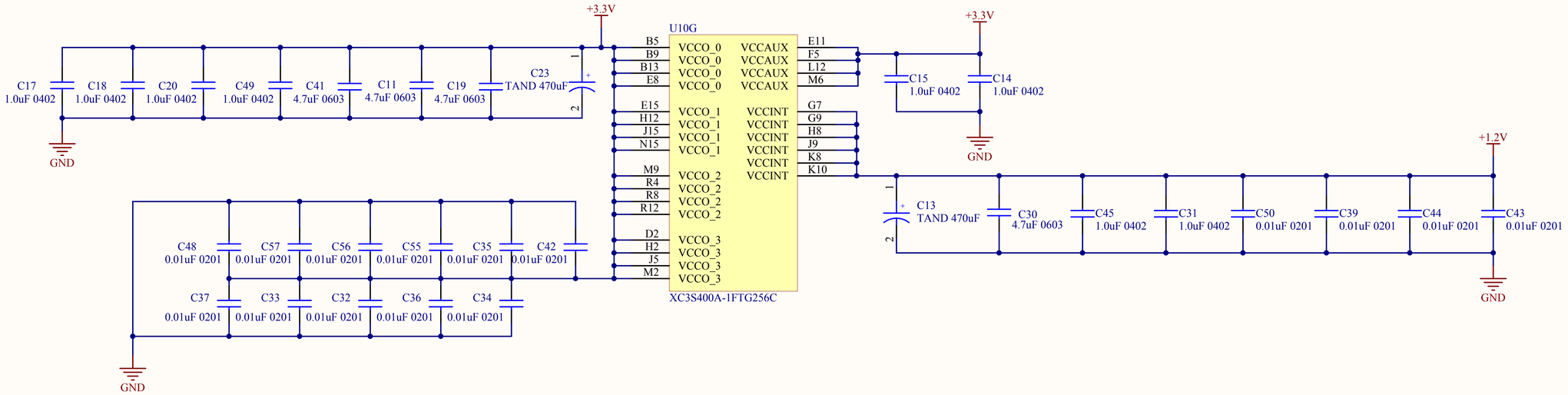
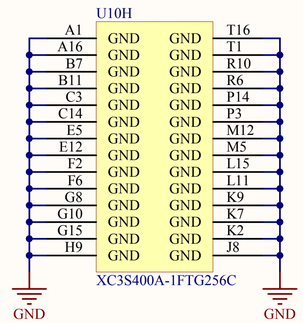


Avnet Engineering Services	
Title:	Sheet 6 - FPGA 3
Size: B	Document Number: Doc #
Rev:	B
Date: 5/13/2008	Sheet 6 of 12





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Title:	Sheet 7 - FPGA Power
Size: B	Document Number: Doc # Rev: B
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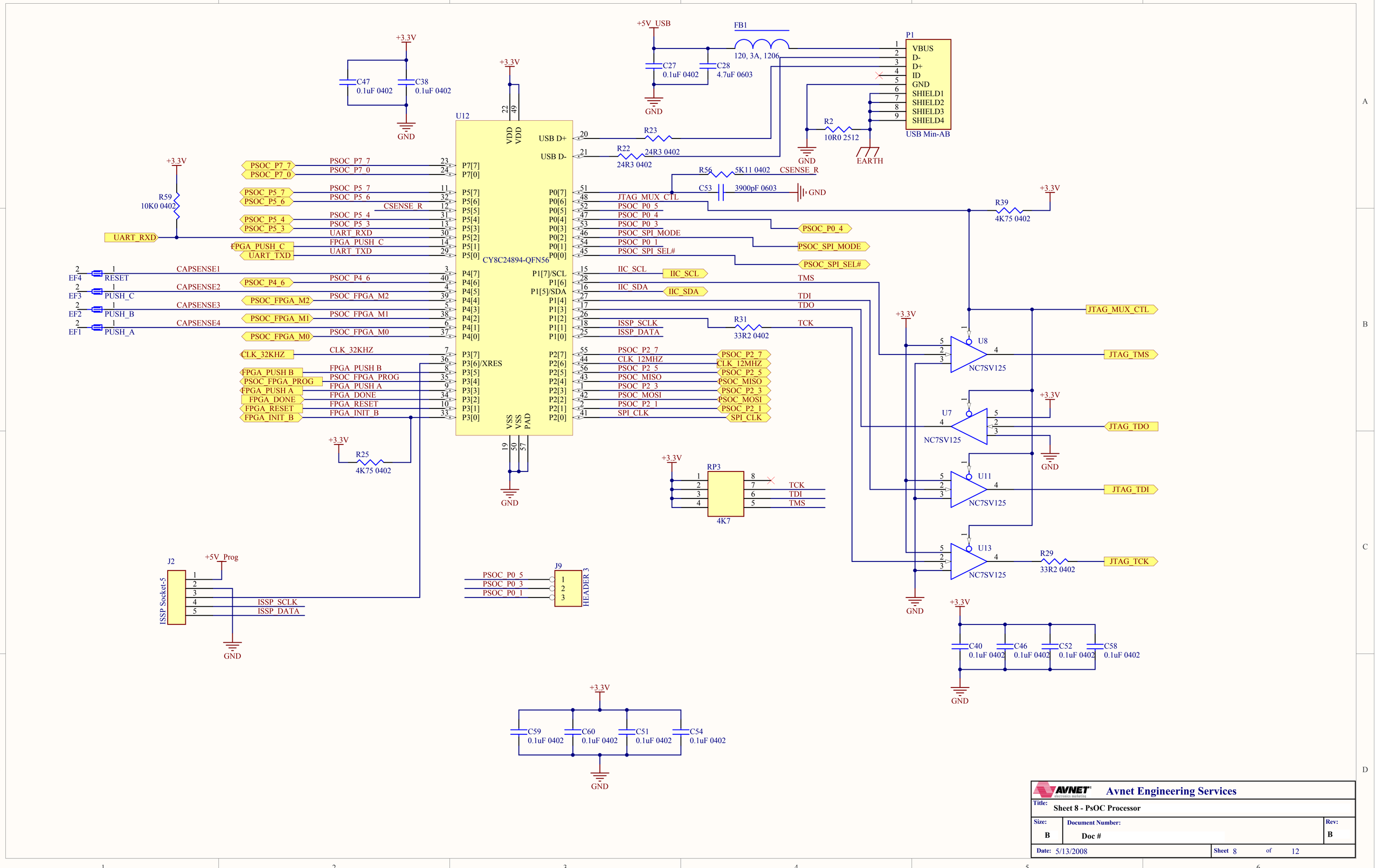

Title:	Sheet 8 - PsOC Processor
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PsOC_SPI_MODE = 0 (default condition) , FPGA_SPI_SEL#
or PsOC_SPI_SEL# = 0 (with JP6 jumpered):
FPGA_MOSI or PsOC_MOSI to SPI_FLASH_SI
SPI_FLASH_SO to FPGA_MISO and PsOC_MISO
Flash_CE# must be high in order to enable the Mux (U14)

PsOC_SPI_MODE = 1:
FPGA_MOSI to PsOC_MISO
PsOC_MOSI to FPGA_MISO

PsOC/FPGA SPI interfaces are isolated through 100-ohm current-limiting resistors (2x 49.9-ohm each line).

Note that access to the parallel flash will cause the Mux (U20) to be disabled

JP6 default = jumpered. Disconnect JP6 jumper to provide off-board SPI via J8

Note: This footprint accomodates the future Spansion quad-bit SPI Flash. If that is used, SPI_MOSI is IO0, Flash_D0 is IO1, SPI_W# is IO2, and SPI_HOLD# is IO3. It also accomodates the the SOC008 package where Pin #1 of that package would mate with Pin #3 of the 16-pin footprint.

JP1 default setting = Open (no write protect)

Note: DQ15 becomes the LSB address input in Byte mode

Title:	Sheet 9 - Memory
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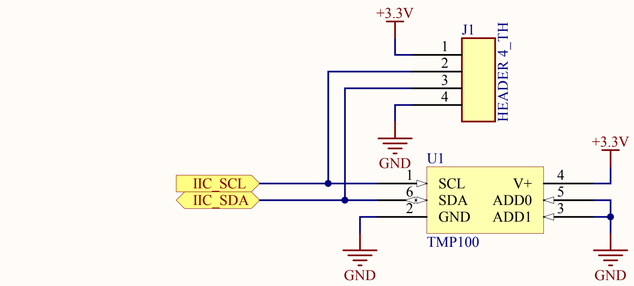

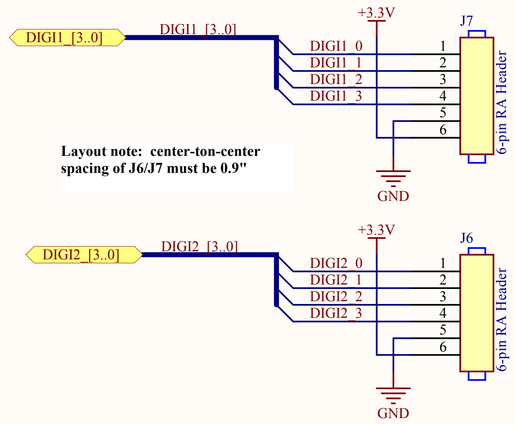

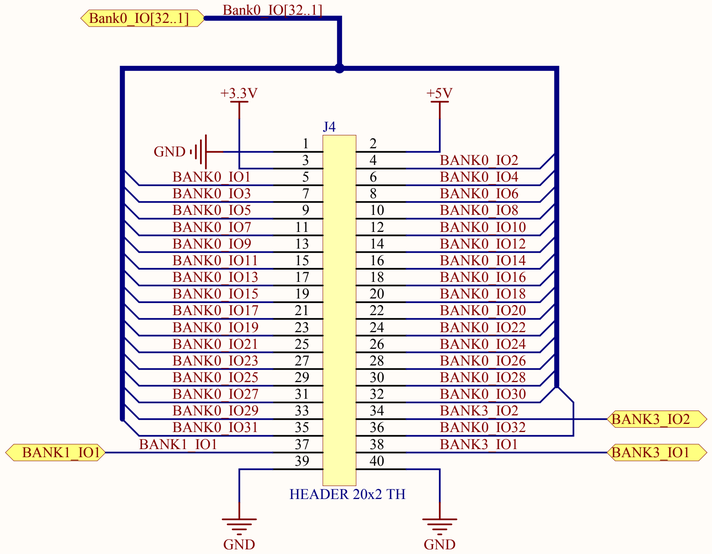

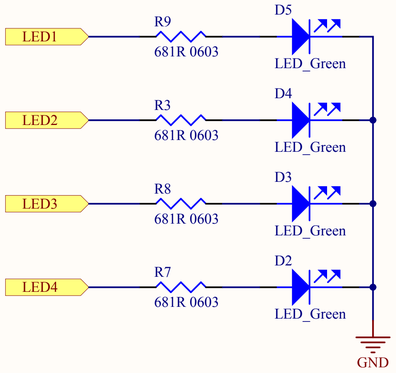

AVNET electronics marketing — Avnet Engineering Services			
Title: Sheet 10 - Miscellaneous Functions			
Size: B	Document Number: Doc #		Rev: B
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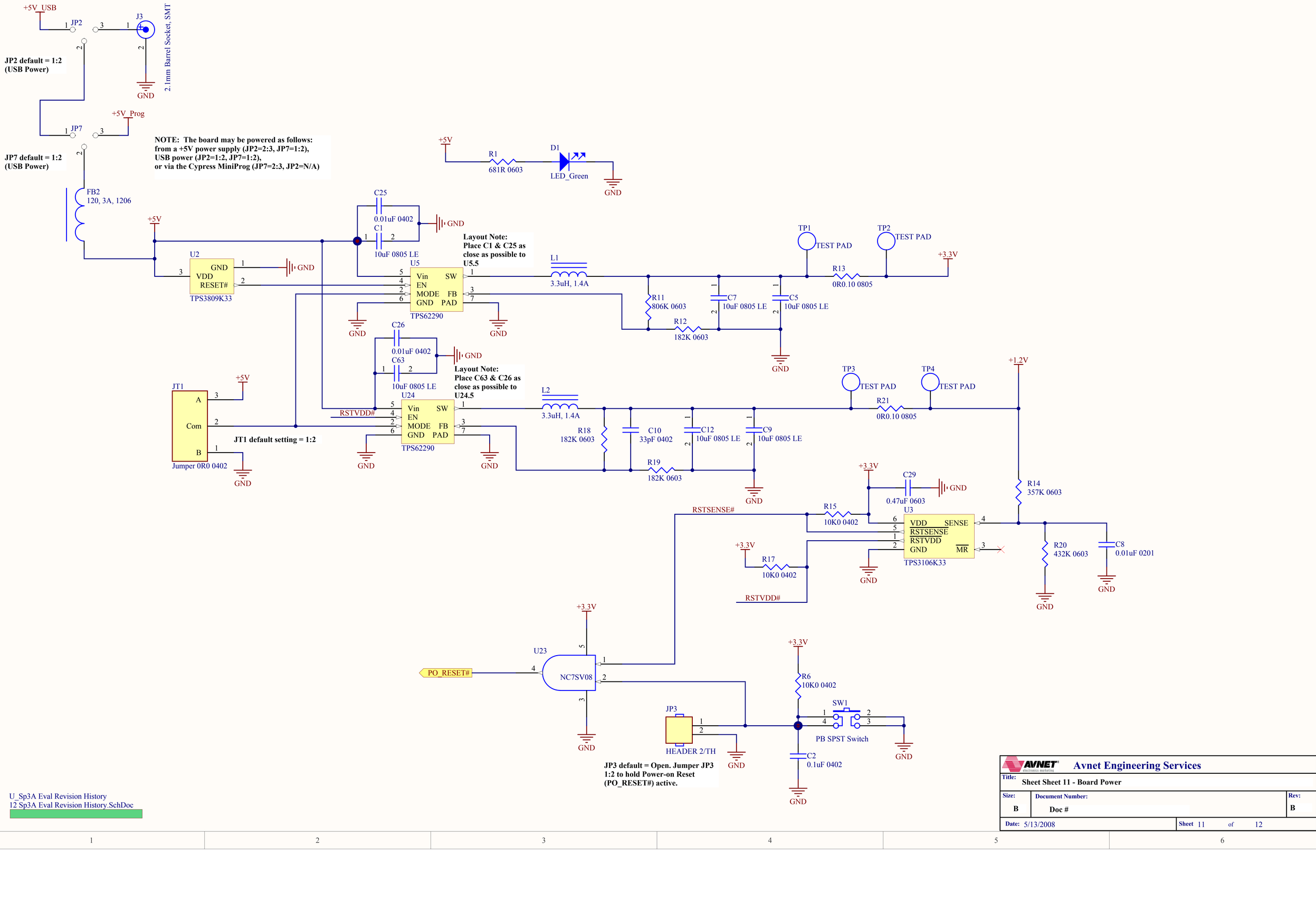
+5V_USB
JP2
J3
2.1mm Barrel Socket, SMT
GND
JP2 default = 1:2
(USB Power)
+5V_Prog
JP7
JP7 default = 1:2
(USB Power)
NOTE: The board may be powered as follows:
from a +5V power supply (JP2=2:3, JP7=1:2),
USB power (JP2=1:2, JP7=1:2),
or via the Cypress MiniProg (JP7=2:3, JP2=N/A)
FB2
120, 3A, 1206
+5V
R1
681R 0603
D1
LED_Green
C25
0.01uF 0402
C1
10uF 0805 LE
Layout Note:
Place C1 & C25 as
close as possible to
U5.5
U2
GND
VDD
RESET#
TPS3809K33
U5
Vin SW
EN
MODE FB
GND PAD
TPS62290
L1
3.3uH, 1.4A
TP1
TEST PAD
TP2
TEST PAD
+3.3V
R13
0R0.10 0805
R11
806K 0603
C7
10uF 0805 LE
C5
10uF 0805 LE
R12
182K 0603
C26
0.01uF 0402
C63
10uF 0805 LE
Layout Note:
Place C63 & C26 as
close as possible to
U24.5
JT1
Com
Jumper 0R0 0402
JT1 default setting = 1:2
U24
RSTVDD#
L2
3.3uH, 1.4A
TP3
TEST PAD
TP4
TEST PAD
+1.2V
R21
0R0.10 0805
R18
182K 0603
C10
33pF 0402
C12
10uF 0805 LE
C9
10uF 0805 LE
R19
182K 0603
+3.3V
C29
0.47uF 0603
U3
VDD SENSE
RSTSENSE
RSTVDD
GND MR
TPS3106K33
RSTSENSE#
R15
10K0 0402
R17
10K0 0402
RSTVDD#
R14
357K 0603
R20
432K 0603
C8
0.01uF 0201
U23
NC7SV08
PO_RESET#
JP3
HEADER 2/TH
JP3 default = Open. Jumper JP3
1:2 to hold Power-on Reset
(PO_RESET#) active.
R6
10K0 0402
SW1
PB SPST Switch
C2
0.1uF 0402
AVNET
Avnet Engineering Services
Title: Sheet Sheet 11 - Board Power
Size: B
Document Number: Doc #
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Sheet 11 of 12
U_Sp3A Eval Revision History
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REV A	REV B

Added 10K pullup (R58) to PsOC_FPGA_PROG

Corrected PCB footprint of J2 PsOC ISSP header (connector keying was reversed).

Renamed NET PsOC_P5_1 to PUSH_C

Replaced 5.0V power supervisor TPS3809I50DBVT (U2) with 3.3V version (TPS3809K33DBVT)

Changed 681-ohm resistor R1 from 0402 to 0603
Changed 10K resistors (R6 & R15) from 0603 to 0402

Layout: Change J6/J7 spacing from the current 31/32" to 0.9"

Added Jumper JT1 to allow different 1.2V/3.3V enable modes.

Updated silkscreen on PCB as follows:
- **Change EF1 to PUSH_A**
- **Change EF2 to PUSH_B**
- **Change EF3 to PUSH_C**
- **Change EF4 to RESET**

Add labels to J8: SEL#, MOSI, MISO, SCK, GND, 3.3V

Reduce font on JP4 and MODE to make room for mode setting information, such as:
- **M1, M2 = SPI**
- **M0, M2 = BPI**
- **M1 = JTAG**

Add labels to south side of JP4
M0 M1 M2 PUDC

Move J4 label to the right. Remove 1 and 4 labels. Using small font if necessary, label pins left to right as:
3.3V SCL SDA GND

Add "www.em.avnet.com/spartan3a-evl" wherever it will fit, either front or back

Replaced TPS62420 dual step-down converter with two TPS62290 step-down converters; added additional 10uF (C63) and 0.01uF (C26) capacitors to Vin of additional converter.

Added 10K pullup resistor R59 to PsOC/FPGA UART_RxD line

Added jumper JP7 to allow board power from Cypress MiniProg

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Title: Sheet 12 - Revision History		
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