2.- INTERCONNECT MODELING

INTRODUCTION

- Characteristics of nm interconnects
- Transmission line modeling; reflections
- Simpler models; when to use them
- Parameter calculation and measurement
- Extraction tools
INTRODUCTION

Back-end process (vs. front-end)

Classification:
• Local
• Intermediate
• Global

Usually alternating directions (Manhattan)

IMPORTANT OF INTERCONNECTS

Delay
• Performance: Wiring delay exceeds gate delay at 130 nm node, is already 75% of total delay at 90 nm node

Reflections
• Ringing, overshoots, slew rate…

Crosstalk
• Signal integrity
• Induced delay

Clock distribution
• Clock skew

Power-supply distribution
• IR drop
• dl/dt noise

Reliability / Electromigration

From "Nano-CMOS Circuit and Physical Design", Wong et al, IEEE Press

Interconnect modeling - 3

Interconnect modeling - 4
CHARACTERISTICS OF nm INTERCONNECTS

Characteristics of a typical 65 nm process:

- 8 metal layers
- Cu interconnects
- Low-k dielectrics (carbon doped oxide)
- M1 distance ~ M1 width ~ 100 nm
- M5 distance ~ M5 width ~ 150 nm
- Approx. 600 m/cm² (excluding global levels)
- M1 length at which RC delay = gate delay: 80 µm

Characteristics of a typical 45 nm process:

- M1 distance ~ M1 width ~ 80 nm
- M5 distance ~ M5 width ~ 140 nm

CHARACTERISTICS OF nm INTERCONNECTS

High aspect ratio:
• Objective: minimize $C_g$ while preserving $R$ (minimize RC delay)

1. Performance problem: due to reduced pitch, $C_{coupling}$ increases, thus
   • 1) total $C$ increases and
   • 2) crosstalk increases

2. Manufacturing problem:
   • difficulty to create deep, narrow trenches;
   • difficulty to and fill them up uniformly with metal (possible voids, pinch-off)
   • This limits $t/w$ to a maximum factor of 4

Conventional manufacturing procedure:
1. non-selective deposition of aluminium layer
2. photolithography step
3. selective aluminium etching
4. oxide deposition
5. oxide CMP
   (Chemical-Mechanical Polishing)

Result not suitable for high-aspect ratio interconnects:

Interconnects of a 0.5 \( \mu \)m technology
CHARACTERISTICS OF nm INTERCONNECTS

Copper technology:
• Aluminum (Al) was the traditional material for interconnects, but has high resistivity (~3.3 $\mu\Omega\cdot cm$)
• Copper was introduced by IBM in 1997. Resistivity is ~2.2 $\mu\Omega\cdot cm$, allowing a 30% to 40% delay time reduction over Al for the same cross section
• Also electromigration performance of Cu is better than Al.
• Al process was dry etching; Cu requires Dual-Damascene process: oxide etch, metal fill, planarization.
• An etch-stop layer ($Si_3N_4$ or SiCN) is needed

Dual Damascene process:
• Trench-first approach

• Via-first approach

• Finally, trench is filled with Tantalum barrier and Copper, CMP is applied for planarization

From "Current Technical Techniques: Dual-Damascene & Low-k Dielectrics", Jerry Healey
CHARACTERISTICS OF nm INTERCONNECTS

Copper technology:
- Nevertheless resistivity increases below 100 nm due to:
  - width process variation (surface roughness scattering)
  - grain scattering
  - edge effects (surface scattering; note that mean free path for electron scattering in copper is 39.3 nm, therefore surface scattering can hinder longitudinal conduction)
- Also frequency effects (skin)

From "Nano-CMOS Circuit and Physical Design", Wong et al, IEEE Press

Copper technology:
- An important cause of resistivity variation is erosion and dishing during planarization
  - Planarization is made with chemical-mechanical polishing (CMP); due to the different material properties of metal and dielectric (copper softer than dielectric), polishing is not uniform
  - Dishing more severe in wider lines (slots required for very wide lines)
CHARACTERISTICS OF nm INTERCONNECTS

Low-κ dielectrics:
- \( \varepsilon_r (\text{SiO}_2) \sim 3.9 \)
- Objective: minimize C while scaling down the wire pitch.
- Many materials tested: SiOC (\( \varepsilon_r \sim 2.9 \)), parylene (\( \varepsilon_r \sim 2.3 \)), dendriglass (\( \varepsilon_r \sim 1.5 \)), xerogel (\( \varepsilon_r \sim 1.3 \))...
- Their porous characteristics are good for low-κ, but have many drawbacks
  - Prone to voids (can create shorts)
  - Lower thermal conduction (worse electromigration properties)
  - Thermal and mechanical stress at the interface with metal (worse reliability)

INTERCONNECT MODELING

- Models are needed to predict the effects associated to interconnects (delay, reflections, crosstalk, etc.).
- Different models can be chosen
  - simple short
  - C
  - RC
  - RLC
  - RLC with frequency-dependant parameters
  - Transmission line
  - Coupled transmission lines
  - Full EM analysis of coupled elements
- The problem is how to assign a proper model to each interconnection subsystem so that the model predicts only the effects important for that subsystem, while preserving reasonable simulation times.
TRANSMISSION LINES

- Any signal propagated through an interconnect is a propagating wave, but this can be highly simplified if appropriate conditions apply.

- TEM wave assumption: if ideal conductors ($\rho=0$) and dielectrics ($\varepsilon=0$), then it can be assumed that no field components exist in the direction of propagation of the wave:

  \[
  E_z = 0 \quad E = E_x \hat{x} + E_y \hat{y} = E_t \\
  H_z = 0 \quad H = H_x \hat{x} + H_y \hat{y} = H_t
  \]

TRANSMISSION LINES

- From Maxwell’s equations these wave equations can be derived \(^1\):

  \[
  \frac{\partial^2 E_t}{\partial z^2} - \mu \frac{\partial^2 H_t}{\partial t^2} = 0 \\
  \frac{\partial^2 H_t}{\partial z^2} - \mu \varepsilon \frac{\partial^2 E_t}{\partial t^2} = 0
  \]

  and using the definition of voltage difference and current:

  \[
  V(z) = -\int_1^z E_t \cdot dl \\
  I = \int H_t \cdot dl
  \]

  the Telegrapher’s equations can be derived:

  \[
  \frac{\partial V}{\partial z} = -L \frac{\partial I}{\partial t} \\
  \frac{\partial I}{\partial z} = -C \frac{\partial V}{\partial t}
  \]

  Where L and C are inductance per unit length and capacitance per unit length, respectively.

TRANSMISSION LINES

• In practice conductors and dielectrics are lossy, and the former Telegrapher's equations are not valid.
• Nevertheless, if losses are small, an approximation can be derived assuming quasi-static voltage and current in the orthogonal direction. This is the quasi-TEM approximation. Assumptions made are:
  • Current flows only in the direction of propagation
  • There is only a small perturbation of the fields respect to the TEM solution

Under this approximation the Telegrapher's equations are:

\[
\frac{\partial V}{\partial z} = -RI - L \frac{\partial I}{\partial t}
\]

\[
\frac{\partial I}{\partial z} = -GV - C \frac{\partial V}{\partial t}
\]

Where R and G are the conductor resistance and dielectric conductance per unit length, respectively. These are found under a static analysis.

• Note that these equations have a direct translation into an electrical circuit:

\[
\frac{\partial V}{\partial z} = -RI - L \frac{\partial I}{\partial t}
\]

\[
\frac{\partial I}{\partial z} = -GV - C \frac{\partial V}{\partial t}
\]
TRANSMISSION LINES

• The solutions to the former equations are waves propagating in the z-direction

\[ V(z) = V_0^+ \exp(-\gamma z) + V_0^- \exp(+\gamma z) \]
\[ I(z) = I_0^+ \exp(-\gamma z) + I_0^- \exp(+\gamma z) \]

where \( \gamma \) is the propagation constant:
\[ \gamma = -j \beta \approx \sqrt{(R + j\omega L)(G + j\omega C)} \]
\( \alpha \) is known as the attenuation coefficient and \( \beta \) is the phase-change coefficient.

For low losses, or at frequencies high enough,
\[ \gamma = j \beta \approx \omega \sqrt{LC} \]

• Given that a wave experiences 2\( \pi \) radians phase shift over a full wavelength

\[ \beta \lambda = 2\pi = \beta \frac{v_p}{f} \]
\[ v_p = \frac{2\pi f}{\beta} = \frac{\omega}{\beta} = \frac{\omega}{\omega \sqrt{LC}} = \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{\mu \varepsilon}} = \frac{c}{\sqrt{\mu \varepsilon_r}} \]

Remember
\[ \varepsilon_r = 8.854 \times 10^{-12} \text{ F/m} \]
\[ \mu_0 = 4\pi \times 10^{-7} \text{ H/m} \]

• Is the propagation speed dependence on \( \varepsilon_r \) consistent with the capacitance dependence with \( \varepsilon_r \)?
• Which is the propagation speed of a chip interconnect in SiO2?
• Given a multilayer PCB, which interconnects will be faster?
• How should be the coaxial lines for microwaves (tens of GHz)?
TRANSMISSION LINES

• Interconnect characteristic impedance is defined as the ratio between voltage and current waves

\[ Z_0 \approx \frac{R + j\omega L}{\sqrt{G + j\omega C}} \]

which in the low-loss, high-freq. situation can be approximated to this real value

\[ Z_0 \approx \frac{L}{\sqrt{C}} \]

• For a given line geometry (coaxial, microstrip, CW, etc.), L and C can be expressed in terms of geometrical parameters, and thus \( Z_0 \) can always be adjusted when designing the line.

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TRANSMISSION LINES

• Note that electrical parameters R, L, C, G can be expressed in terms of \( Z_0 \) and \( \gamma \) as 1:

\[
X = Z_0 \gamma = \frac{R + j\omega L}{\sqrt{G + j\omega C}} \sqrt{(R + j\omega L)(G + j\omega C)} = R + j\omega L
\]

\[
Y = \frac{\gamma}{Z_0} = \frac{R + j\omega L}{\sqrt{G + j\omega C}} = G + j\omega C
\]

where X, Y, R, L, C, G are parameters per unit length

TRANSMISSION LINES

• Assuming that the line is loaded with an impedance \( Z_L \), the following expression for the input impedance can be derived:

\[
Z_{in} = Z_r \left( \frac{Z_L \cosh \gamma L + Z_s \sinh \gamma L}{Z_r \cosh \gamma L + Z_L \sinh \gamma L} \right)
\]

which in the lossless case simplifies to:

\[
Z_{in} = Z_r \left( \frac{Z_L + jZ_0 \tan \beta L}{Z_r + jZ_0 \tan \beta L} \right)
\]

- Which is the behavior of the line when the far-end is shorted?
  \( Z_{sc} = jZ_0 \tan \beta L \), inductance dependent on the line length, frequency

- Which is the behavior of the line when the far-end is open?
  \( Z_{oc} = -jZ_0 \cot \beta L \), capacitance dependent on the line length, frequency

- Which is the behavior of the line when \( Z_L = Z_0 \)?
  \( Z_{in} = Z_0 \), matched condition, broadband

REFLECTION AND RINGING

• Whenever a traveling wave encounters a load impedance, part of the wave is reflected and part is transmitted:

\[
\begin{align*}
V_l &= V_t \left( \frac{Z_L - Z_0}{Z_L + Z_0} \right) \quad V_r = V_t \left( \frac{Z_L - Z_0}{Z_L + Z_0} \right) \\
I_l &= I_t + I_r \quad \Gamma = \frac{Z_L - Z_0}{Z_L + Z_0}
\end{align*}
\]

- The reflection coefficient is defined as:

\[
\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0}
\]

Matching \( \Gamma = 0 \)
Short load \( \Gamma = -1 \)
Open load \( \Gamma = +1 \)

\( Z_L < Z_0 \Rightarrow \text{negative reflected pulse} \)
\( Z_L > Z_0 \Rightarrow \text{positive reflected pulse} \)
**REFLECTION AND RINGING**

- At the driving end

![Interconnect model](image)

\[ I_i = I_e + I_r \]

\[ \frac{V_i}{Z_o} = \frac{V_e - V_i}{Z_d} + \frac{V_r}{Z_o} = \frac{V_i + V_r}{Z_d} - \frac{V_e}{Z_o} \]

\[ V_e = V_i \frac{Z_d - Z_o}{Z_d + Z_o} + V_r \frac{Z_o}{Z_d + Z_o} \]

\[ V_i = V_i \frac{2Z_d}{Z_d + Z_o} + V_r \frac{Z_o}{Z_d + Z_o} \]

\[ \Gamma_d = \frac{Z_d - Z_o}{Z_d + Z_o} \]

- If \( Z_o < Z_d \) ⇒ negative reflected pulse

- If \( Z_o > Z_d \) ⇒ positive reflected pulse

**REFLECTION AND RINGING**

- Since a line has a driver and load, reflections occur at both ends:

![Interconnect model](image)

\[ \Gamma_d = \frac{Z_d - Z_o}{Z_d + Z_o} \]

\[ \Gamma_L = \frac{Z_L - Z_o}{Z_L + Z_o} \]

- The voltage at a given point and instant is the addition of the successive reflected waves:

![Voltage graphs](image)
**REFLECTION AND RINGING**

- Since a line has a driver and load, reflections occur at both ends:

\[ \Gamma_d = \frac{Z_d - Z_o}{Z_d + Z_o} \quad \Gamma_L = \frac{Z_L - Z_o}{Z_L + Z_o} \]

- The condition for ringing to occur is that the sign of \( \Gamma_d \) is different from that of \( \Gamma_L \), i.e.

\[ Z_d < Z_o < Z_L \quad \text{or} \quad Z_d > Z_o > Z_L \]

- Since CMOS circuit present capacitive input impedance (\( Z_L \uparrow \uparrow \)), in practice ringing occurs if \( Z_d < Z_o \)

**RINGING AND MODELING**

- It is very important to identify the conditions for ringing. When the conditions for *no ringing* apply, the interconnect does not need to be modeled as a transmission line (*inductive effects do not need to be included in the model*), and thus a simpler model can be used.

- We have already identified a *first* condition: \( Z_d < Z_o < Z_L \) or \( Z_d > Z_o > Z_L \)

- A *second* condition is that ringing will only show if the input transition is much faster than the propagation time, \( t_r << t_p \)

- A simple analysis (1) leads that ringing may appear if \( t_r < 2t_p \), and will never appear if \( t_r > 4t_p \)

- Others (2) suggest that the limits are \( t_r < 2.5t_p \) and \( t_r > 5t_p \), respectively

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RINGING AND MODELING

• On the other hand, the bandwidth of a digital pulse is often approximated by \( t_r \approx \frac{1}{4f} = \frac{\pi}{2\delta} \) (others make \( t_r \approx \frac{2}{\delta} \)).

• Therefore, \( t_r < 2t_p \quad t_r > 4t_p \)
  \[ \frac{1}{4f} < 2 \quad \frac{1}{v_p} \quad \frac{1}{4f} > 4 \quad \frac{1}{v_p} \]
  \[ \frac{\lambda}{4v_p} < 2 \quad \frac{1}{v_p} \quad \frac{\lambda}{4v_p} > 4 \quad \frac{1}{v_p} \]
  \[ \lambda < 8l \quad \lambda > 16l \]

…which is the criteria typically used to determine the need for transmission line modeling in case of single tones (in (2): \( \lambda < 10l \) and \( \lambda > 20l \), respectively)


RINGING AND MODELING

• In summary, the second condition for ringing is

<table>
<thead>
<tr>
<th>(Transmission line model necessary)</th>
<th>(RC model enough)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single tone</td>
<td>Ringing possible</td>
</tr>
<tr>
<td></td>
<td>Ringing impossible</td>
</tr>
<tr>
<td>( l &gt; \frac{\lambda}{8} )</td>
<td>( l &lt; \frac{\lambda}{16} )</td>
</tr>
<tr>
<td>( ( l &gt; \frac{\lambda}{10} )</td>
<td>( ( l &lt; \frac{\lambda}{20} )</td>
</tr>
<tr>
<td>Digital pulse</td>
<td>2( t_p &gt; t_r )</td>
</tr>
<tr>
<td></td>
<td>( 2.5( t_p &gt; t_r ) )</td>
</tr>
<tr>
<td></td>
<td>4( t_p &lt; t_r )</td>
</tr>
<tr>
<td></td>
<td>( 5( t_p &lt; t_r ) )</td>
</tr>
</tbody>
</table>

• The former derivations do not take into account losses during line propagation. High losses may eliminate ringing. Therefore, a third condition is necessary for ringing to occur.
RINGING AND MODELING

• Ho et al. found that for when $R \cdot l > 2.5Z_0$, then ringing was negligible and Transmission line modeling not necessary.
• On the contrary, it is considered that when $R \cdot l < 2Z_0$, losses are not enough to eliminate ringing, and TL line modeling is necessary.

<table>
<thead>
<tr>
<th>Condition</th>
<th>Ringing possible (Transmission line model necessary)</th>
<th>Ringing impossible (RC model enough)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single tone</td>
<td>$l &gt; \lambda/8$</td>
<td>$l &lt; \lambda/16$</td>
</tr>
<tr>
<td></td>
<td>($l &gt; \lambda/10$)</td>
<td>($l &lt; \lambda/20$)</td>
</tr>
<tr>
<td>Digital pulse</td>
<td>$2t_p &gt; t_i$</td>
<td>$4t_p &lt; t_i$</td>
</tr>
<tr>
<td></td>
<td>($2.5t_p &gt; t_i$)</td>
<td>($5t_p &lt; t_i$)</td>
</tr>
<tr>
<td>Loss condition</td>
<td>$R \cdot l &lt; 2Z_0$</td>
<td>$R \cdot l &gt; 2.5Z_0$</td>
</tr>
</tbody>
</table>

RINGING AND MODELING

• The conditions for TL line modeling are usually expressed in terms of $L$, $C$ as:

$$\frac{t_r}{2\sqrt{LC}} < l < \frac{2}{R\sqrt{C}}$$

• In summary:

• Ignoring terribly simplifies interconnect extraction and modeling.

- Rd=$Z_0$?
  - no
  - yes

- $R < 2.5Z_0$?
  - no
  - yes

- $t_r < 2t_p$?
  - no
  - yes
**ELECTRICAL MODEL**

- R, L, C, G model parameters can be obtained from:
  - manufacturer’s data,
  - semi-empirical formulas,
  - field simulators or
  - measurements

- This model can be simplified depending on the ringing (in general, frequency) conditions:

**Physical**
- R, L, C, G values obtained from physical descriptions of the interconnect

**Non-physical**
- R, L, C, G values obtained ignoring the physical description of the interconnect

These methods can be grouped in:

- Physical
- Non-physical
NON-PHYSICAL MODELING

1. Individual interconnects are measured (test structures accessed with probes)

2. S-parameters are obtained

3. $Z_0$ and $\gamma$ derived from S-parameters

4. $R$, $L$, $C$, $G$ obtained from $Z_0$ and $\gamma$

\[
X = Z_{0,y} = \frac{R + j\omega L}{\sqrt{(R + j\omega L)(G + j\omega C)}} = R + j\omega L,
\]
\[
Y = \frac{\gamma}{Z_0} = \frac{\sqrt{(R + j\omega L)(G + j\omega C)}}{\sqrt{G + j\omega C}} = G + j\omega C,
\]
\[
R = \text{Re}\left\{\frac{Z_{0,y}}{\gamma}\right\},
\]
\[
L = \frac{\text{Im}\left\{\frac{Z_{0,y}}{\gamma}\right\}}{\omega},
\]
\[
G = \text{Re}\left\{\frac{\gamma}{Z_0}\right\},
\]
\[
C = \frac{\text{Im}\left\{\frac{\gamma}{Z_0}\right\}}{\omega},
\]


- Note that frequency-dependant parameters are obtained
**PHYSICAL MODELING**

- R is the series interconnect resistance
- L is the interconnect inductance
- C is the interconnect capacitance to ground
- G is the conductance to ground

- Parameters may be obtained from formulas or simulation tools.
- Accuracy will depend on the accuracy (phenomena accounted for) of the formulas or simulation tool
- Frequency dependency may be accounted for, or ignored

![Interconnect Modeling Diagram](image)

\[
Y(\omega) = \frac{\omega^2 C_p G_s}{G_s^2 + \omega^2 (C_{ox} + C_s)^2} + j\omega \left( C_p + \frac{C_{ox} G_s^2 + \omega^2 C_{ox} C_s (C_{ox} + C_s)}{G_s^2 + \omega^2 (C_{ox} + C_s)} \right)
\]

\[
Y(\omega) = G(\omega) + j\omega C(\omega)
\]

Note frequency-dependent behavior
PHYSICAL MODELING

- Interconnects on a semiconducting substrate:

\[ Y(\omega) = \frac{\omega^2 C_p G_p}{G_1^2 + \omega^2 (C_{ox} + C_s)^2} + j \omega \left( \frac{C_{ox} G_p^2 \omega^2 C_p G_w (C_{ox} + C_s)}{G_1^2 + \omega^2 (C_{ox} + C_s)^2} \right) \]

- Three frequency regimes are traditionally distinguished according to field penetration in the substrate:

\[ \delta = \sqrt{2 \rho_s / \omega \mu_0} \]

- Slow wave (low frequencies): skin depth larger than substrate thickness; return though the backplane (inductance depends on \( t_{ox} + t_s \))
- Skin depth mode ("medium" frequencies): skin depth smaller than substrate thickness; return through the substrate (inductance depends on \( t_{ox} + \delta \))
- Dielectric mode: (high frequencies, \( \omega \gg \frac{C_{ox}}{t_{ox} + t_s} \), substrate behaves as a dielectric

INTERCONNECT MODELING

- Skin effect: high-frequency currents concentrate at the conductor’s surface

\[ \text{Cross Section High Freq.} \]

- at high frequency, the equivalent cross-section of the interconnect is reduced
- at high frequency, the resistance of the interconnect is increased
- this effect be modeled as a frequency-dependant resistivity \( \rho(\omega) \)

PHYSICAL MODELING

• Proximity effect between two conductors:
  - Important only in close conductors
  - The result is an increase of series resistance (similar to skin-effect) and inductance reduction (loop reduction)


PHYSICAL MODELING

• Interconnects on a semiconducting substrate:
  - L value depends on the current loop, i.e. on the forward path (interconnect) and on the return path
  - Given that currents follow the minimum-impedance path, return current path in the substrate depends on the frequency:
PHYSICAL MODELING

• The combined effect of skin effect, proximity effect and return-path reduction result in a strong frequency-dependency of R and L:

![Graph showing frequency-dependency of R and L](image)

• This frequency-dependency becomes more and more critical as circuits’ frequencies increase.

INTERCONNECT PARAMETERS

• R provided by manufacturer’s data:

\[ R = \rho \frac{L}{t \cdot W} = R_L \frac{L}{W} \]

- Usually the square resistance is provided, together with a temperature coefficient.
- Example for a 0.35 µm technology:

<table>
<thead>
<tr>
<th>METX sheet resistance</th>
<th>min</th>
<th>Typ</th>
<th>max</th>
</tr>
</thead>
<tbody>
<tr>
<td>70 mΩ/sq</td>
<td>120 mΩ/sq</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

\[ R(T) = R(T_0) \left( 1 + TCR (T - T_0) \right) \]
INTERCONNECT PARAMETERS

- $R$ provided by manufacturer's data:

In a straight resistor:

$$R = R_{\text{metal}} \frac{L}{W} = R_{\text{via}} \frac{16W}{W} = R_{\text{via}} 16$$

- Each corner square counts as aprox. 0.56 squares.
- The value extracted depends on the extraction tool.

At the 90 nm node, vias can contribute up to 10% of the critical path delay at the 90 nm node.
INTERCONNECT PARAMETERS

• \( C \) provided by manufacturer’s data:

\[
C = C_{\text{AREA}} + C_{\text{PERIMETER}}
\]

\[
C = \epsilon_{\text{dielectric}} \frac{L \cdot W}{d} + \epsilon_{\text{dielectric}} (2L + 2W) f(t)
\]

\[
= C_{\text{AREA}} \cdot L \cdot W + C_{\text{PERIMETER}} \cdot 2L
\]

• Example for a 0.35 \( \mu \)m technology:

<table>
<thead>
<tr>
<th></th>
<th>min</th>
<th>typ</th>
<th>max</th>
</tr>
</thead>
<tbody>
<tr>
<td>METX area capacitance to well</td>
<td>0.010 fF/( \mu )m(^2)</td>
<td>0.012 fF/( \mu )m(^2)</td>
<td>0.017 fF/( \mu )m(^2)</td>
</tr>
<tr>
<td>METX perimeter capacitance to well</td>
<td>0.032 fF/( \mu )m</td>
<td>0.035 fF/( \mu )m</td>
<td>0.039 fF/( \mu )m</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>min</th>
<th>typ</th>
</tr>
</thead>
<tbody>
<tr>
<td>METX-METX coupling capacitance</td>
<td>0.084 fF/( \mu )m</td>
<td></td>
</tr>
</tbody>
</table>

• Manufacturer may obtain these values from numerical field simulators.
• Note that proximity effects are not taken into account.
INTERCONNECT PARAMETERS

• **R** obtained from closed-form expressions:

  • The common expression for regular resistors works well at low frequencies:
    \[ R = \frac{\rho L}{t \cdot W} \]
  
  • At high frequencies, skin-effects must be added: \( \delta = \frac{2}{\sqrt{\omega \mu \sigma}} \)
  
  • At 1 GHz, \( \delta \sim 2 \mu m \) for copper and \( \delta \sim 2.5 \mu m \) for aluminum
  
  • An expression to include skin-effect is suggested by Lee:
    \[ R_s \approx \frac{L}{W \cdot \sigma \cdot \delta \left( 1 - e^{-\frac{L}{\delta}} \right)} \]

  nevertheless, skin depth is heavily influenced by interconnect geometry and proximity effects, thus expressions for isolated interconnects are often not applicable to real situations.

Also for the case of dog-bone interconnect endings
INTERCONNECT PARAMETERS

• C obtained from closed-form expressions:

• Many papers exist that develop closed-form expressions for interconnect self-capacitance and coupling capacitance. Some have some analytical basis, while others are just fitting formulas to dependencies obtained from a batch of field simulations.

• Probably the best known formulas are from Sakurai:

  "Simple formulas for two- and three-dimensional capacitances"
  Sakurai, T.; Tamaru, K.

\[
C_L = 1.15 \left( \frac{h}{w} \right)^{2.95} \left( \frac{a}{w} \right)^{0.811} \\
C_t = C_{10} + C_{12} \\
C_3 = C_{20} + 2C_{21} \\
(C_{2} = C_{t} + C_{L}) \\
(C_{2} = C_{t} + C_{L})
\]

INTERCONNECT PARAMETERS

• C obtained from closed-form expressions:

• Suggested expressions (note values per unit length):

  "Modeling of interconnect capacitance, delay, and crosstalk in VLSI"  
  Shyh-Chyi Wong; Geo-Yann Lee; Dye-Jyun Ma  

  on-line calculator at:  
  http://www.eas.asu.edu/~ptm/interconnect.html
**INTERCONNECT PARAMETERS**

- \( L \) obtained from **closed-form expressions**:
  - Suggested expressions (note values per unit length):

  \[
  L_c = \frac{Z_0}{2\pi} \ln \left( \frac{L}{w + t} \right) - \frac{1}{2} \left( \frac{0.22(w + t)}{l} \right)
  \]
  \[
  M = \frac{\mu_0}{2\pi} \ln \left( \frac{2L}{d} \right) - 1 + \frac{d}{L}
  \]

- Note non-linearity with length \( l \) (inductance must be calculated for the full length)
- Paper also shows expressions including skin-effect, unequal line lengths, etc…


On-line calculator at: [http://www.eas.asu.edu/~ptm/interconnect.html](http://www.eas.asu.edu/~ptm/interconnect.html)

**INTERCONNECT PARAMETERS**

- \( R, L, C \) obtained from simulations:
  - Independent capacitance and inductance extraction is valid under the quasi-TEM assumption

  - Capacitance
    - Integral Equation Method
      - 2D description
    - Finite Element Method
      - both 2D and 3D
    - Boundary Element method
      - both 2D and 3D
    - PEEC
      - both 3D
  - Inductance
    - Moment
    - Frequency domain
      - S-parameter
    - Time Domain
      - FDTD

  Ex: Raphael, FastCap, FastHenry…

  Ex: Momentum
INTERCONNECT PARAMETERS

• R, L, C obtained from simulations:

  • Finite Element Method (FEM) based on discretization (meshing) of the structures, computation (linearization) of the equations in each sub-cell
  • High-resolution, total geometrical flexibility, but slow…

  • Boundary Element Method (BEM, or MoM) based on directly solving Green’s function given boundary conditions
  • Lower resolution, restricted to stratified layers, but faster…

INTERCONNECT PARAMETERS

• R, L, C obtained from simulations:

  • The problem with inductance calculation is that you must know the return path (inductance depends on the loop)
  • Partial inductance concept: assume that return path for each interconnect segment is at infinity, then calculate partial inductance as magnetic flux through the loop of a victim line to infinity. The total loop inductance can be calculated from the partial inductances of the loop segments.
  • Important: partial inductance has no meaning outside of a loop.

\[ L_{\text{loop}} = \sum_i \sum_j S_{ij} L_{ij, \text{partial}} \quad \text{with} \quad S_{ij} = \pm 1 \]

Where \( S_{ij} = +1 \) for currents in the same direction and \( S_{ij} = -1 \) for currents in the opposite direction.
INTERCONNECT PARAMETERS

• R, L, C obtained from simulations:

• PEEC method (Partial Equivalent Electric Circuit): Each interconnect is divided in a number of filaments of rectangular section. Current in each filament is assumed to be uniform in its cross-section, and partial elements (resistance, capacitances and self and mutual inductances) are calculated.

• Total inductance is calculated from the partial inductances of the bars. This method allows to calculate frequency-dependant inductance and resistance (skin effect is inherently considered).

INTERCONNECT PARAMETERS

• R, L, C obtained from simulations:

• It must be noted that HSPICE simulator includes a simplified version of RAPHAEL 2-D field solver.

• Result are matrices of frequency-independent parameters per unit length.

• Example for three conductors and a reference node:

\[
\begin{align*}
\mathbf{L} & = \begin{bmatrix} L_{11} & \cdots & L_{1n} \\
\vdots & \ddots & \vdots \\
L_{n1} & \cdots & L_{nn} \end{bmatrix}, & \mathbf{C} & = \begin{bmatrix} C_{11} & \cdots & C_{1n} \\
\vdots & \ddots & \vdots \\
C_{n1} & \cdots & C_{nn} \end{bmatrix}, & \mathbf{G} & = \begin{bmatrix} G_{11} & \cdots & G_{1n} \\
\vdots & \ddots & \vdots \\
G_{n1} & \cdots & G_{nn} \end{bmatrix}
\end{align*}
\]

\[
\begin{align*}
\mathbf{R} & = \begin{bmatrix} R_{11} & \cdots & R_{1n} \\
\vdots & \ddots & \vdots \\
R_{n1} & \cdots & R_{nn} \end{bmatrix},
\end{align*}
\]

- \( R_{xy} \) for \( x \neq y \) (no-skin effect)
- \( R_{xy} \) for \( x = y \) (skin effect present)
INTERCONNECT PARAMETERS

• Coupled interconnect models

• The basic method to create a model of an interconnect is to build the model from R, L, C, G basic elements. This is done automatically by parasitic extraction tools.

• Some simulators support also transmission line models; these usually request user-specified R, L, C, G values as inputs parameters

• HSPICE is known to support multi-conductor coupled transmission line model, which includes mutual inductance and capacitance between conductors (as well as skin-effect)

INTERCONNECT EXTRACTION

• Assura™ is the current DRC, LVS and parasitic extractor of Cadence

• Assura-RCX extracts interconnect and substrate parasitics

• Possible to obtain Ronly, Conly, RC, RLC and RLCX interconnect models

• Flexibility to extract models for all, or only selected nets

• Possible to filter out small interconnects segments, R, C and L values
**INTERCONNECT EXTRACTION**

- Interconnects can be subdivided in segments according to specified length (max-length) or frequency criteria.
- Frequency criteria can be specified for nets specified in a list file.

- Capacitances is extracted except for shielded interconnects

- Possibility to use decoupled mode to reduce the number of capacitors (neglect crosstalk effects while preserving the total capacitance value for delay effects)

- Capacitance values can be obtained from built-in field solver
INTERCONNECT EXTRACTION

- Inductances can be extracted in two different modes: PEEC and Return-limited.

- In the PEEC mode, partial self and mutual inductances are extracted for each interconnect segment (for all interconnects within a specified user region), including GND and power.

- In the Return-limited mode, it is assumed that return is through the nearest GND or power lines. Therefore, loops are defined and partial self and mutual inductances are added to compute total self and mutual inductances for each signal interconnect.

- Optionally, heavily doped substrate can also be included as a return path; eddy losses in the substrate are taken into account (the substrate profile must be provided).

- By default, extracted R and L values are frequency independent.

- An optional ladder model can be extracted to account for frequency dependance.