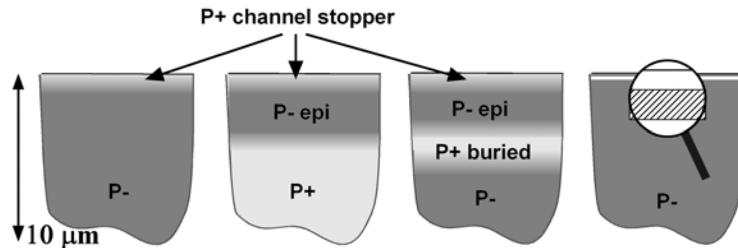
IFSIN

4.- SUBSTRATE MODELING
SUBSTRATE COUPLING

INTRODUCTION

- Types of substrates
- Substrate coupling problem
- Coupling mechanisms
- Modeling
    - Detailed modeling
    - Macromodeling
- Recommended measures

TYPES OF SUBSTRATES



P+ channel stopper

• The IC fabrication process usually creates a surface implant to avoid the appearance of parasitic channels (surface inversion) induced by the lowest level of metalization.

• This implant is commonly known as **channel-stop layer**, has a conductivity about two orders of magnitude higher than the bulk (i.e., ρ~0.1 Ω·cm) and extends about 1 μm deep.

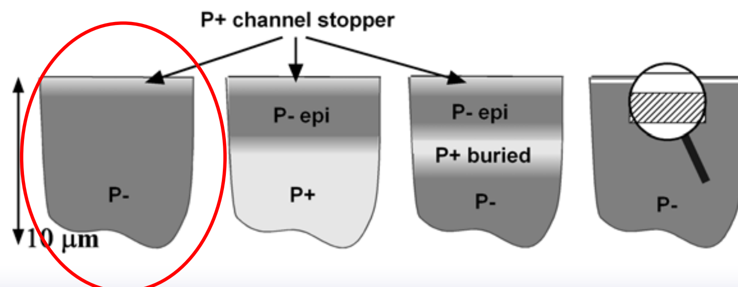
TYPES OF SUBSTRATES

P- or lightly doped or high resistive or RF substrate

• Uniform resistivity between 10 and 20 Ω·cm.

• Usually preferred for analog and RF applications because of their low losses (high Q passive devices).

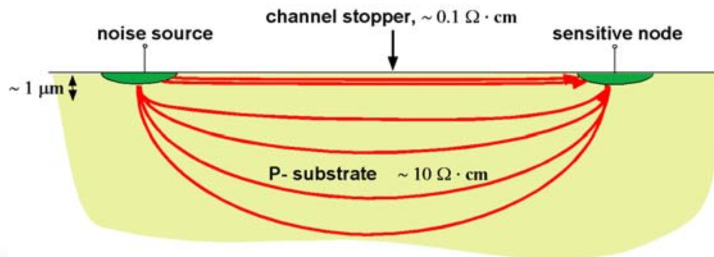
• Higher resistivities (100 to 1000 Ω·cm) are possible, but not common.



TYPES OF SUBSTRATES

P- or **lightly doped** or **high resistive** or **RF substrate**

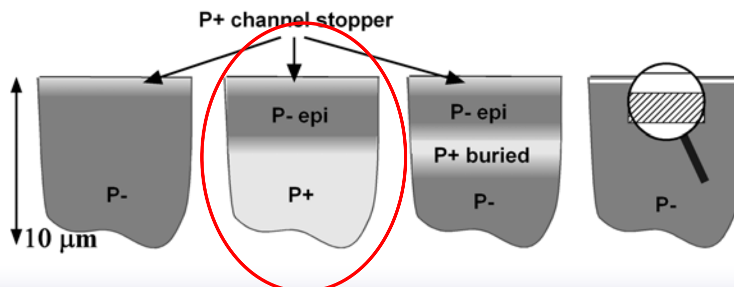
• Currents penetrate and distribute inside the silicon bulk. A distributed 3D modeling is necessary.
• A significant part of the current propagates in the channel stopper, making it necessary to model.
• After a minimum distance, resistance propagates ~linearly as distance increases, thus attenuation increases ~linearly.



TYPES OF SUBSTRATES

P+ or **heavily doped** or **low resistive** or **digital substrate**

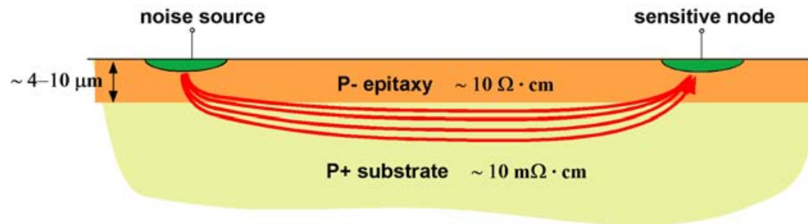
• Bulk (P+ region) resistivity between 10 and 20 mΩ·cm.
• A lightly doped **epitaxial** layer, resistivity between 10 and 20 Ω·cm, is grown on the surface. After processing this layer can be as thin as ~4 µm
• Usually preferred for digital applications because it provides immunity to latch-up



TYPES OF SUBSTRATES

P+ or **heavily doped** or **low resistive** or **digital substrate**

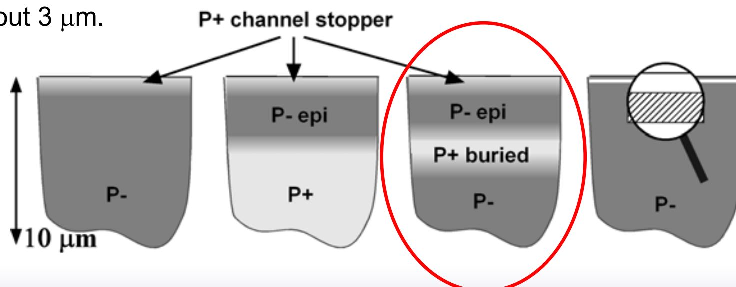
• As a rule of thumb, for distances larger than 4 times the epi-layer thickness, all currents propagate through the P+ bulk.
• Attenuation is produced mainly through the epi-layer. Therefore, negligible attenuation with increasing distance.
• Since no attenuation is produced in the P+ bulk, it is reasonable to model it as a single node.



TYPES OF SUBSTRATES

P+ buried layer on a high resistive substarte

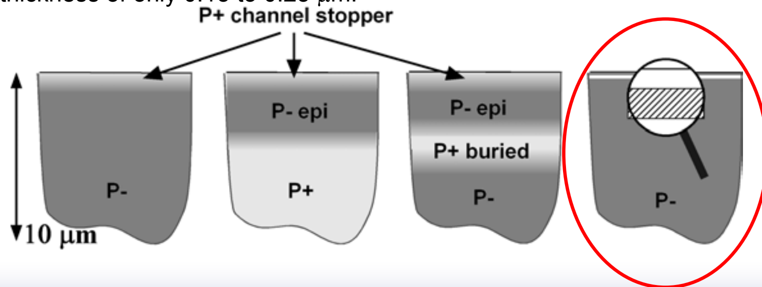
• A compromise between the two former approaches: to start from a highly resistive wafer, and create a conductive buried layer some microns below the wafer surface.
• This way, it is argued that the low-loss advantages of resistive wafers are preserved while preventing latch-up with the buried layer.
• Resistivity of the buried layer is in the order of 10 mΩ·cm with a thickness of about 3 μm.



TYPES OF SUBSTRATES

SOI (Silicon-On-Insulator) substrates

• SOI technology offers better speed-power tradeoff, at the expense of higher cost.
• In the RF / System-on-a-Chip area, SOI is a promising option because of speed and isolation.
• There exist several processes to implement SOI, but the most common one is SIMOX (Separation by IMplanted OXygen). In SIMOX, the buried oxide (BOX) layer may be between 0.1 and 0.4 μm thick, while the silicon on the insulator layer has a thickness of only 0.15 to 0.25 μm.



TYPES OF SUBSTRATES

SOI (Silicon-On-Insulator) substrates

• SOI technology offers ideal DC isolation, but after some frequency threshold the isolation matches that of silicon bulk.
• The threshold is produced then the impedance os the insulator layer matches that of a silicon layer for the same geometry

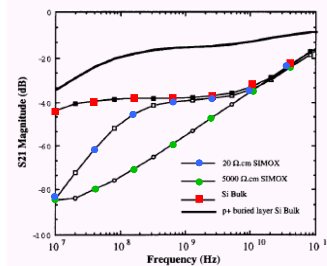
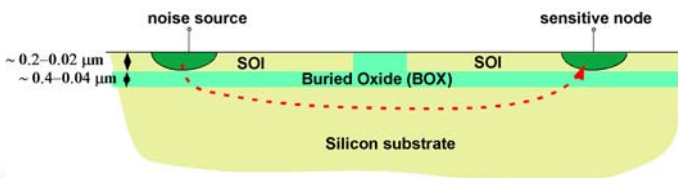
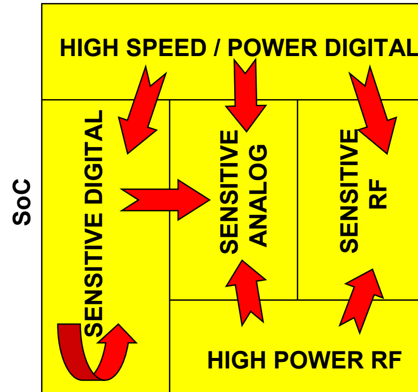


Fig. 2 : Numerical device simulation of crosstalk figures as a function of frequency for the basic test structure on different substrates : bulk with and without buried layer and SOI for 2 different substrate resistivities. The distance between devices is 50 μm.



SUBSTRATE COUPLING PROBLEM

- High-speed signals (digital, power RF) couple to the substrate and reach all elements in the same chip
- It becomes a problem when reaches sensitive analog and RF parts, and affects their performance.
- Relevant problem in SoCs



SUBSTRATE COUPLING PROBLEM

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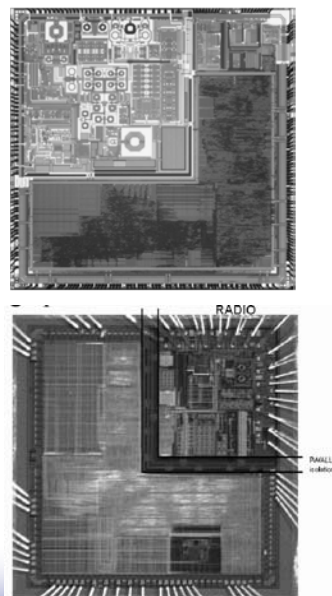
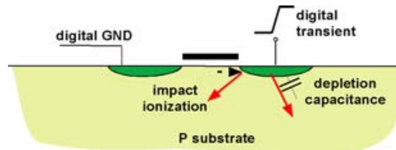


SUBSTRATE NOISE GENERATION

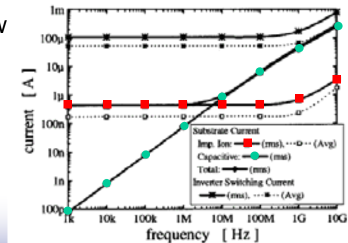
MOSFET transistors

• Capacitive coupling from switching output nodes (drain) of digital gates

$$C_j = \frac{A\varepsilon_{Si}}{\left[\frac{2\varepsilon_{Si}}{q}V_{bi}\left(\frac{1}{N_A}+\frac{1}{N_D}\right)\right]^{1/2}\cdot\left(1-\frac{V_A}{V_{bi}}\right)^m}$$



• Impat ionization current (dominant only at low frequencies[1,2] ,below 10 MHz aprox.)



[1] R.B. Merrill *et al.* "Effect of Substrate Material in Mixed Analog/Digital Integrated Circuits", *IEEE IEDM'94.*

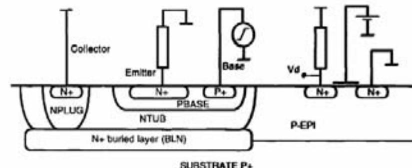
[2] J. Briaire, K. Krisch, "Principles of Substrate Crosstalk Generation in CMOS Circuits", *IEEE Trans on CAD of ICs and Systems*, June 2000.

SUBSTRATE NOISE GENERATION

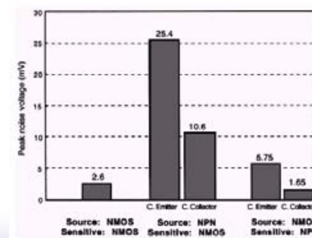
Bipolar transistors

• Capacitive coupling from switching output nodes (collector) of digital gates

$$C_j = \frac{A\varepsilon_{Si}}{\left[\frac{2\varepsilon_{Si}}{q}V_{bi}\left(\frac{1}{N_A}+\frac{1}{N_D}\right)\right]^{1/2}\cdot\left(1-\frac{V_A}{V_{bi}}\right)^m}$$



• Noise importance dewpends a lot on the gate topology (switching collector vs. switching emitter) and collector resistance



[1] J.M. Casalta, X. Aragonès, A. Rubio, "Substrate Coupling Evaluation in BiCMOS Technology", *IEEE J. Solid-State Circuits*, April 1997.

SUBSTRATE NOISE GENERATION

Passive components

• Noise coupled from <u>spiral inductors</u> used in RF blocks (mainly from high-power blocks like LO and PA; coupling to other RF blocks).

• In fact, any large area component (inductor, capacitor, resistor, bonding <u>pads</u> or even long interconnects) will be <u>capacitively coupled</u> to the substrate.

• Depending on the nodes affected, the component will be a *noise injector* or *noise-sensitive.*

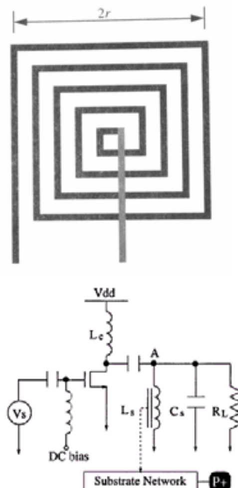


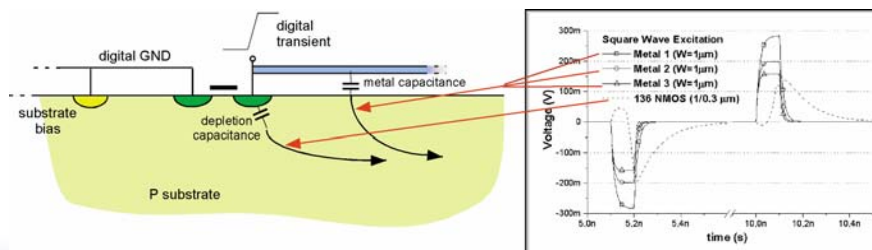
Fig. 10. Schematic of power amplifier for inductor (Ls) substrate noise analysis.

SUBSTRATE NOISE GENERATION

Signal Interconnects

• Switching interconnects may couple (capacitive) disturbances to the substrate.

• Long interconnects may couple as much noise as hundreds MOS transistors



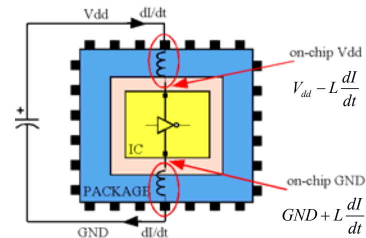
SUBSTRATE NOISE GENERATION

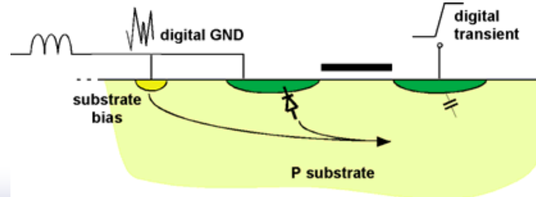
Power-supply lines

• Power-supply switching noise is injected to the substrate by ohmic taps / contacts

• Number of contacts↑↑: The equivalent resistance between a substrate point and on-chip GND may be as low as < 1 Ω !!

• This is the most important noise source in mixed A/D designs!!



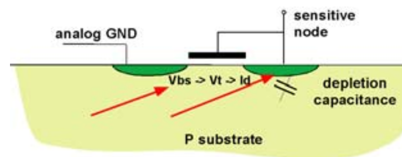


SUBSTRATE NOISE SENSITIVITY

MOSFET transistors

• Capacitive coupling to MOSFET nodes (source, drain)

$$C_j = \frac{A\varepsilon_{Si}}{\left[\frac{2\varepsilon_{Si}}{q} V_{bi}\left(\frac{1}{N_A} + \frac{1}{N_D}\right)\right]^{1/2} \cdot \left(1 - \frac{V_A}{V_{bi}}\right)^m}$$



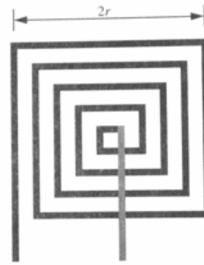
• Body effect (V_T modulation)

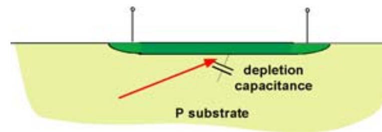
$$V_T = V_{TO} + \gamma\left(\sqrt{2\phi_b - V_{BS}} - \sqrt{2\phi_b}\right)$$

SUBSTRATE NOISE SENSITIVITY

Passive components

• Noise capacitively coupled to spiral inductors used in RF blocks, and in general any large area component (inductor, capacitor, resistor, bonding pads or even long interconnects).



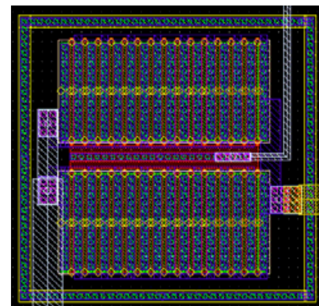


(N-well resistor)

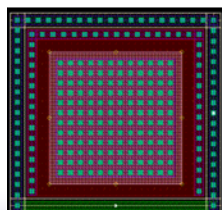
SUBSTRATE NOISE SENSITIVITY

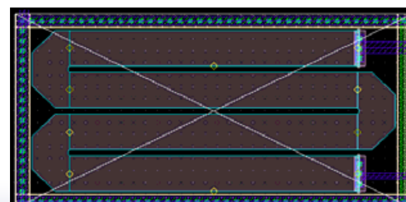
Power-supply lines

• Noise present in the substrate affects analog supply lines (V_{ss}, V_{dd}) used for substrate biasing. This in turn affects the analog signals,



(Ex: large area components (multifingered MOSFET, poly capacitor, snake resistor) enclosed by GND biasing contacts.)





SUBSTRATE COUPLING MODELING

Detailed modeling:

1. Modeling coupling between components and substrate (i.e., modeling all the relevant coupling mechanisms)
2. Modeling the substrate itself (modeling the transmission means)

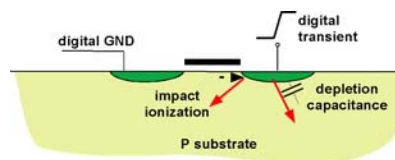
SUBSTRATE COUPLING MODELING

1. Modeling coupling between components and substrate

MOSFET transistors

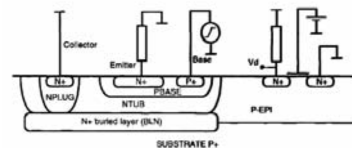
• Both parasitic capacitances and impact ionization are already included in the MOSFET model

• Care must be taken to extract the source/drain areas and perimeters



Bipolar transistors

• Parasitic capacitance already included in the transistor model



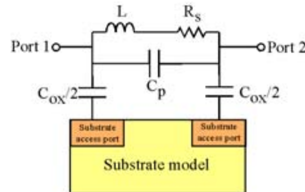
SUBSTRATE COUPLING MODELING

1. Modeling coupling between components and substrate

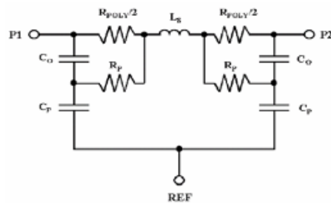
Passive components

• Passive components model should include the coupling capacitances to the substrate.

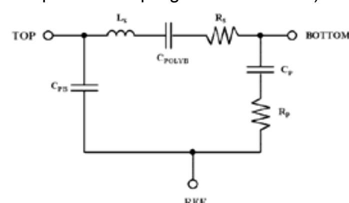
• This may not be the default case, you have to check it !!



(Spiral inductor model including capacitive coupling to the substrate)



(RF poly resistor model including capacitive coupling to the substrate)



(RF capacitor model including capacitive coupling to the substrate)

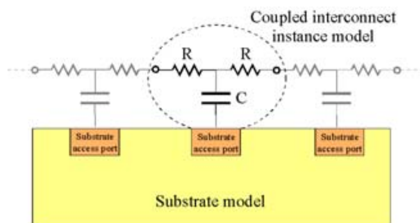
SUBSTRATE COUPLING MODELING

1. Modeling coupling between components and substrate

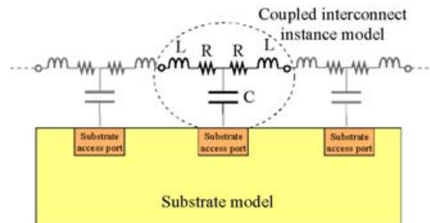
Signal interconnects

• An RC or RLC model coupled to the substrate is desirable.

• This extraction is possible now in Assura-RF, but must be done selectively



(Interconnect RC distributed model coupled to the substrate)



(Interconnect RLC distributed model coupled to the substrate)

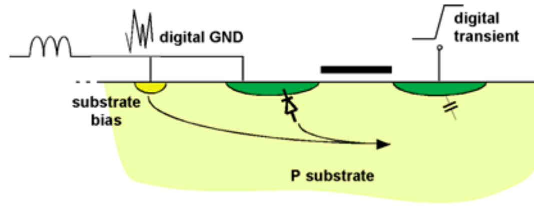
SUBSTRATE COUPLING MODELING

1. Modeling coupling between components and substrate

Power-supply lines

• By default extractors consider substrate and wells as single-node ideal connections to global nodes (gnd! , vdd!)

• This must be replaced by a model, and biasing taps locations identified.

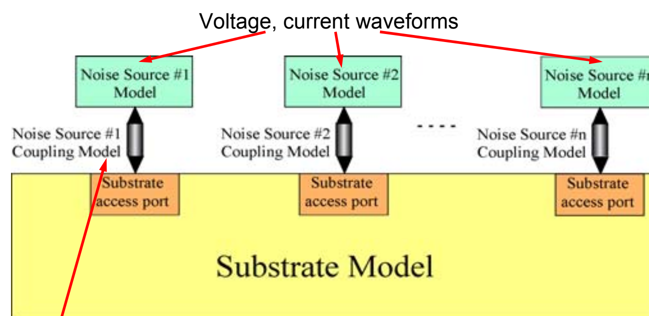


SUBSTRATE COUPLING MODELING

1. Modeling coupling between components and substrate

• All the noisy or sensitive devices must be coupled to a substrate model

• Locations for the interaction between devices (including substarte taps) and substarte are known as *access ports*

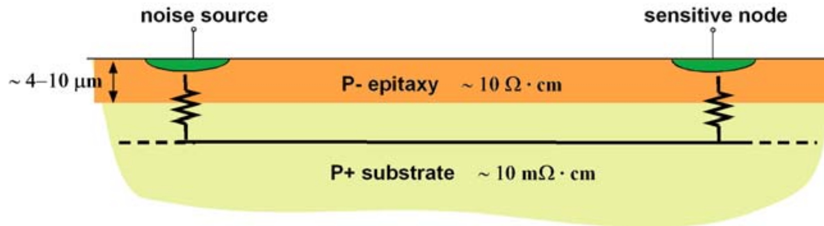


SUBSTRATE COUPLING MODELING

2.- Modeling the substrate itself

• For digital substrates, the P+ bulk can be modeled as a single node, and it is enough to obtain the resistance between each access port and the bulk through the epitaxial layer.

• This resistance can be obtained by using simulators, or with semi-empirical analytical formulas [1,2,3]



1 K. Joardar, "A Simple Approach to Modeling Cross-Talk in Integrated Circuits", *IEEE J. Solid-State Circuits*, October 1994.
2 A.J. van Genderen *et al*., "Fast Computation of Substrate Resistances in Large Circuits", *Proc. IEEE EDTC'96.*
3 N. Masoumi *et al.,*"Fast and Efficient Parametric Modeling of Contact-to-Substrate Coupling", *IEEE Trans., CAD of ICs and Systems*, November 2000.

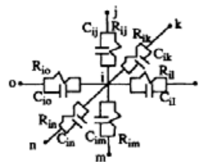
SUBSTRATE COUPLING MODELING

2.- Modeling the substrate itself

• For the rest of substrates, a distributed 3D modeling is necessary.

• The nature of the model depends on the frequency and technology characteristics:

$$J = (\sigma + j\omega\varepsilon) E$$



Example: $\sigma = 10\ S/m\ for\ \rho = 10\,\Omega cm$ $\qquad \omega\varepsilon = 6.51^{-10}\ f\ S/m$

$$\omega\varepsilon = 0.1\sigma \quad @ \quad 1.5\ GHz$$
$$\omega\varepsilon = 0.2\sigma \quad @ \quad 3\ GHz$$
$$\omega\varepsilon = 0.5\sigma \quad @ \quad 7.5\ GHz$$
$$\omega\varepsilon = \sigma \quad @ \quad 15\ GHz$$

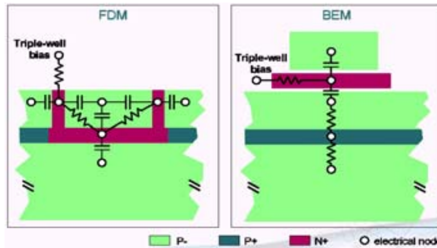
SUBSTRATE COUPLING MODELING

2.- Modeling the substrate itself

• The substrate model will then consist of a mesh of R//C or C connected to the *access ports.*

• Two main methods exist to extract the substrate model:
  • *Finite Difference Method (FDM)*
  • *Boundary Element Method (BEM)*

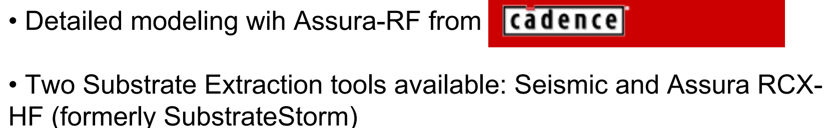
FDM:
• Full discretization of the substrate needed (huge matrices)
• Accuracy depends strongly on discretization
• Sparse matrices (fast matrix computations). Mesh reduction techniques available
• May deal with any technology; horizontal & vertical variations



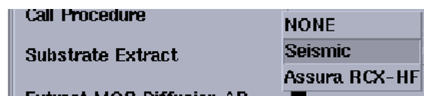
BEM:
• Only discretization of ports is needed (smaller matrices). Only port to port relationship modeled
• Dense matrices (slow matrix computations)
• Substrate is treated as a few number of uniform layers (no possible horizontal variation)

SUBSTRATE COUPLING MODELING

2.- Modeling the substrate itself

• Detailed modeling wih Assura-RF from 

• Two Substrate Extraction tools available: Seismic and Assura RCX-HF (formerly SubstrateStorm)

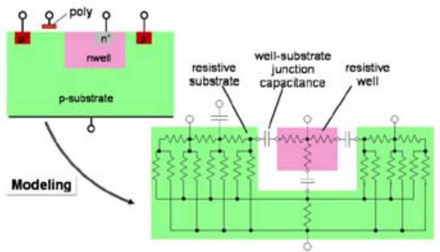


• Seismic:
  • Boundary Element Method default (faster), changes to Finite Differences Method where needed (accuracy or wells/trenches)
  • Supports adding macromodels for noise computation at floorplan or chip level

SUBSTRATE COUPLING MODELING

2.- Modeling the substrate itself

- Assura RCX-HF or SubstrateStorm
  - Finite Differences Method (accurate, slow…)
  - Extracted model is a subcircuircuit consisting of a mesh of R//C or R elements (depending on the desired frequency)
    - (A RC reduction algorithm can be applied to simplifiy the extracted net; this is a mathematical algorithm, individual Rs and Cs will no longer have a physical meaning, although the subckt behavior remains the same; do not confuse this option with R//C or R extraction).
  - The extracted view of the circuit including the substrate model can then be simulated (.TRAN, .AC…).



Example: extraction of three NMOS and a ptap

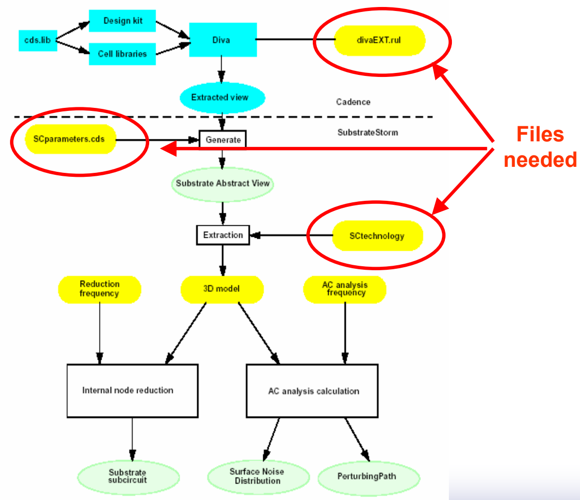
```
.SUBCKT SCav_extracted gnd! SCbk1 SCbk2 SCbk3

R1 SCbk3 gnd! 17673.5
R2 SCbk1 gnd! 51304.8
R3 SCbk2 gnd! 52170.3
R4 SCbk1 SCbk3 42991.5
R5 SCbk2 SCbk3 43866.1
R6 SCbk2 SCbk1 23335.6

.ENDS SCav_extracted
```


SUBSTRATE COUPLING MODELING

2.- Modeling the substrate itself

- Assura RCX-HF or SubstrateStorm flow :

1. DRC and LVS must be passed first; substarte parasitics are extracted after interconnect parasitics.
2. Devices, taps, (interconnects) and regions are identified in the layout
3. A substrate resistivity vertical profile is attached below each device, tap, region…
4. Surface discretization, R (C) computation, optional RC reduction, subckt creation



Files needed

SUBSTRATE COUPLING MODELING

2.- Modeling the substrate itself

• Files needed: **extract.rul**

• File that controls the layout extraction process. Must be provided by the silicon foundry.
• Identifies devices by logic functions (and, or, not) applied on layers

```
pgate = geomAnd( poly pdiff )
ngate = geomAnd( poly ndiff )
pimp = geomAndNot( pdiff poly )
nimp = geomAndNot( ndiff poly )
psd = geomAnd( nwell pimp )
nsd = geomAnd( pwell nimp )
 extractDevice( ngate (poly "G") (nsd "S" "D") (pwell "B")
"nmos4 ivpcell analogLib" )
 ngateWidth = measureParameter( length ( ngate coincident
poly ) 0.5e-6 )
 ngateLength = measureParameter( length ( ngate inside poly
) 0.5e-6 )
 saveProperty( ngate "model" "nfet" )
 saveParameter( ngateWidth "w" )
 saveParameter( ngateLength "l" )
 saveRecognition( ngate "device" )
```


SUBSTRATE COUPLING MODELING

2.- Modeling the substrate itself

• Files needed: **extract.rul**

• File that controls the layout extraction process. Must be provided by the silicon foundry.
• Identifies devices by logic functions (and, or, not) applied on layers

• For substrate modeling, an especial version of *extract.rul* must be provided that includes all relevant layout information for the substrate extraction:
  • Identification of taps, (saved as TIE device)
  • Identification of regions (n-well, triple well…)
  • Saving recognition shapes for any access port (device) and region

SUBSTRATE COUPLING MODELING

2.- Modeling the substrate itself

• Files needed: **SCtechnology**

• File that contains substrate resistivity data. Must be provided by the silicon foundry.

• Defines a vertical resistivity profile for each region and device type

• Simplifies the substrate conductivity profile to a reduced number of layers

• Calculates capacitances (ex: well capacitance)

SUBSTRATE COUPLING MODELING

2.- Modeling the substrate itself

• Files needed: **SCparameters.cds**

• File that links extracted data (devices, taps, and regions) to each vertical resistivity profile , and model nodes to access ports

```
snaGeneration = '(
    ( ( "ntap"  "net" ) "nwell"   "contact"  "Resistive"  "metal1" "Unique" 1 -1 1 0 )
    ( ( "ptap"  "net" ) "default" "contact"  "Resistive"  "metal1" "Unique" 1 -1 1 0.2 )
)
```

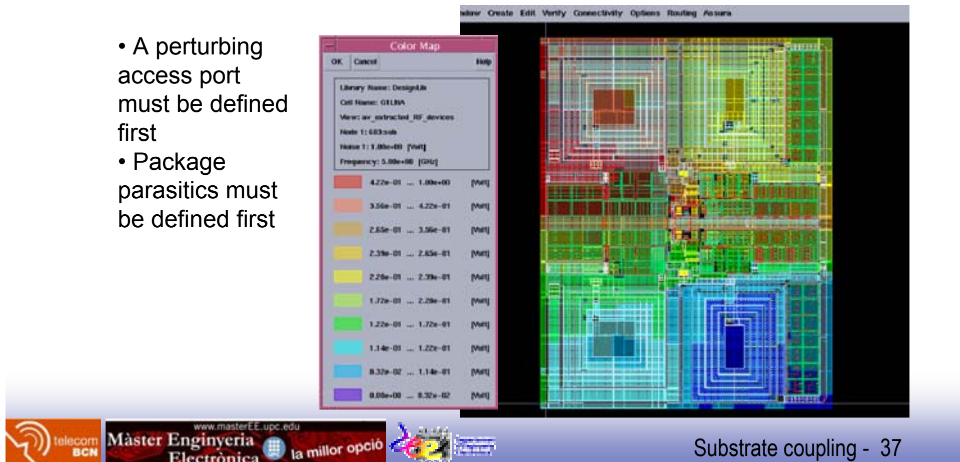
```
snaSelection = '(
  ( "nmos4" nil (( "B" )( "S"  "D" )( "G" )) "default" "channel"  "Resistive"  "device"
"Unique" 1e4 -1 0 0  "new" )
  ( "pmos4" nil (( "B" )( "G" )( "S"  "D" )) "nwell" "channel" "Resistive"  "device"
"Unique"  1e4 -1 0 0 "new" )
  ( "nfet"  nil (( "B" )( "S"  "D" )( "G" )) "default" "channel" "Resistive"  "device"
"Unique" 1e4 -1 0 0 "new" )
  ( "pfet"  nil (( "B" )( "G" )( "S"  "D" )) "nwell" "channel" "Resistive"  "device"
"Unique" 1e4 -1 0 0 "new" )
  ( "cap"  nil (( "MINUS" )( "PLUS" )) "default" "default"  "Capacitive" "poly"  "Unique"
1e4 -1 0 0 "inline" )
```

```
snaRegions='(
( ( "CNW"  "net" ) "nwell" ( ( 3.0 "VDD" ) ) )
( ( "CPW"  "net" ) "pwell" ( ( 0.0 "VSS" ) ) )
( ( "CTW"  "net" ) "triplewell" ( ( 0.0 "VSS" ) ( 3.0 "VDD" ) ) )
)
```

SUBSTRATE COUPLING MODELING

2.- Modeling the substrate itself

- Optional feature: **.AC analysis**
  - An .AC analysis can be applied to the .subckt generated to calculate the surface noise distribution



SUBSTRATE COUPLING MODELING

Assura RCX-HF limits:

1. Skin-effect not considered (probably not necessary)

$$T_{skin} = \sqrt{\frac{\rho}{\pi \mu f}}$$

$$for\ \rho = 10\Omega cm,\ \mu = 4\pi 10^{-7}\ H/m$$
$$for\ \rho = 10\,m\Omega cm,\ \mu = 4\pi 10^{-7}\ H/m$$

frequency	T_{skin} in P-	T_{skin} in P+
3 GHz	2906 µm	92 µm
7.5 GHz	1838 µm	58 µm
15 GHz	1300 µm	42 µm
20 GHz	1125 µm	36 µm

2. Still deficient solution for interaction between RLC interconnect models and substrate

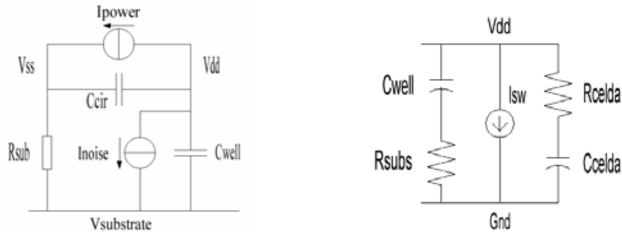
3. Bottleneck: Large .subckt size, huge simulation time (inherent to approach)

SUBSTRATE COUPLING MODELING

Macromodeling:

• Approach consisting on replacing the large digital noisy circuits by equivalent circuit with reduced number of elements and access ports

1.- Replace each digital gate or circuit by a reduced equivalent circuit



Possible equivalent cicuits for a digital gate. In the right circuit, only power-supply noise generation is considered.

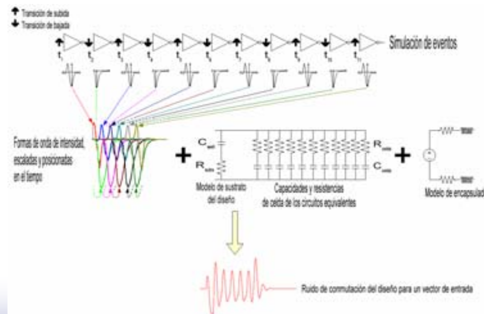
SUBSTRATE COUPLING MODELING

Macromodeling:

2.- Obtain switching information (time instant, input vector) from an event simulation

3.- Compose macromodel and total current waveforms

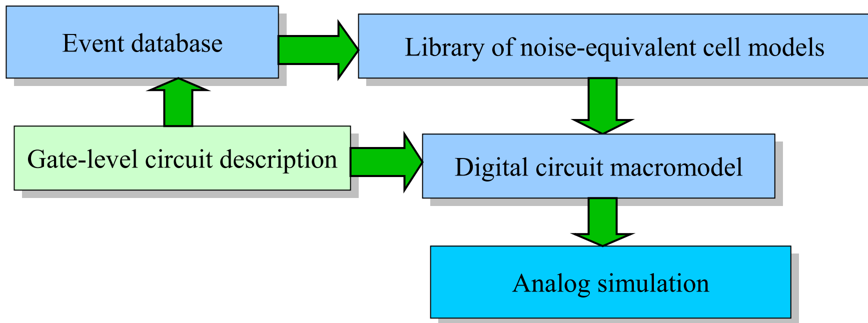
4.- Simulate together with package model, substrate model and sensitive circuit model.



SUBSTRATE COUPLING MODELING

Macromodeling:

Equivalent circuits for each cell type can be generated in a library generation phase :



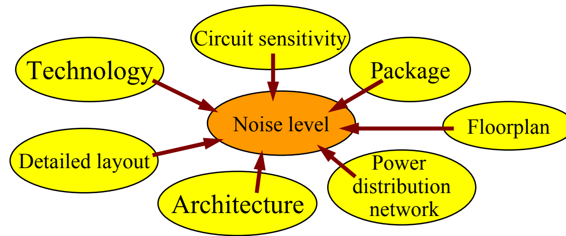
SUBSTRATE COUPLING MODELING

Macromodeling:

- Macromodeling approach developed by several universities
- Now included in commercial tool WaveIntegrity™ (release fall 2006)

- Includes modeling of coupling between interconnects, package and substrate
- Can generate macromodels for IPs
- Can increase accuracy as design frow goes on

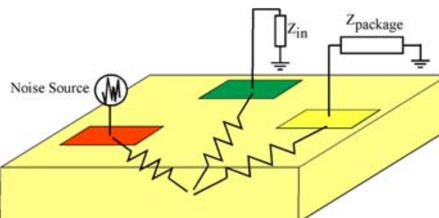
RECOMMENDED MEASURES



- Many factors influence noise coupling
- Therefore, there is no single recipe valid for all situations, all circuits
- An analysis must be performed for each circuit to determine
  - Main noise generators (aggressors)
  - Coupling paths
  - How noise affect sensitive circuit

RECOMMENDED MEASURES

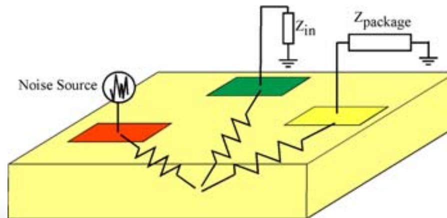
- An analysis must be performed for each circuit to determine
  - Main noise generators (aggressors)
    ⇒ implement measures to reduce noise generation
  - Coupling paths
    ⇒ implement measures to increase isolation between noisy and sensitive circuitry
  - How noise affect sensitive circuit
    ⇒ implement measures to become less sensitive to noise



RECOMMENDED MEASURES

- Main noise generators (aggressors)
  - ⇒ implement measures to reduce noise generation

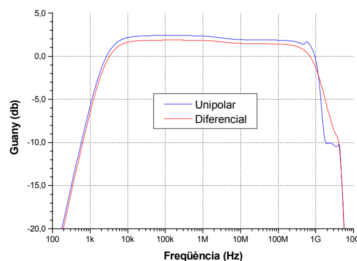
- Techniques aimed to reduce SSN (decoupling caps, staggered switching, clock modulation, current-mode logics…)
- Package selection, careful pin assignment, minimization of parasitics of GND, Vdd pins, low-parasitics on-chip power distribution
- Isolate input (clock) pads from substrate



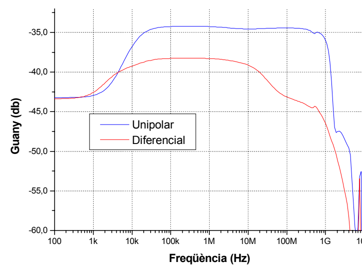
RECOMMENDED MEASURES

- How noise affect sensitive circuit
  - ⇒ implement measures to become less sensitive to noise

- Differential analog processing
  - Cancels out common-mode noise
  - Also less sensitive to noise coupled in the circuit
  - Example: Differential vs. Single-Ended amplifier



Same response to input



6 dB difference in isolation of substrate noise

RECOMMENDED MEASURES

• How noise affect sensitive circuit

⇒ implement measures to become less sensitive to noise

• Isolate sensitive analog *components* from substrate

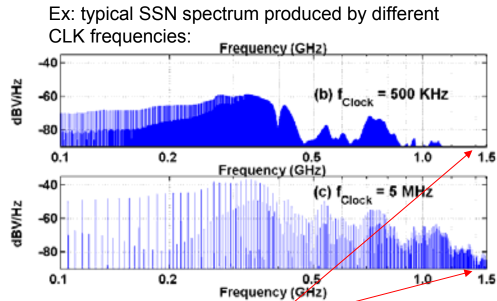
• Bias substrate according to sensitivity to body-effect, power-supply noise

• Stagger analog signal and digital noise

• In time domain (sampled circuits)

• In frequency domain (RF receivers) (works unless the circuit is non-linear)

Ex: typical SSN spectrum produced by different CLK frequencies:



Allocate channel where there is no noise

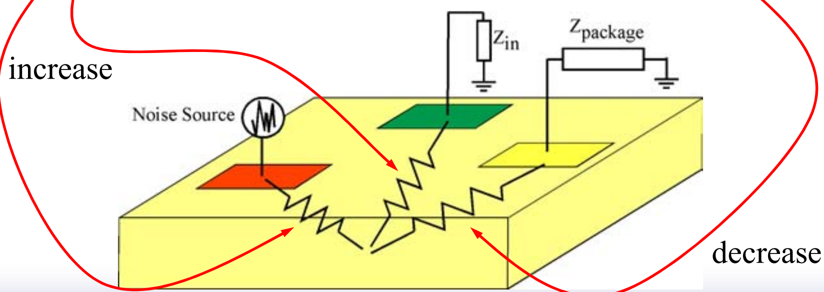
RECOMMENDED MEASURES

• Coupling paths

⇒ implement measures to increase isolation between noisy and sensitive circuitry

a) Isolate noise source and sensitive circuitry

b) Sink noise to ground before reaching the sensitive circuitry



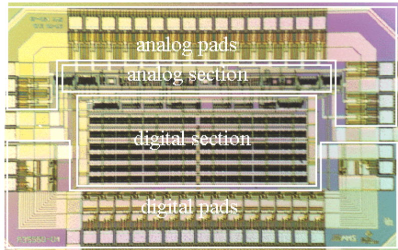
RECOMMENDED MEASURES

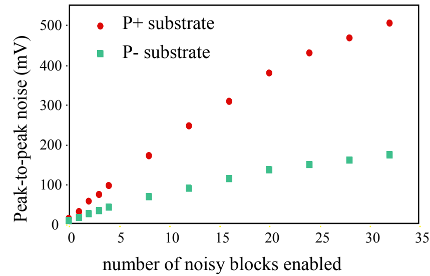
• Coupling paths

⇒ implement measures to increase isolation between noisy and sensitive circuitry

a) Isolate noise source and sensitive circuitry

• Choose high resistive substrates





Ex: Measurements on a mixed A/D test IC, DIP48 package

RECOMMENDED MEASURES

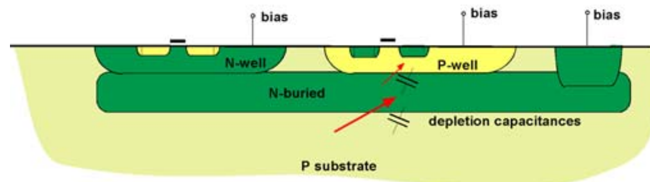
• Coupling paths

⇒ implement measures to increase isolation between noisy and sensitive circuitry

a) Isolate noise source and sensitive circuitry

• "cut" propagation through surface conductive layers (technology may offer oxide trenches)

• Isolate in triple wells (valid up to a frequency threshold)



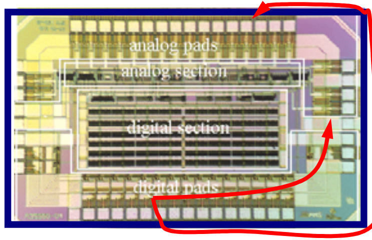
RECOMMENDED MEASURES

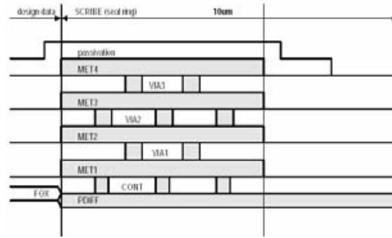
• Coupling paths

⇒ implement measures to increase isolation between noisy and sensitive circuitry

a) Isolate noise source and sensitive circuitry

• Identify other possible propagation paths





Conduction through the scribe line

RECOMMENDED MEASURES

• Coupling paths

⇒ implement measures to increase isolation between noisy and sensitive circuitry

a) Isolate noise source and sensitive circuitry

• Identify other possible propagation paths

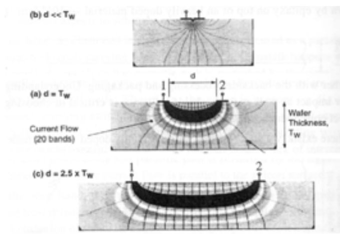


Figure 10: Substrate current flow in a lightly doped wafer with non-conductive epoxy on the backside

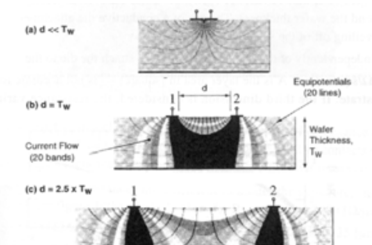


Figure 11: Substrate current flow in a lightly doped wafer with conductive epoxy on the backside

Conduction through the chip backside

[1] F. Clement, "Technology Impacts on Substrate Noise", in *Analog Circuit Design*, Kluwer 1999.

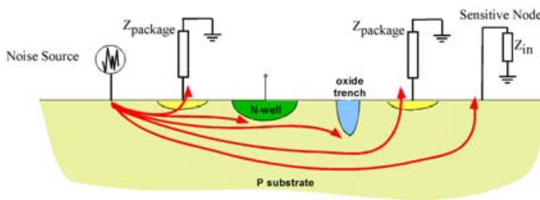
RECOMMENDED MEASURES

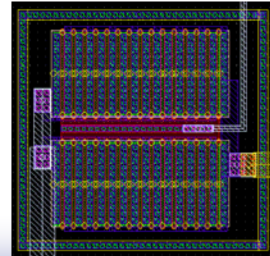
• Coupling paths

⇒ implement measures to increase isolation between noisy and sensitive circuitry

b) Sink noise to ground before reaching the sensitive circuitry

• Enclose sensitive circuits in guard rings connected to low-impedance GND
(Exclusive GND connection for substrate is called Kelvin grounding)





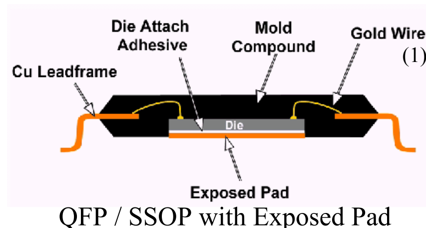
RECOMMENDED MEASURES

• Coupling paths

⇒ implement measures to increase isolation between noisy and sensitive circuitry

b) Sink noise to ground before reaching the sensitive circuitry

• Derive noise to GND through the chip backside



QFP / SSOP with Exposed Pad

[1] Amkor Technologies datasheets, www.amkor.com