2. Crosstalk reduction and shielding techniques

Crosstalk reduction
- Technology
- Layout, driver sizing
- Tolerant circuits

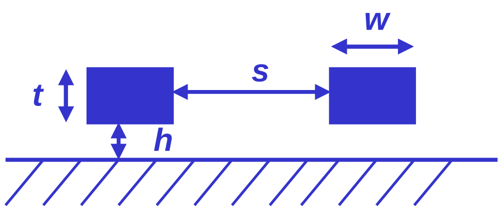
Shielding

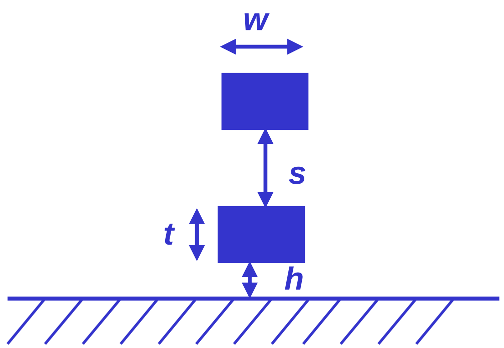
3. References

Crosstalk reduction: technology

There are four sides to consider to reduce the effects of crosstalk:

- Technology
- Layout, driver sizing
- Design tolerance





Approximation

$$C_L \approx \varepsilon_{OX} \frac{lw}{h}$$

$$C_C \approx \varepsilon_{OX} \frac{lt}{s}$$

$$\Delta V \approx \frac{V_{DD}}{1 + \frac{C_L}{C_C}}$$

$$\frac{C_L}{C_C} \approx \frac{ws}{ht}$$

$w \uparrow$, $h \downarrow$ → **delay**

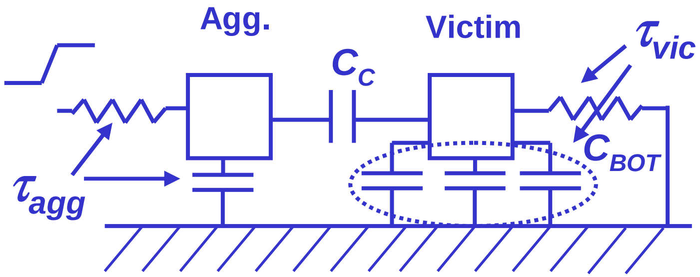
$s \uparrow$ → **area**

$t \downarrow$ → **technology**

Crosstalk reduction: layout

Scenarios (ITRS05)

	2007	2010	2013	
Local wiring pitch	156	90	64	[nm]
Intermediate wiring pitch	167	90	64	[nm]
Global wiring pitch	250	135	96	[nm]
Local wiring aspect ratio	1.7	1.8	1.9	t/w
Intermediate wiring aspect ratio	1.6	1.7	1.8	t/w
Global wiring aspect ratio	2.1	2.3	2.4	t/w



Simple model. Not capture distributed effects.
Wire resistance lumped with driver resistance.

(Ho01)

$$\Delta V = \frac{V_{DD}}{1+\frac{C_{BOT}}{C_C}} \cdot \frac{1}{1+\frac{\tau_{agg}}{\tau_{vic}}}$$

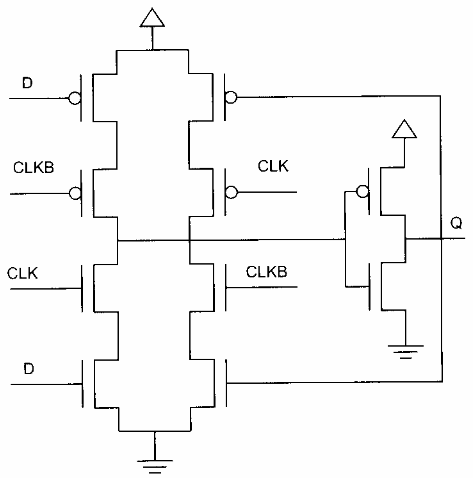
Ratio of driver strengths

- Line width → increases C_{BOT}
- Distance and screening → decreases C_C
- Driver strength → $\frac{\tau_{agg}}{\tau_{vic}} = 2 \text{ to } 4$

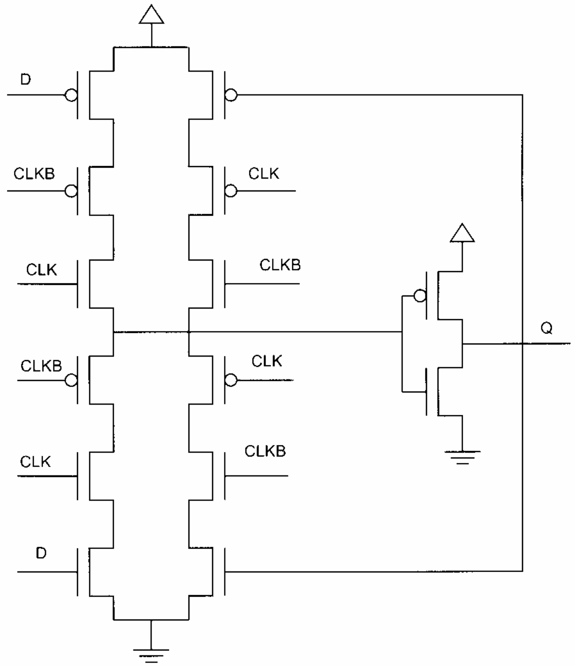
Small influence for long interconnects

Crosstalk tolerant design: example

CLK = 0 transparent state, CLK = 1 latch state
CLKB = nCLK



Conventional latch



Crosstalk tolerant latch [Rubio92]

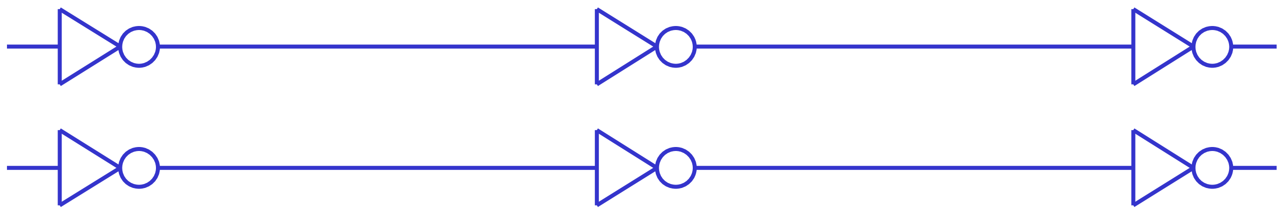
CLK = 0 (CLKB=1) and D goes to 0 while the latch stores a 1. CLK and CLKB have a positive glitch, the latch can store a wrong "0"

Crosstalk reduction: length and number of aggressors

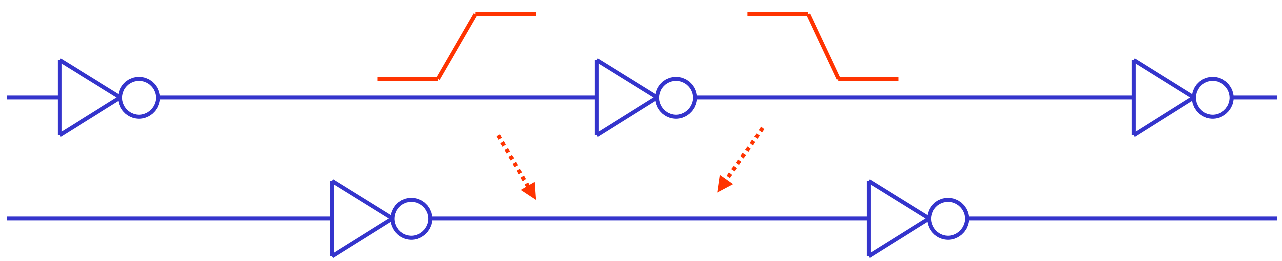
Crosstalk increases with number of aggressors, but tends to saturate with length

Arbitrary units

Crosstalk reduction: repeater insertion



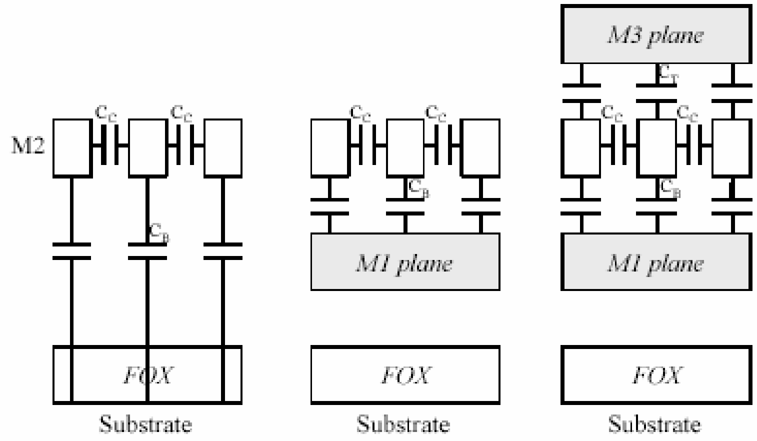
Insertion of repeaters decrease crosstalk



Interleaved repeaters gives a further reduction

Optimization for delay and consumption

Shielding: crosstalk peak noise



Arbitrary units

Planes are ideal conductors at zero potential

2, 4 or 6 aggressors equally distributed at both sides of the victim line

Worst case: same transition in all aggressors

Shielding: propagation delay

- Worst case delay: opposite transitions in victim and aggressors (2)
- Typical case delay: only transition in victim line
- Best case delay: same transition in all lines

Shielding: delay noise

Delay noise = worst case delay – best case delay

Shielding: conclusions

Highest robustness: bus with top and bottom planes and wider spacing (at cost of lower performance)

Several basic references on crosstalk

- F. Moll, M. Roca, *Interconnection Noise in VLSI Circuits*, Kluwer 2004
- C.R. Paul, *Analysis of Multiconductor Transmission Lines*, Wiley 1994
- T. Sakurai, "Closed-Form Expressions for Interconnect Delay, Coupling and Crosstalk in VLSI's", *IEEE Transactions on Electron Devices*, Vol 40, No 1, January 1993, pp. 118-124
- J.A. Davis, J.D. Meindl, "Compact Distributed RLC Interconnect Models – Part I: Single Line Transient, Time Delay, and Overshoot Expressions", *IEEE Transactions on Electron Devices*, Vol 47, No 11, November 2000, pp. 2068-2077.
- J.A. Davis, J.D. Meindl, "Compact Distributed RLC Interconnect Models – Part II: Coupled Line Transient Expressions and Peak Crosstalk in Multilevel Networks", *IEEE Transactions on Electron Devices*, Vol 47, No 11, November 2000, pp. 2078-2087.
- A. Deutsch, G. V. Kopcsay *et al*., "When are Transmission-Line Effects Important for On-Chip Interconnections?", *IEEE Transactions on Microwave Theory and Techniques*, Vol 45, No 10, October 1997, pp. 1836-1846
- International Technology Roadmap for Semiconductors, Edition 2005, http:// www.itrs.net
- R. Ho, K.W. Mai, M. A. Horowitz, "The Future of Wires", *Proceedings of the IEEE*, Vol 89, No 4, April 2001, pp. 490-504