Implementation of Components and Circuits

- Fundamental concepts
- Examples

Outline

- Floorplan
- Layout vs. Schematic: origin of differences
  - Fabrication
  - Design
- Design rules
- Layout of large area components
- Layout for matching
- Effects of Layout on IC reliability
- Layout for reliability
Floorplan

- Sketch of the layout
- Estimation of the IC area
- Technology dependent
  - List of components – subcircuits
  - View
  - Library - models
- Physical layers available
- Components with multiple physical implementations
  - Resistors
  - Capacitors
  - Bipolar transistors
  - Power components
- Pad limited vs. Core limited designs

Example of components: bipolar transistor

- CMOS Parasitic Vertical, 0.35
- CMOS Parasitic Lateral, 0.35
- Vertical BiCMOS, 0.35
- Vertical CMOS, 0.25
Example of components: Resistor

- N Diffusion resistor
- 5 KΩ
- W = 3 microns
- L = 206 microns

Designing a layout: CAD Tools

- Layout design facilities in nowadays CAD Tools:
  - Library of component's layout (Design Kit)
  - Automatic layout generation (Place & route)
  - Layout vs. Schematic
  - Rules checking
  - Extractor and layout simulation
- Is the proposed layout a good layout?
- Identification of weak points. Suggestion of modifications.
Differences between layout and Circuit (I)

- Fabrication process limitations
  - Lateral diffusion
  - Etching under protection
  - Boundary dependent etching
  - Three-dimensional effects
    - Chemical Mechanical Polishing (CMP)
    - Surface topography
- Errors and limitations
  - Mask productions
  - Mask alignement

Differences between layout and Circuit (II)

- Absolute accuracy of physical parameters
  - Controlled at technological level
  - Simulation: Process variation
- Relative inaccuracies of physical parameters
  - Gradients, local variations
    - Matching between components
  - Controlled at technological level
  - Compensated with suitable layout techniques

\[
\frac{\sigma^2(\beta)}{\beta^2} = \frac{A^2}{WL} + S^2 \beta D^2
\]

\[
\sigma^2(V_f) = \frac{A^2}{WL} + S^2 V_f^2 D^2
\]
Differences between layout and Circuit (III)

- Gradients of physical magnitudes
  - Pressure
    - Package dependent
    - Crystal orientation dependent
  - Temperature
  - Compensated with suitable layout strategies

---

Differences between layout and Circuit (IV)

- Parasitic coupling
  - Capacitive coupling
  - Couplings through the power supply
  - Couplings through the substrate
- Parasitic resistances
  - Contacts
  - Interconnect
- Compensated with suitable layout techniques
Design rules: Limitations of Mask production and alignment

Example: Poly 1

Example of design rules for POLY 1

- PO.W.1a
  - Minimum gate length of PMOS
- PO.W-2a
  - Minimum gate length of NMOS
- PO.W.3
  - Minimum POLY1 width for interconnect
- PO.S.1
  - Minimum POLY1 spacing
- PO.C.1
  - Minimum POLY 1 to DIFF spacing
- PO.C.2
  - Minimum DIFF extension of GATE
- PO.O.1
  - Minimum POLY1 extension of GATE
Design of large area components

- Bended structures
- MOS TRANSISTORS
  - Multiple contacts to minimize serial resistance
    - No big contacts!!!
  - Metal out active area
  - “staked” structures
    - Lower parasitic capacitances
    - Lower area
  - Analogue applications
    - Avoid minimum size

Design of Large area components

- Resistances
  - Bended structures
  - Dummy structures
  - 45 degrees (avoid non laminar current flow)
  - Dummy structures
  - Contacts
    - Current in the same direction
    - Multiple contacts
  - Piezoresistive effect

Resistor: 5K, 275x3 sq microns.
Example of “good” and “bad” layout
Layout for matching

- Devices with the same orientation
  - Current in the same direction
- Gradients increase with distance
- Same orientation towards physical gradients

- Interdigitated structures

Mos transistors M1 and M2

Resistors R1 and R2
Layout for matching

- **Common centroid:**

  - Coincidence
    - Centroids of matched devices should coincide
  - Symmetry
    - Array symmetric around both X and Y axis
  - Dispersion
    - Segment of each device distributed throughout the array as uniformly as possible
  - Compactness
    - Ideally: array should be square
Rules for matching

- Same W and L: Vary M
- Capacitors
  - Multiple M of a capacitance reference \( C_R \)
- Ms: Even (factors of 4!!)
- Clean and balanced routing
  - IR drops
  - Parasitic capacitance and couplings
  - Kelvin connections
- Avoid minimum sizing and overlapping
- Use dummy structures

Layout Strategies for circuit reliability (I)

- Electromigration
  - Electromigration is the transport of material caused by the gradual movement of the ions in a conductor due to the momentum transfer between conducting electrons and diffusing metal atoms
  - Dependent on:
    - Temperature
    - Current density
    - Conductor Shape
Layout Strategies for circuit reliability (II)

- **Latch-up**
  - A *latchup* is the inadvertent creation of a *low-impedance* path between the power supply rails of an electronic component, triggering a *parasitic device*, which then acts as a short circuit, leading to ceasement of proper function of the part and perhaps even its destruction with the overcurrent.

Layout Strategies for circuit reliability (III)

- **Antenna Effects or Plasma-Induced damage**
  - The "Antenna Rules" deal with process induced gate oxide damage caused when exposed polysilicon and metal structures, connected to a thin oxide transistor, collect charge from the processing environment (e.g., reactive ion etch) and develop potentials sufficiently large to cause Fowler Nordheim current to flow through the thin oxide.

- **ESD**
  - Electrostatic Discharge
  - Damage in dielectrics due to IC manipulation
Layout Strategies for circuit reliability (IV)

- CMP
  - Chemical Mechanical Polishing or Chemical Mechanical Planalization
  - Removal any irregular topography
  - Surface within the depth of field of a photolithography system.

Layout for reliability: CMP

- Example: MOSIS 0.25 (TSMC)
- Design rules:
  - Minimum % coverage of Metal layers
  - Polysilicon layers
  - Capacitor Layers
Layout for reliability: CMP

Dummy patterns are distributed over chip as uniformly as possible in order to reach the required for each material (Metal 1, 2, 3, 4, 5, Poly 1 and CTM (capacitor top metal)).

All Metal Fill pattern (staked M1, M2, M3, M4)

Poly 1 Fill pattern as metal metals

Stress releasers
- Slots in metals W> Value (tech. dependent)
- Possible library of components
  - Corners
  - Pads

| AM.C.1 | Minimum slots spacing between neighbor layers (i.e.: MET1 / MET2, MET2 / MET3, MET3 / MET4) |
| AM.C.2 | Minimum slot to inner metal edge spacing |
| AM.C.3 | Minimum slot to outer metal edge spacing |
| AM.W.2 | Minimum width of METx connected to wide METx with slots |
| AM.R.1 | Starting position of parallel slots should be staggered. |
| AM.R.2 | Slot must be parallel to the current direction. |
Layout for reliability: Electromigration

- Exist technological preventive measures
  - Type of metal layer (Cu better than Al)
  - Oxidation (better over field oxide)
  - Use of protective overcoats
- With of interconnections: $M \, \mu m/mA$
  - Typical $M$: between 1 and 0.5
- Maximum current per contact and vias

Layout for reliability: Antenna

- Vulnerability depends on ratio between periphery/area of trapping material to gate area
- Fab. 1: Rules Poly and metal layers (including contacts)
  - Max perimeter ratio of field poly to active poly
  - Max perimeter ratio of floating metals to active poly
  - Max drawn area of CO vs. Active Poly

Poly and Metal ratio definition

$$ratio = \frac{2[(L_1 + W_1) \cdot Z_1]}{W_2 \cdot L_2}$$

Contact and via ratio definition

$$ratio = \frac{\text{Contact(Via) area}}{W_2 \cdot L_2}$$
Layout for reliability: Antenna

- Fab. 2
  - Maximum floating (Poly, Metal) Edge area ratio to active area ratio.
    - Use of “leakers” and metal jumpers

Layout for reliability: Latch-up

- Activation if voltages:
  - Higher than VDD
  - Lower than GND
  - I/O Circuitry more sensible
- Elimination of minority carriers
  - Guard rings
  - Biased with low resistances
- Increase distances between sensible and sensitive structures
- Reduce beta parasitic transistors. Reduce forward bias resistance
Layout for reliability: Latch-up

<table>
<thead>
<tr>
<th>Condition</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>L1</td>
<td>A guard ring structure should be inserted between M0S0 and M10S0.</td>
</tr>
<tr>
<td>L2</td>
<td>M0S0 and M10S0 guard rings should be drawn with ESR裕量 for 2 V DD buffers.</td>
</tr>
<tr>
<td>L3</td>
<td>Minimum ESR裕量 spacing for I/O buffers and SS devices.</td>
</tr>
<tr>
<td>L4</td>
<td>Minimum I/O buffer IC layout circuit spacing.</td>
</tr>
<tr>
<td>L5</td>
<td>Any HST/LSHT area connecting to I/O pads should be surrounded by guard rings.</td>
</tr>
<tr>
<td>L6</td>
<td>For special designs such as interface circuits, clocks, or analog circuits such as change pumps, power supplies, logic or high power circuits, a double guard ring should be inserted somewhere between them.</td>
</tr>
<tr>
<td>L7</td>
<td>Any N0S with direct connection to I/O and VDD_N/O should be surrounded by guard rings.</td>
</tr>
<tr>
<td>L8</td>
<td>All I/O guard rings and perhaps should be connected to VSS, VDD, VSS with very low series resistance. This is to N0S should be tied together with N0S and N0VSS should be tied together with contacts and to VSS and VDD. As many as possible points should be used.</td>
</tr>
</tbody>
</table>

Layout for reliability: Analog PAD

- Diodes and resistors for ESD protection
- Reverse diodes: Parasitic capacitance!!!
Example of RF PAD without diodes

References

- http://www.wikipedia.org/