Implementation of Components and Circuits

- Fundamental concepts
- Examples

Outline

- Layout basic concepts and examples
- Layout vs. Schematic: origin of differences
  - Fabrication
  - Design
- Design rules
- Layout of large area components
- Layout for matching
- Effects of Layout on IC reliability
- Layout for reliability
Floorplan

- Sketch of the layout
- Estimation of the IC area
- Technology dependent
  - List of components – subcircuits
  - View
  - Library - models
  - Physical layers available

- Pad limited vs. Core limited designs

Pads

- Provide surface for bond-wire soldering
- Include I/O protection circuitry
## Layouts

- Digital logic: automatic place & route, use of standard cells
- Analog & High Performance: aided manual design
- Components with multiple physical implementations
  - Resistors
  - Capacitors
  - Bipolar transistors
  - Power components

## Example of components: transistors

- Single-gate NMOS, 0.35 μm
- Multiple-gate NMOS, 0.35 μm
- Vertical NPN BJT, 0.35 μm
- Lateral BJT, 0.35 μm
Example of components: passives

- N Diffusion resistor
- Polysilicon resistor
- Polysilicon capacitor
- NMOS transistor
- Polysilicon capacitor

P-cells
Designing a layout: CAD Tools

- Layout design aids in nowadays CAD Tools:
  - Library of components’ layouts (Design Kit)
  - Parameterized layouts
  - Automatic layout generation (Place & route)
  - Layout vs. Schematic
  - Rules checking
  - Extractor and layout simulation

- Is the proposed layout a good layout?

Designing a layout: CAD Tools

- A good layout must be:
  - Ease manufacturability (increase yield)
  - Robust to variations
  - Robust to gradients (matching)
  - Robust against perturbations
  - Robust against other undesired phenomena
Lithography

Illuminator: can be Krypton Fluoride (KrF, $\lambda = 248$ nm), Argon Fluoride (ArF, $\lambda = 193$ nm), Fluorine (F2, $\lambda = 157$ nm).

Condenser Lens: focuses light on 4x (or 5x) mask

Photomask: made of fused quartz (aka, fused silica)

Projection lens: focuses light on wafer
characterized by its numerical aperture NA

Definition of numerical aperture NA where $n$ is a diffraction index:

$$NA = n \cdot \sin \alpha$$

where

- $1$ for air
- $\sim 1.5$ for water, oils

Rayleigh’s equations:

$$\text{resolution} = k_1 \frac{\lambda}{NA}$$
$$\text{depth of focus (DOF)} = k_2 \frac{\lambda}{NA^2}$$

where $k_1$, $k_2$ depend on the quality of the photolithography system (typ. $k_1 \sim 0.25 - 0.7$, $k_2 \sim 0.5$)
Lithography

• Example: which is the critical dimension that can be achieved with $\lambda=248\text{ nm}$?
  Reasonable NA for air is $0,8$
  Guess $k_1=0,4$
  
  \[ \text{resolution} = 0,4 \times \frac{248\text{nm}}{0,8} = 124\text{nm} \]

• Example: which is the critical dimension that can be achieved with $\lambda=193\text{ nm}$?
  Reasonable NA for air is $0,8$
  Guess $k_1=0,3$
  
  \[ \text{resolution} = 0,3 \times \frac{193\text{nm}}{0,8} = 72\text{nm} \]

Lithography

• 436 nm: used down to 3 $\mu$m technologies
• 365 nm: used down to 0,6 $\mu$m technologies
• 248 nm: used down to 130 nm technologies

• 193 nm in air (dry lithography)
  Used in technologies down to 90 nm
  (still in use for some layers in 65 nm, 45 nm...)

![50nm Resist Lines With 193nm Light](image)
**Lithography**

- 436 nm: used down to 3 \( \mu \text{m} \) technologies
- 365 nm: used down to 0.6 \( \mu \text{m} \) technologies
- 248 nm: used down to 130 nm technologies
- 193 nm in air (dry lithography)
- 157 nm: needs special lens materials

**Abandoned definitively in 2005** (due to technical difficulties associated with the mask and photoresist materials for this wavelength; also for the economical cost)

**Lithography**

- 436 nm: used down to 3 \( \mu \text{m} \) technologies
- 365 nm: used down to 0.6 \( \mu \text{m} \) technologies
- 248 nm: used down to 130 nm technologies
- 193 nm in air (dry lithography)
- 157 nm: needs special lens materials
- EUV (\( \lambda = 13 \text{ nm} \)). New approach: mirrors, no lenses

**Optimistic forecast:** ready for 22 nm technology node (~2011)
**Lithography**

- 436 nm: used down to 3 \(\mu\)m technologies
- 365 nm: used down to 0,6 \(\mu\)m technologies
- 248 nm: used down to 130 nm technologies
- 193 nm in air (dry lithography)
  - 193 nm in liquid (immersion lithography)

Used in 65 nm, 45 nm, (32 nm) technology nodes (NA 1.1 → 1.3)

**Double patterning:** generate a single layer by using two masks

- Double exposure
  - Spacer mask
  - Heterogeneous mask

Used in 65 nm, 45 nm, technology nodes
Lithography

32 nm SRAM Chip

- 0.182 μm² cell size
- 291 Mbit, >1.9 billion transistors
- 118 mm² chip size
- 2nd gen. high-k + metal gate transistors
- 193 nm immersion lithography on critical layers
- 193 nm dry or 248 nm dry litho on less critical layers
- Functional silicon in Sept '07

Manufacturing: subwavelength gap

⇒ Increased diffraction effects!

From Massimo Conti, BCN 2006
Differences between layout and Circuit (I)

- Fabrication process limitations
  - Lateral diffusion
  - Etching under protection
  - Boundary dependent etching
  - Three-dimensional effects
    - Chemical Mechanical Polishing (CMP)
    - Surface topography

Differences between layout and Circuit (II)

- Fabrication process limitations
  - Narrowing after annealing
  - Inherent grain variability
  - Proximity effects
  - Errors and limitations
    - Mask productions
    - Mask alignment

Oxide variations over a 20 Å nominal oxide thickness
Differences between layout and Circuit (III)

- Absolute accuracy of physical parameters
  - Controlled at technological level
  - Simulation: Process variation

\[
\frac{\sigma^2(\beta)}{\beta^2} = \frac{A^2_p}{WL} + S^2_p D^2
\]

\[
\sigma^2(V_T) = \frac{A^2_i}{WL} + S^2_i D^2
\]

From Massimo Conti, BCN 2006

Differences between layout and Circuit (III)

- Absolute accuracy of physical parameters
  - oxide damage
  - impurities
  - temperature
  - stress
  - bias conditions
  - growth rate
  - grain size
  - etching inaccuracy
  - mask alignment

From Franco Maloberti, "Layout of Analog CMOS ICs"
Differences between layout and Circuit (IV)

- Relative inaccuracies of physical parameters
  - Gradients, local variations
    - Compensated with suitable layout techniques
  - Crystal orientation variations
    - Components required to be laid in a determined orientation

Example: normalized drain current dispersions of 2 MOSFETs for different geometries and distances

- Inaccuracy in absolute value, but matched devices
- Inaccuracy in absolute value, and mismatched devices
Differences between layout and Circuit (V)

- Parasitic coupling
  - Capacitive coupling
  - Couplings through the power supply
  - Couplings through the substrate

- Parasitic resistances
  - Contacts
  - Interconnect

What you get is not what you draw!

- Many of the systematic inaccuracies can be avoided through good layout style.

- But designers must understand the limitations and apply design techniques to mitigate these effects.
Corrections performed by the foundry

- Some manufacturing distortions can be predicted and fixed by introducing modifications to the mask
  - OPC: Optical Proximity Correction

Examples of corrections automatically introduced by a OPC algorithm to the shapes in the mask

From "Nano-CMOS Circuit and Physical Design", Wong et al, IEEE Press
Corrections performed by the foundry

This top down SEM image was taken without any OPC. The pullback over the contact is clearly seen.

This image of the same structure was taken with OPC implemented on the mask. Good contact coverage can be seen.

Design for manufacturability: design rules:

Example: Poly 1
Example of design rules for POLY 1

- **PO.W.1a**
  - Minimum gate length of PMOS
- **PO.W-2a**
  - Minimum gate length of NMOS
- **PO.W.3**
  - Minimum POLY1 width for interconnect
- **PO.S.1**
  - Minimum POLY1 spacing
- **PO.C.1**
  - Minimum POLY 1 to DIFF spacing
- **PO.C.2**
  - Minimum DIFF extension of GATE
- **PO.O.1**
  - Minimum POLY1 extension of GATE

Optimized layouts:

From "Nano-CMOS Circuit and Physical Design", Wong et al. IEEE Press
Optimized layouts:

- Optimize efficiency of vias/contacts
- Maximize number of vias/contacts

All transistors in the same orientation
  - Better control of manufacturing
  - Easier lithography (mask) corrections

From "Nano-CMOS Circuit and Physical Design", Wong et al, IEEE Press

Optimized layouts:

- Possible shortcircuit of nodes A and B due to diffusion flaring and mask misalignment
- Possible shortcircuit due to poly flaring
- Possible shortcircuit due to diffusion flaring

Will lead to diffusion short

From "Nano-CMOS Circuit and Physical Design", Wong et al, IEEE Press
Layout for matching

- Devices with the same orientation
  - Current in the same direction
- Gradients increase with distance
- Same orientation towards physical gradients

Layout for matching

- Interdigitated structures

MOS transistors M1 and M2

Resistors R1 and R2
Layout for matching

- Interdigitated structures

Different symmetry axes for transistors A and B

Same symmetry axis for transistors A and B

from Franco Maloberti, “Layout of Analog CMOS ICs”

Layout for matching

- Common centroid:
Layout for matching: Common centroid

- **Coincidence**
  - Centroids of matched devices should coincide

- **Symmetry**
  - Array symmetric around both X and Y axis

- **Dispersion**
  - Segment of each device distributed throughout the array as uniformly as possible

- **Compactness**
  - Ideally: array should be square

From Franco Maloberti, "Layout of Analog CMOS ICs"
Layout for matching: Use of dummies

- **Dummies**
  - Use dummy devices to provide the same contour conditions.
    - Ground dummies (do not let them float)
    - Dummies can be full (shorted) devices, or part of them
    - Beware of their parasitics!

Reference cell

- Use multiple basic transistors instead of different sizes
  - Same $W$, same orientation,
Design of large area components

- MOS Transistors
  - Multiple gates to minimize serial resistance
  - Multiple contacts to minimize serial resistance
    - No big contacts!!!
  - “stacked” structures
    - Lower parasitic capacitances
    - Lower area
  - Analogue applications
    - Avoid minimum size

Design of large area components

- Resistances
  - Bended structures
  - Dummy structures
  - 45 degrees (avoid non laminar current flow)
  - Contacts
    - Current in the same direction
    - Multiple contacts
  - Piezoresistive effect

Example of “good” and “bad” layout

Resistor: 5K, 275x3 sq microns.
Layout for matching: interconnects

- CMP:
  - Erosion effect: denser interconnects will have higher R


Rules for matching

- Same W and L: Vary M
- Capacitors
  - Multiple M of a capacitance reference $C_R$
- Ms: Even (factors of 4!!)
- Clean and balanced routing
  - IR drops
  - Parasitic capacitance and couplings
  - Kelvin connections
- Avoid minimum sizing and overlapping
- Use dummy structures
- Same spacing in interconnects
Electromigration

- **Electromigration** is the transport of material caused by the gradual movement of the ions in a conductor due to the momentum transfer between conducting electrons and diffusing metal atoms.

- Dependent on:
  - Temperature
  - Current density
  - Conductor Shape
  - Material

Exist technological preventive measures

- Type of metal layer (Cu better than Al)
- Oxidation (better over field oxide)
- Use of protective overcoats

Width of interconnections: M μm/mA

- Typical M: between 1 and 0.5

Maximum current per contact and vias
Layout Strategies for circuit reliability (II)

**Latch-up**
- A latchup is the inadvertent creation of a low-impedance path between the power supply rails of an electronic component, triggering a parasitic device, which then acts as a short circuit, leading to malfunctioning of the part and perhaps even its destruction with the overcurrent.

**Layout for reliability: Latch-up**

**Activation:**
- If voltages higher than VDD
- If voltages lower than GND
- If currents through the well/substrate
- I/O Circuitry more sensitive

**Elimination of minority carriers**
- Guard rings
- Biased with low resistances

**Reduce beta parasitic transistors. Reduce forward bias resistance**
Layout for reliability: Latch-up

- Reduce forward bias resistance:

Rules:

<table>
<thead>
<tr>
<th>Condition</th>
<th>Description</th>
<th>Rule 1</th>
<th>Rule 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>I/O buffer</td>
<td>Must be within 25% of NSD and JNOS of I/O buffer</td>
<td></td>
<td></td>
</tr>
<tr>
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<td>Minimum distance to PTAP or NTAP is 0.5 mm</td>
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</tr>
</tbody>
</table>

Maximum distance from any point inside NSD to the nearest PTAP
Maximum distance from any point inside PSD to the nearest NTAP

NTUB must be covered with NTAP sized by

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Layout for reliability: Latch-up

- I/O Circuitry more sensitive

I/O transistors surrounded by pick-ups and guard rings

I/O and core transistors separated by guard rings
Layout Strategies for circuit reliability (III)

- CMP
  - Chemical Mechanical Polishing or Chemical Mechanical Planarization
  - Removal any irregular topography
  - Surface within the depth of field of a photolithography system.

Layout for reliability: CMP

- Example: MOSIS 0.25 (TSMC)
- Design rules:
  - Minimum % coverage of Metal layers
  - Polysilicon layers
  - Capacitor Layers
Dummy patterns are distributed over the chip as uniformly as possible in order to reach the required coverage for each material (Metal 1, 2, 3, 4, 5, Poly 1 and CTM (capacitor top metal)).

All Metal Fill pattern (staked M1, M2, M3, M4)

Poly 1 Fill pattern as metal

Layout for reliability: CMP

1. Orientation of dummy pattern should be perpendicular to previous layer
2. Top layer should have larger dummy pattern

Example: 4-metal technology

Pattern for M1 | Pattern for M2 | Pattern for M3 | Pattern for M4 (top)
Layout for reliability: CMP

- Patterns generated automatically by the foundry

- User has masks to define areas that will NOT be filled with patterns (Ex: inductors, capacitors, test structures, etc)

Example in a 0.18 μm technology:

![Example of Transmission line in M7 with dummy metals below:](image)

Open question: How do dummy metal fills affect transmission lines and passives?
Layout for reliability: CMP

Proposal: slow-wave transmission lines
- Low Q
- Small area
- Necessary grid fulfills metal coverage

Borremans et al., "VCO design for 60 GHz applications using differential shielded inductors in 0.13 µm CMOS", RFIC’08

Layout for reliability: CMP

- Slots
  - Act both as stress releasers and to minimize dishing
  - Slots in metals W> Value (tech. dependent)
  - Possible library of components
    - Corners
    - Pads

| AM.C.1 | Minimum slots spacing between neighbor layers (i.e.: MET1 / MET2, MET2 / MET3, MET2 / MET4) |
| AM.C.2 | Minimum slot to inner metal edge spacing |
| AM.C.3 | Minimum slot to outer metal edge spacing |
| AM.W.2 | Minimum width of METx connected to wide METx with slots |
| AM.R.1 | Starting position of parallel slots should be staggered. |
| AM.R.2 | Slot must be parallel to the current direction. |
Layout Strategies for circuit reliability (IV)

- **Antenna Effects or Plasma-Induced damage**
  - The "Antenna Rules" deal with process induced gate oxide damage. Reactive ion-etching may induce charges to exposed polysilicon and metal structures. If these structures are connected to gates (and not to diffusion), they may develop potentials sufficiently large to cause Fowler Nordheim current to flow through the thin oxide.

Layout for reliability: Antenna

- Vulnerability depends on ratio between periphery/area of trapping material to gate area
- Fab. 1: Rules Poly and metal layers (including contacts)
  - Max perimeter ratio of field poly to active poly
  - Max perimeter ratio of floating metals to active poly
  - Max drawn area of CO vs. Active Poly

**Poly and Metal ratio definition**

\[
\text{ratio} = \frac{2[(L_1 + W_1) \cdot Z_1]}{W_2 \cdot L_2}
\]

**Contact and via ratio definition**

\[
\text{ratio} = \frac{\text{Contact(Via) area}}{W_2 \cdot L_2}
\]
Layout for reliability: Antenna

- **Fab. 2**
  - Maximum floating (Poly,Metal) Edge area ratio to active area ratio.

- **Use of “leakers” and metal jumpers**

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Layout Strategies for circuit reliability (V)

- **ESD**
  - Electrostatic Discharge
  - Damage in dielectrics due to IC manipulation (mainly gate oxide)
Layout for reliability: Analog PAD

Diodes and resistors for ESD protection
Reverse diodes: Parasitic capacitance!!!
References

- http://www.wikipedia.org/