SYSTEM INTEGRATION ASPECTS

High Performance Integrated Circuits Design Group
http://pmos.upc.es/blues/

Design of CMOS Integrated Circuits for RF wireless communications
May 2005

Departament d’Enginyeria Electrònica
Universitat Politècnica de Catalunya

Contents:

1. SoC vs SiP
2. SSN
   • Concept
   • Design techniques for SSN reduction
3. Substrate noise
   • Concept
   • Isolation techniques
   • Prediction
4. Packages for RF
5. Pads for RF
1. SoC vs. SiP

SoC:

- Bluetooth radio + baseband in a single chip
- 0.18 µm CMOS technology

Paul van Zeijl, et al., “A Bluetooth Radio in 0.18 µm CMOS”, IEEE JSSC December 2002
1. SoC vs. SiP

SoC:

- Crosstalk / signal integrity problems!!!
- Crosstalk between interconnects
- Noise at the power-supply nodes
- Disturbances coupled through the common silicon substrate in CMOS technologies

1. SoC vs. SiP

SiP:

- 33 mm
- 17 mm
- RF Module
- BB Chip
- Flash
- Flip-Chip mounting
- Wire-bond mounting
1. SoC vs. SiP

SoC:

↑ Maximum integration – minimum cost
↓ All chip (including digital area, typ >50%) implemented in a costly analog technology
↓ Faulty die implies dismissing all the system!
↓ Signal integrity problems (modeling/tools)
↓ Integration of flash, other complex technologies
↓ Digital/analog generation mismatch
↓ Analog redesign required when technology scales
↓ Some blocks (duplexer, PA) still off-chip

SiP

↓ Cost
↑ Integration of different technologies
↓ Packaging Yield
↓ Lack of system integration models/tools

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2. SSN Fundamentals

Basic concept:

- Noise in power-supply lines due to package / bonding parasitics (inductance)

\[ V_{dd} - L \frac{dI}{dt} \]

\[ GND + L \frac{dI}{dt} \]

Aka. delta-I noise, GND bounce

2. SSN Fundamentals

Inductances in on-chip current loops:

- Package pin inductance, bonding inductance

<table>
<thead>
<tr>
<th>Package Type</th>
<th>Inductance (nH)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PGA 256 pins</td>
<td>15.0 nH</td>
</tr>
<tr>
<td>EBGA 256 pins</td>
<td>6.0 nH</td>
</tr>
<tr>
<td>DIP 68 pins</td>
<td>35.0 nH</td>
</tr>
<tr>
<td>PLCC 44 pins</td>
<td>6.2 nH</td>
</tr>
<tr>
<td>MQFP 44 pins</td>
<td>3.5 nH</td>
</tr>
<tr>
<td>DIP 18 pins</td>
<td>13.7 nH</td>
</tr>
<tr>
<td>SOIC 18 pins</td>
<td>8.5 nH</td>
</tr>
<tr>
<td>QSOP 18 pins</td>
<td>3.6 nH</td>
</tr>
<tr>
<td>TQFP 48 pins</td>
<td>1.5 nH</td>
</tr>
<tr>
<td>Wire bond</td>
<td>1 nH/mm</td>
</tr>
<tr>
<td>Solder ball</td>
<td>0.1 nH</td>
</tr>
</tbody>
</table>

Average self-inductance per pin for different packages and bonding systems.

- On-chip interconnect inductances
  - In the range of ~1 - 2 nH/mm
  - No closed analytical modeling, some semiempirical (?) expressions available, some measurement results.

- Inductances associated to undesired (non-ideal) return paths (?)
2. SSN Fundamentals

- L = 10 nH, 10 buffers simultaneously switching, 0.35 µm technology, (W/L)_{NMOS}=(0.5/0.35), (W/L)_{NMOS}=(1/0.35), fanout=5

- In a fall transition, current through the package is due to the charge of a PMOS load capacitance (C2) through a NMOS net (T1)
- In a rise transition, current through the package is due to the charge of a NMOS load capacitance (C3) through a PMOS net (T4)

⇒ different SSN in rise / fall transitions
2. SSN Fundamentals

Current loops producing SSN (off-chip load):

- In a fall transition, no current through \( I_{Vdd} \) ⇒ no SSN in \( V_{dd} \) in fall transitions
- In a rise transition, no current through \( I_{GND} \) ⇒ no SSN in GND in rise transitions

+ \( I_1, I_4 \) now produce SSN!!

---

2. SSN Fundamentals

Charge sharing:

\[ R_{NS} \] and \( C_{NS} \) represent the Non-switching part of the IC and contribute to the transient current demanded by the switching part represented by \( R_S \) and \( C_S \).

© The non-switching gates act as on-chip decoupling capacitance, reducing the current that flows through the power supply inductance.

© The circuit behaves as a RLC resonator. A damped oscillation can be found in the power supply nodes just after the \( dI/dt \) noise pulse.
2. SSN fundamentals

SSN prediction. Simple (but wrong) model:

- If $I$ is the current drawn by ONE gate, it was assumed that, for $n$ gates switching simultaneously, SSN takes the value

$$V_{\text{SSN}} = n L_{\text{eff}} \frac{dI}{dt}$$

$$L_{\text{eff}} = L_{\text{self}} - L_{\text{mutual}}$$

- This is a wrong (overestimates noise) assumption since does not include negative feedback effects, charge sharing, etc.
- In practice, package modeling is not so simple, thus $V_{\text{SSN}}$ is not strictly linear with $L_{\text{eff}}$
- Also, due to parasitic capacitances, resonance appears and $V_{\text{SSN}}$ is not strictly linear with $dI/dt$


2. SSN fundamentals. Simple models

- $L = 10$ nH, 10 buffers simultaneously switching, 0.35 μm technology, $(W/L)_{\text{NMOS}} = (0.5/0.35), (W/L)_{\text{PMOS}} = (1/0.35)$, fanout=5
2. SSN fundamentals. Simple models

Effect of package inductance $L$

- Now $L = 1$ nH, 10 buffers simultaneously switching

- Now $L = 10$ nH, only 1 buffer switching

- Current peaks reduced (approx. /10)
- Noise amplitude reduced (approx. /3)
- Smaller period of oscillations
2. SSN Fundamentals
Package-related techniques to reduce SSN in ICs: Package / pin selection

- **Choose low-inductive packages!!**

<table>
<thead>
<tr>
<th>Package</th>
<th>Average Self-inductance (nH)</th>
</tr>
</thead>
<tbody>
<tr>
<td>PGA 256 pins</td>
<td>15.0 nH</td>
</tr>
<tr>
<td>EBGA 256 pins</td>
<td>6.0 nH</td>
</tr>
<tr>
<td>PLCC 64 pins</td>
<td>3.5 nH</td>
</tr>
<tr>
<td>MQFP 44 pins</td>
<td>1.5 nH</td>
</tr>
<tr>
<td>TQFP 48 pins</td>
<td>1.5 nH</td>
</tr>
<tr>
<td>PLCC 68 pins</td>
<td>6.2 nH</td>
</tr>
<tr>
<td>EBGA 68 pins</td>
<td>6.2 nH</td>
</tr>
<tr>
<td>MQFP 64 pins</td>
<td>3.5 nH</td>
</tr>
<tr>
<td>TQFP 68 pins</td>
<td>3.5 nH</td>
</tr>
<tr>
<td>DIP 68 pins Plastic</td>
<td>10.3 nH</td>
</tr>
<tr>
<td>DIP 18 pins Plastic</td>
<td>13.7 nH</td>
</tr>
<tr>
<td>DIP 18 pins Plastic</td>
<td>13.7 nH</td>
</tr>
</tbody>
</table>

- **Multiple assignment:**
  - Assigning \( n \) pins for GND-Vdd, self-inductance is reduced to approx. \( 1/n \)
  - Nevertheless, due to the effect of mutual inductances, \( L_{\text{eff}} \) is not reduced so strongly ⇒ SSN is not reduced so strongly.
  - In fact, large digital chips already need large number of supply pins to stand large currents*. **

* ITRS predicts number of pins in MPU assuming supply pins are 2/3 of total
** IBM's POWER4 has ~2200 I/O pins out of ~5000 pins in total

- Assign low-inductive pins to Vdd-GND:

  - Ex: Self-inductance of 68_PLCC trace:
    - Corner: 10.4 nH
    - Center: 6.8 nH

  - Ex: Self-inductance of 64_MQFP trace:
    - Corner: 3.5 nH
    - Center: 2.4 nH

  - Ex: Self-inductance of 64_TQFP trace:
    - Corner: 1 nH
    - Center: 0.8 nH
2. SSN Fundamentals
Circuit-related techniques to reduce SSN in ICs: Decoupling capacitors

- On-chip decoupling capacitors supply charge to switching gates, minimizing peak currents across inductances:

\[ V_{dd} \rightarrow C_d \rightarrow V_{NS} \rightarrow R_S \]

- Nevertheless, high capacitance values require large areas (Ex: poly1-poly2 \( \sim 1 \text{fF/} \mu\text{m}^2 \Rightarrow 1 \text{nF/mm}^2 \))
- MOS gate capacitance may be used as decoupling capacitor (Ex: \( \sim 5 \text{fF/} \mu\text{m}^2 \Rightarrow 5 \text{nF/mm}^2 \))
  - Here, the series channel (and polisilicon) resistance value is significant.
  - This resistance value has to be chosen in a trade-off between series voltage drop, and damping effect.

Ex: Decoupling capacitors in digital and analog supplies of a 1.3 Gs/s 6 bit Flash ADC [1]:

Pad-limited layout: 1.6 nF decoupling capacitance included in empty areas; 64-pin TQFP package, \( \sim 500 \text{ mW} \) power consumption.

2. SSN Fundamentals
Circuit-related techniques to reduce SSN in ICs: Decoupling capacitors

- On-chip capacitors unuseful to decouple noise of off-chip drivers:

- Decoupling capacitors contribute to oscillations in power-supply
  - First peak SSN itself (current-peak dependant)
  - Sustained oscillation

\[ \omega_{res} = \frac{1}{\sqrt{L_{eff}C_{chip}}} \]

\[ \xi = \frac{\alpha_{des}}{2} \sqrt{L_{eff}} \]

2. SSN Fundamentals
Circuit-related techniques to reduce SSN in ICs: Alternative logic families

- Constant-current logics
  - No current spikes
  - High power consumption (limited usage)

- Ex: ESCL (Enhancement Source-Coupled Logic)

\[ \Delta V_L < 0.2V_{DD} \]

- Others: SCL (Current-Steering Logic), FSCL (Folded Source-Coupled Logic)
2. SSN Fundamentals

Circuit-related techniques to reduce SSN in ICs: Skewing output buffer switching

- Skew output driver switching to add up a “constant” current consumption.

Ex: 2 groups of 4 buffers skewed ΔT, SPICE simulations [1]

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2. SSN Fundamentals

Circuit-related techniques to reduce SSN in ICs: Self-timed differential logics

- Extension of the former technique to the IC core: divide circuit into blocks that generate similar current peaks, and that switch *consecutively*, to add a trapezoidal current consumption

- Conditions:
  - Make logic circuit as regular as possible, adding redundant logic if necessary to equalize the number of switching gates per block.
  - Use logic that produces similar current pulses regardless of the input vector.
  - Partition logic into blocks of similar delay.
2. SSN Fundamentals

Circuit-related techniques to reduce SSN in ICs: Self-timed differential logics

- Current-controlled buffer (currents limited to \( I_{p_{\text{max}}} I_{n_{\text{max}}})

![Diagram of current-controlled buffer](image)


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3. Substrate Noise Fundamentals

Complexity of Substrate Noise evaluation

- Distributed nature of propagation path (hard to get an efficient model)
- Many (all?) factors influence noise levels:
  - Technology
  - Circuit sensitivity
  - Package
  - Floorplan
  - Detailed layout
  - Architecture
  - Power distribution network

3. Substrate Noise Fundamentals

Complexity of Substrate Noise evaluation

- No single recipe valid for all situations, all circuits
- When evaluating substrate noise problems, it is necessary to take into account all the system
  - Package
  - Substrate
  - Noise generation
  - Affected circuit
  - Parasitics related with power/ground distribution & substrate biasing

⇒ Prediction necessary, but extremely complex!!
3. Substrate Noise Fundamentals

Noise sources: MOS transistors

- **Capacitive coupling** through drain-substrate junction ($C_j \cdot dV/dt$)

- **Impact ionization** substrate current. Dominant only at low frequencies $^{1,2}$ (below 10 MHz aprox.)

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3. Substrate Noise Fundamentals

Noise sources: Bipolar transistors

- Again **capacitive coupling** is dominant.
- NPN larger, faster than MOS ⇒ noisier!!$^1$
- Noise amount depends on topology (switching emitter vs. switching collector), and technology (collector resistance)$^1$

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3. Substrate Noise Fundamentals

Noise sources: Passive components

- Noise coupled from spiral inductors used in RF blocks (mainly from high-power blocks like LO and PA; coupling to other RF blocks)
- Capacitors and resistors are mainly noise sensitive components, rather than noise sources.
- Bonding pads have important capacitance, may inject noise

![Image of noise coupling model]

(left) Noise coupling model has to be included in inductor device model

(right) Models for on-chip inductors

- Accuracy of parasitics ($C_{ox}$) and substrate model important to accurately predict inductor’s losses ($Q$)

3. Substrate Noise Fundamentals

Noise sources: Interconnects

- Switching interconnects may couple (capacitive) disturbances to the substrate.
- Long interconnects may couple as much noise as hundreds of MOS transistors.
- Wells under the interconnects may isolate coupling.

\[ V_{dd} - L \frac{dl}{dt} \]

3. Substrate Noise Fundamentals

Noise sources: SSN

- Noise in power-supply lines due to package / bonding parasitics (inductance)
### 3. Substrate Noise Fundamentals

#### Noise sources: SSN

- May switch-ON ESD or source-substrate diodes
- **MOST IMPORTANT**: noise is injected to the substrate by ohmic taps / contacts

  ![Diagram: Substrate Noise Injection](image)

  - Number of contacts↑↑: The equivalent resistance between a substrate point and on-chip GND may be as low as < 1 Ω!!
  - This is the most important noise source in mixed A/D designs!!

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### 3. Substrate Noise Fundamentals

#### Noise propagation: “Digital” substrates

- To prevent latch-up, pure digital technologies use heavily doped / low resistive / P+ substrates
- Noise currents flow mainly just below the epi layer, not near the surface (guard rings cannot be effective)
- Negligible attenuation with distance. Highly conductive substrate can be modeled as a single node.

![Diagram: Substrate Noise Attenuation](image)
3. Substrate Noise Fundamentals

Noise propagation: “RF” substrates

- But in mixed-signal and RF processes, a lightly doped / highly resistive / P- substrate is preferred
- Part of the currents propagate along the channel-stopper, the rest distribute inside the bulk (guard rings may work)
- Noise may attenuate with distance. A complex distributed substrate model is necessary.

![Diagram of substrate noise propagation](image)

3. Substrate Noise Fundamentals

Noise propagation: “Digital” vs. “RF” substrates

- P+ substrates propagate more noise than P-, unless biased with very low inductive packages

![Measurement graph](image)

Measurements on a mixed A/D test IC, DIP48 package

3. Substrate Noise Fundamentals
Noise propagation: “Digital” vs. “RF” substrates

- Provides ideal DC isolation
- Nevertheless, BOX behaves as a capacitor. At freq. high enough, isolation matches that of bulk silicon

Simulations on a mixed A/D test IC

3. Substrate Noise Fundamentals

Noise propagation: other propagation paths

• Noise between distant points will propagate through a conductive chip backside (if present)

\[ \begin{align*}
\text{(a)} & \quad d \ll T_w \\
\text{(b)} & \quad d = T_w \\
\text{(c)} & \quad d = 2.5 \times T_w
\end{align*} \]

Figure 10: Substrate current flow in a lightly doped non-conductive epoxy on the backside


• If \( V_{dd} \) and GND connections are inductive (high AC impedance), noise may propagate along the supply ring in the periphery

• Noise may propagate also along the “scribe line” that encloses (and almost shortcircuits) the whole IC.
3. Substrate Noise Fundamentals

Noise propagation: other propagation paths

- Noise may propagate also along the “scribe line” that encloses (and almost shortcircuits) the whole IC.

3. Substrate Noise Fundamentals

Noise sensitivity: MOS transistors

- **Capacitive coupling** through drain-substrate junction \((C_j \cdot dV/dt)\)

- **Body effect** \((V_T \text{ modulation})\)

\[
V_f = V_{FG} + \gamma \left( \sqrt{2}\phi_b - V_{BS} - \sqrt{2}\phi_b \right)
\]

\(\Rightarrow\) Analog \(V_{ss}\) must be connected to substrate to minimize body effect

- **Analog \(V_{ss}\** \((\text{and } V_{dd})\) also contaminated with substrate noise
3. Substrate Noise Fundamentals

Noise sensitivity: Passive elements

- Capacitive coupling to N-well resistors
- Capacitive coupling to capacitors
- Capacitive coupling to inductors

⇒ well shielding may help (depends on freq., total area)
⇒ triple-well technologies are welcome

3. Substrate Noise Fundamentals

Noise sensitivity: Circuits

- Differential analog processing necessary
  - Cancels out common-mode noise
  - Also less sensitive to noise coupled in the circuit
    - Example: Differential vs. Unipolar amplifier

<table>
<thead>
<tr>
<th>(freq in Hz)</th>
<th>Unipolar</th>
<th>Differential</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
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<tr>
<td></td>
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</tbody>
</table>

- Same response to input
- 6 dB difference in amplification of substrate noise (other than the input)
3. Substrate Noise Fundamentals

Noise sensitivity: Circuits

- To avoid $V_T$ modulation, short $V_S$ and substrate $\Rightarrow$ bias analog P-wells with analog GND. Use NMOS transistors for current sources

- Refer analog signals to a clean analog ground. Use PMOS transistors for signal handling. Bias analog N-wells with analog $V_{DD}$


In pure analog circuits, if the noise frequency content is outside the signal band, no effect will be produced unless the analog circuit is non-linear.

- In RF circuits, overlap of noise and signal frequency spectrums is also important
  - Ex: coupling from LO to RF path in direct-conversion receivers, which manifests as offset.

3. Substrate Noise: Reduction of substrate noise

- 1st.- Techniques to reduce substrate noise sources
- 2nd.- Once the noise is there
  - a) Isolate noise source and sensitive circuitry
  - b) Sink noise to ground before reaching the sensitive circuitry
  - c) Active techniques to reduce noise (negative feedback, noise “compensation”, etc.)

But: the efficacy of increasing isolation impedance / decreasing GND sink impedance depends on already existing impedances (substrate, package, load….) ⇒ no universal recipes!!
3. Substrate Noise: Reduction of substrate noise

Horizontal isolation

- Horizontal isolation techniques effective both in P+ and P- substrates
- Depletion capacitances provide series isolation impedance in propagation path. N-well $V_{DD}$ biasing for maximum capacitance.
- N-well may be used to isolate passive components. For CMOS gates, triple-well or buried layer is necessary.

3. Substrate Noise: Reduction of substrate noise

Horizontal isolation

- The efficacy of these isolation depends on well area (and other possible series impedances)
- SOI is another horizontal isolation, (S-O-S capacitance instead of junction depletion capacitance), with increased impedance/area
3. Substrate Noise: Reduction of substrate noise

Vertical isolation

- Vertical isolation techniques not effective in P+ (epi) substrates
- N-wells force substrate currents deep into substrate (increase isolation). OK if propagation in the channel stopper is important.
- Oxide Trenches force substrate currents deep into substrate. Deeper trenches ⇒ better isolation

Guard rings should be connected to quiet (Kelvin) GNDs
- Guards rings in noisy and sensitive areas should be connected to different GNDs (max. isolation)
- …but: in large circuits, all GNDs are virtually shorted… and you have Z_{package}!!!
3. Substrate Noise: Reduction of substrate noise
Sinking to GND though the backside

- P+ (epi) wafers provide a very-low resistive path to a backside GND connection
- Ex: resistance between GND nodes and backside connection in a mixed A/D test IC (including epoxy attachment)

![Diagram of substrate noise reduction](image)

IC manufactured in P- substrate

IC manufactured in P+ substrate

- Nevertheless, GND backside connection useless if package / bonding parasitics dominate!
- Packages with exposed pad (intended for heat transfer) may provide excellent GND backside connection

1 Amkor Technologies datasheets, www.amkor.com
3. Substrate Noise: Prediction of substrate noise

Substrate modeling techniques

- Finite Element Methods (solution of carrier continuity and Poisson equations, i.e., device simulation)\(^1,2,3\)
- Finite Difference Methods (solve \(\frac{\partial}{\partial x}(\nabla \cdot E) + \frac{1}{\rho} \nabla \cdot E = 0\) which reduces substrate to a simple RC mesh)\(^4,5,6\)
- Boundary Element Methods (solve Laplace’s equation by finding the substrate’s Green function under determined contour conditions)\(^7,8,9,10,11,12\)
- Semi-empirical formulas (technology and geometry dependences)\(^1,13,14,15\)
- Single-node approximation (reasonably valid for P+ (epi) substrates)\(^1,16\)

3. Substrate Noise: Prediction of substrate noise

FEM vs. BEM

- Full discretization of the substrate needed (huge matrices)
- Accuracy depends strongly on discretization
- Sparse matrices (fast matrix computations). Mesh reduction techniques available
- May deal with any technology; horizontal & vertical variations.

- Only discretization of ports is needed (smaller matrices). Only port to port relationship modeled
- Dense matrices (slow matrix computations)
- Substrate is treated as a few number of uniform layers (no possible horizontal variation)

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\(^1\) F. Clement, “Substrate Noise Coupling Analysis in Mixed-Signal ICs”, in IMEC 2001 Workshop on Substrate Coupling.
3. Substrate Noise: Prediction of substrate noise

Technology data

- **Needed!!**: substrate technology profiles from the foundry!!

- Resistivity profiles or carrier concentration profiles
- Open profiles or encrypted (tool dependant) profiles

Simplex Solutions, Inc.

3. Substrate Noise: Prediction of substrate noise

Commercial substrate extraction tools

- **SeismIC (CadMOS, acquired 2001 by Cadence)**
  - Boundary Element Method default (faster), changes to Finite Differences Method where needed (accuracy or wells/trenches)\(^1\)
  - Included in Cadence’s physical verification flow of circuits
  - [http://www.cadence.com/datasheets/cadMOSSeism.html](http://www.cadence.com/datasheets/cadMOSSeism.html)


- **SubstrateStorm (Simplex, acquired 2002 by Cadence)**
  - Finite Differences Method (accurate, slow…)
  - Included in Cadence’s physical verification flow of circuits
  - [http://www.cadence.com/datasheets/substratestorm.html](http://www.cadence.com/datasheets/substratestorm.html)
3. Substrate Noise: Prediction of substrate noise

Commercial substrate extraction tools

- At high frequencies, dielectric effect in Si cannot be neglected

\[ J = (\sigma + j\omega\varepsilon)E \]

\[ \sigma = 10 \text{ S/m for } \rho = 10\Omega\text{cm} \]

\[ \omega\varepsilon = 0.1\sigma \quad @ \quad 1.5 \text{ GHz} \]  
1.5 GHz on-chip clocks in 2001\(^1\)

\[ \omega\varepsilon = 0.2\sigma \quad @ \quad 3 \text{ GHz} \]  
3 GHz on-chip clocks in 2003\(^1\)

\[ \omega\varepsilon = 0.5\sigma \quad @ \quad 7.5 \text{ GHz} \]  
7.5 GHz on-chip clocks in ~2008\(^1\)

\[ \omega\varepsilon = \sigma \quad @ \quad 15 \text{ GHz} \]  
15 GHz on-chip clocks in ~2012\(^1\)


Substrate needs to be modeled as a mesh of resistance & capacitances (resistive-only model no longer valid)
3. Substrate Noise: Prediction of substrate noise

Ex: SubstrateStorm substrate extraction flow

- Conventional extraction flow
  - Layout generation
  - Circuit netlist extraction
  - Circuit netlist simulation

- Extraction flow with SubstrateStorm™
  - Layout generation
  - Circuit netlist extraction
  - Identification of technology profiles, definition of access ports
  - Substrate netlist generation
  - Circuit & substrate netlist simulation

...but these tools are usually inadequate

- Existing substrate extraction tools provide an electrical model to allow electrical simulation of the interaction between individual noisy devices and individual sensitive nodes.
  - Thus, you need electrical (SPICE) simulation of all the circuit (before simulation you ignore which are the dominant sources of noise)
    - Prohibitive!!
  - Thus, you will extract a substrate mesh of impedances between all transistors, substrate & well contacts, interconnects...
    - Prohibitive!!
  - Thus, you need a final layout to perform verification
    - Inefficient!!
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4. Packages for RF

Objective: low inductance!!

• Small package/chip size ratio
• Exposed pad for chip backside GND connection
• Unleaded packages
• Flip chip connection
• System in Package (SiP)
4. Packages for RF

**Small package**

**TQFP**

**TSSOP**

**MicroLead Frame (MLF)**

<table>
<thead>
<tr>
<th>Package Type</th>
<th>Body Size (mm)</th>
<th>Pad Size</th>
<th>Inductance (nH)</th>
</tr>
</thead>
<tbody>
<tr>
<td>17-flip</td>
<td>3 x 3</td>
<td>3.5 x 3.4</td>
<td>1.97</td>
</tr>
<tr>
<td>20-flip</td>
<td>7 x 7</td>
<td>5 x 5</td>
<td>2.29</td>
</tr>
<tr>
<td>64-flip</td>
<td>10 x 10</td>
<td>7.5 x 7.5</td>
<td>3.64</td>
</tr>
<tr>
<td>100-flip</td>
<td>14 x 14</td>
<td>16.3 x 16.3</td>
<td>2.57</td>
</tr>
<tr>
<td>144-flip</td>
<td>20 x 20</td>
<td>10 x 11</td>
<td>4.00</td>
</tr>
<tr>
<td>174-flip</td>
<td>24 x 24</td>
<td>10 x 11</td>
<td>5.00</td>
</tr>
<tr>
<td>203-flip</td>
<td>28 x 28</td>
<td>10 x 11</td>
<td>6.00</td>
</tr>
</tbody>
</table>

**ChipArray BGA**

**Square Package Options:**
- 8 to 288 ball counts
- 5 mm to 19 mm body sizes available
- 0.5, 0.75, 0.80 & 1.0 mm ball pitch available

**Low inductance (modeled data):**
- 1.4 nH (1.0 mm trace length)
- 4.1 nH (5.0 mm trace length)
4. Packages for RF
Exposed pad

Features and Benefits:
• Low Profile (1.2 mm max mounted height)
• Low Loop Inductance
• Excellent Thermal Performance

4. Packages for RF
Unleaded packages

These packages use perimeter lands on the bottom of the package to provide electrical contact to the PCB. The package also offers ExposedPad technology.
4. Packages for RF

Unleaded packages

These packages use perimeter lands on the bottom of the package to provide electrical contact to the PCB. The package also offers ExposedPad technology.

Features:
- Larger die size in the same footprint
  - SOIC 8Ld up to 118% increase in die area
  - TQFP 64 10x10 100% increase in die area
  - SOT 6 lead - approximately 168% increase in die area
- Major thermal and electrical improvements
  - Shorter wires and 8 mil thick leadframes = lower inductance and resistance
- No leads (No bent leads!)

Benefits of Flip Chip:
- Reduced signal inductance - because the interconnect is MUCH shorter in length (0.1 mm vs 1-5 mm).
- Reduced power/ground inductance - by using flip chip interconnect, power can be brought directly into the core of the die, rather than having to be routed to the edges.
- Higher signal density - the entire surface of the die can be used for interconnect, rather than just the edges. It can support vastly larger numbers of interconnects on the same die size.
- Die shrink - for pad limited die, the size of the die can be reduced, saving silicon cost.
- Reduced package footprint – this can be achieved by reducing the die to package edge requirements, since you no longer have to leave space for wires.

<table>
<thead>
<tr>
<th>Pin</th>
<th>Body Size (mm)</th>
<th>LO</th>
<th>0.1G</th>
<th>0.2G</th>
<th>0.3G</th>
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</table>
4. Packages for RF

System in package (SiP)

SiP may contain one or more IC chips (wirebonded or flip chip) plus other components such as:
- Discrete passive
- Integrated passive networks
- Passives embedded or patterned in the substrate
- SAW filters
- Decoupling capacitors
- Memories
- Pre-packaged ICs
- Antennas
- Mechanical parts

Additional Benefits of a System in Package Approach:
- Compatibility with die design changes and integration of various die technologies (e.g., Si, GaAs, SiGe, SOI, MEMs and Optical)
- Smaller size solution than individually-packaged ICs
- Enhanced electrical performance by moving critical ICs closer together within the package and reduces parasitics
- Eliminate packaging (multiple ICs now in one package)
  - Reduces system board complexity and layer count
  - Uses less system board space than individually packaged ICs
- Reduced time to market:
  - Changes can be made to the SiP without costly changes to the system board
  - Design flexibility and easy redesign versus complex System on Chip design
Contents:

1. SoC vs SiP
2. SSN
   - Concept
   - Design techniques for SSN reduction
3. Substrate noise
   - Concept
   - Isolation techniques
   - Prediction
4. Packages for RF
5. Pads for RF

5. Pads for RF
Conventional analog pad

- Substrate biased with analog GND
- Series resistor for overcurrent and ESD protection
- Conventional square pad
5. Pads for RF

- Independent substrate biasing
- Octagonal shape to avoid 90° antenna effects
- Guard ring enclosing the pad
- Buried layer beneath the pad
- Protection diodes