Low Noise Amplifiers

High Performance Integrated Circuits Design Group
http://pmos.upc.es/blues/

RF Communications System-on-Chip
http://www.eel.upc.edu/rfcs/

International Master Course 2008-2009

Departamento de Ingeniería Electrónica
Universitat Politècnica de Catalunya

Contents:

1. Low Noise Amplifier (LNA) figures of merit
2. Basic LNA topologies
3. Source degenerated LNA
   3.1 Input matching
   3.2 Current gain
   3.3 Noise Figure
   3.4 Design procedures
4. LNA implementations
   4.1 Single ended topologies
   4.2 Differential topologies
1. Low Noise Amplifier in a receiver

**RF ARCHITECTURES**

- Heterodyne
- Homodyne

1. Low Noise Amplifier figures of merit

- Reduced noise figure, NF
- Moderated gain
- Good input, output impedance matching
- Low power consumption
- Isolation between input and output
- Acceptable linearity (low distortion)
- Stability
1. Low Noise Amplifier figures of merit

Examples (i)

<table>
<thead>
<tr>
<th>Author [Ref.]</th>
<th>NF (dB)</th>
<th>Gain (dB)</th>
<th>IP3/-1dB* (dBm)</th>
<th>Power (mW)</th>
<th>f0 (GHz)</th>
<th>Architecture</th>
<th>Technology</th>
<th>Year</th>
</tr>
</thead>
<tbody>
<tr>
<td>Chang et al. [8]</td>
<td>6.0*</td>
<td>14</td>
<td>na / na</td>
<td>7</td>
<td>0.75</td>
<td>R-Term.</td>
<td>2µm CMOS</td>
<td>1993</td>
</tr>
<tr>
<td>Karaniconicas et al. [5]</td>
<td>2.2</td>
<td>15.6</td>
<td>12.4 / na</td>
<td>20</td>
<td>0.9</td>
<td>L-Degen.</td>
<td>0.5µm CMOS</td>
<td>1996</td>
</tr>
<tr>
<td>Sheng et al. [7]</td>
<td>7.5</td>
<td>11.0</td>
<td>na / na</td>
<td>36</td>
<td>0.9</td>
<td>Shunt-Ser. FB</td>
<td>1µm CMOS</td>
<td>1996</td>
</tr>
<tr>
<td>Refougaran et al. [6]</td>
<td>3.5</td>
<td>22</td>
<td>na / na</td>
<td>27</td>
<td>0.9</td>
<td>1/8m-Term.</td>
<td>1µm CMOS</td>
<td>1996</td>
</tr>
<tr>
<td>Benton et al. [9]</td>
<td>2.7</td>
<td>28</td>
<td>na / 8.5</td>
<td>208</td>
<td>1.6</td>
<td>Shunt-Ser. FB</td>
<td>GaAs FET</td>
<td>1992</td>
</tr>
<tr>
<td>Cioffi [10]</td>
<td>2.2</td>
<td>17.4</td>
<td>na / na</td>
<td>10</td>
<td>1.6</td>
<td>L-Degen.</td>
<td>1µm GaAs FET</td>
<td>1992</td>
</tr>
<tr>
<td>2.2</td>
<td>19.6</td>
<td>6 / -3</td>
<td>10</td>
<td>1.0</td>
<td>L-Degen.</td>
<td>1µm GaAs FET</td>
<td>1992</td>
<td></td>
</tr>
<tr>
<td>Nakatsugawa et al. [11]</td>
<td>2.0</td>
<td>12.2</td>
<td>5.1 / na</td>
<td>2</td>
<td>1.9</td>
<td>L-Degen.</td>
<td>0.5µm GaAs FET</td>
<td>1993</td>
</tr>
<tr>
<td>Heaney et al. [12]</td>
<td>1.5</td>
<td>14.5</td>
<td>11.2 / -1.1</td>
<td>12</td>
<td>1.9</td>
<td>L-Degen.</td>
<td>0.5µm GaAs FET</td>
<td>1993</td>
</tr>
<tr>
<td>Imai et al. [13]</td>
<td>2.5</td>
<td>11.5</td>
<td>9 / na</td>
<td>14</td>
<td>1.6</td>
<td>L-Degen.</td>
<td>0.3µm GaAs FET</td>
<td>1994</td>
</tr>
<tr>
<td>Sheng et al. [14]</td>
<td>5.7</td>
<td>7.8</td>
<td>23.9 / 11</td>
<td>115</td>
<td>1.0</td>
<td>Shunt-Ser. FB</td>
<td>GaAs HBT</td>
<td>1991</td>
</tr>
<tr>
<td>Meyer et al. [15]</td>
<td>2.2</td>
<td>16</td>
<td>6 / -4</td>
<td>40</td>
<td>0.9</td>
<td>L-Degen.</td>
<td>QUBIC BICMOS</td>
<td>1994</td>
</tr>
<tr>
<td>Kobayashi et al. [16]</td>
<td>2.9</td>
<td>17.5</td>
<td>na / na</td>
<td>480</td>
<td>1.0</td>
<td>1/8m-Term. &amp;</td>
<td>GaAs HBT</td>
<td>1994</td>
</tr>
</tbody>
</table>

*IP3 / -1dB compression point are output-referred.
*Neglects contribution of termination resistors. See text for discussion.


1. Low Noise Amplifier figures of merit

Examples (ii)

<table>
<thead>
<tr>
<th>Typical Values [12]</th>
<th>LNA in Fig. 1</th>
<th>LNA in Fig. 5</th>
<th>[13]</th>
<th>[5]</th>
<th>[11]</th>
<th>[11]</th>
</tr>
</thead>
<tbody>
<tr>
<td>NF</td>
<td>2 dB</td>
<td>2.2 dB</td>
<td>2.4 dB</td>
<td>2.5 dB</td>
<td>2.4 dB</td>
<td>2.5 dB</td>
</tr>
<tr>
<td>IP3</td>
<td>-10 dBm</td>
<td>1.3 dBm</td>
<td>-3.4 dBm</td>
<td>2 dBm</td>
<td>2 dBm</td>
<td>-10 dBm</td>
</tr>
<tr>
<td>1-dB Compression</td>
<td>-20 ~ -25 dBm</td>
<td>-18 dBm</td>
<td>-21 dBm</td>
<td>-12 dBm</td>
<td>-12 dBm</td>
<td>-12 dBm</td>
</tr>
<tr>
<td>Power Gain</td>
<td>15 dB</td>
<td>15 dB</td>
<td>20 dB</td>
<td>19.9 dB</td>
<td>19 dB</td>
<td>22 dB</td>
</tr>
<tr>
<td>Input Return Loss</td>
<td>-15 dB</td>
<td>-17 dB</td>
<td>-19 dB</td>
<td>-10 dB</td>
<td>-10 dB</td>
<td>-10 dB</td>
</tr>
<tr>
<td>Output Return Loss</td>
<td>-15 dB</td>
<td>-23 dB</td>
<td>-21 dB</td>
<td>-21 dB</td>
<td>-21 dB</td>
<td>-21 dB</td>
</tr>
<tr>
<td>Reverse Isolation</td>
<td>20 dB</td>
<td>24 dB</td>
<td>35 dB</td>
<td>47.8 dB</td>
<td>47.8 dB</td>
<td>47.8 dB</td>
</tr>
<tr>
<td>Stability Factor</td>
<td>&gt; 1</td>
<td>1.4</td>
<td>3.6</td>
<td>3.6</td>
<td>3.6</td>
<td>3.6</td>
</tr>
<tr>
<td>Frequency</td>
<td>2.4 GHz</td>
<td>2.4 GHz</td>
<td>2.4 GHz</td>
<td>2.4 GHz</td>
<td>2.4 GHz</td>
<td>2.4 GHz</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>4.8 mW</td>
<td>7.2 mW</td>
<td>14.7 mW</td>
<td>12 mW</td>
<td>12 mW</td>
<td>12 mW</td>
</tr>
<tr>
<td>Process</td>
<td>0.25 µm</td>
<td>0.25 µm</td>
<td>0.35 µm</td>
<td>0.5 µm</td>
<td>0.35 µm</td>
<td>0.35 µm</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>3.3 V</td>
<td>3.3 V</td>
<td>2 V</td>
<td>3 V</td>
<td>1.5 V</td>
<td>1.5 V</td>
</tr>
</tbody>
</table>

1. Low Noise Amplifier figures of merit

Examples (iii)

<table>
<thead>
<tr>
<th>$f_0$ 2.45 GHz</th>
<th>CMOS LNA</th>
<th>SiGe LNA</th>
</tr>
</thead>
<tbody>
<tr>
<td>50-ohm NF</td>
<td>2.88 dB</td>
<td>2.86 dB</td>
</tr>
<tr>
<td>Bias Current</td>
<td>8.1 mA</td>
<td>7.0 mA</td>
</tr>
<tr>
<td>Transducer Gain</td>
<td>15.1 dB</td>
<td>15.9 dB</td>
</tr>
<tr>
<td>$S_{11}$</td>
<td>-14.2 dB</td>
<td>-12.7 dB</td>
</tr>
<tr>
<td>$S_{22}$</td>
<td>-20.2 dB</td>
<td>-16.0 dB</td>
</tr>
<tr>
<td>$S_{12}$</td>
<td>&lt; -34</td>
<td>&lt; -30</td>
</tr>
<tr>
<td>IIIP$_1$</td>
<td>2.2 dBm</td>
<td>-2.6 dBm</td>
</tr>
<tr>
<td>IP$_{1dB}$</td>
<td>-7.0 dBm</td>
<td>-11.2 dBm</td>
</tr>
</tbody>
</table>


Contents:

1. Low Noise Amplifier (LNA) figures of merit
2. Basic LNA topologies
3. Source degenerated LNA
   3.1 Input matching
   3.2 Current gain
   3.3 Noise Figure
   3.4 Design procedures
4. LNA implementations
   4.1 Single ended topologies
   4.2 Differential topologies
2. Basic topologies
2.1 Shunt input termination

- Input matching: $R_1 = R_s$
- Effective gate voltage: $0.5 v_{IN}$
- Shunt resistor adds noise to the input
- Noise Factor: $F \geq 2 + \frac{4 \gamma}{\alpha} \cdot \frac{1}{g_m R_s}$

- For comparison, assume no input matching ($R_1 = \infty$): $F = 1 + \frac{\gamma}{\alpha} \cdot \frac{1}{g_m R_s}$
- Input matching adds more than 6 dB to the Noise Figure
- Noise Figure degrades at high frequencies and when gate current noise is taken into account

Homework
2.1 Shunt input termination

- Demonstrate this expression for the Noise Factor:
  
  $F \geq 2 + \frac{4 \gamma}{\alpha} \cdot \frac{1}{g_m R_s}$

- Account only for the thermal noise sources associated to $R_s$, $R_1$ and channel
2. Basic topologies

2.2 Shunt-series feedback amplifier

- Input matching: $R_{in} = R_s$
- It is actually a broad band amplifier, not a resonant LNA
- Shunt resistor adds noise to the input
- Noise Figure results larger than $F_{min}$ (a few dB)
- Power consumption is much higher compared with other amplifiers with the same Noise Figure.
- Requires on-chip resistors of high-quality: not appropriate for CMOS integration

- Noise Figure degrades at high frequencies and when gate current noise is taken into account

2.3 Common gate amplifier

- Input matching: $Z_{in} \equiv \frac{1}{g_m} \equiv R_s$
- No matching resistors $\Rightarrow$ no added noise, but...
- Transistor channel is in the input signal path: channel noise source limits noise performance.
- Noise Figure:
  $$F \geq 1 + \frac{\gamma}{\alpha}$$

- The minimum possible noise figure is limited to 2.2 dB in long channel regime and 4.8 dB in short channel regime (1.76 dB for Bipolar common-base LNAs)
- Noise Figure degrades at high frequencies and when gate current noise is taken into account
Homework
2.3 Common gate amplifier

1.- Demonstrate the following expression for the Gain:

\[ A_V \equiv g_m \left( \frac{r_{ds}}{R_L} \right) \]

assume \( r_{ds} \gg \frac{1}{g_m}, R_L \gg R_S \)

2.- Demonstrate the following expression for the Input impedance

\[ Z_{in} \equiv \frac{1 + \frac{R_L}{r_{ds}}}{g_m} \approx \frac{1}{g_m} \]

assume \( r_{ds} \gg \frac{1}{g_m}, r_{ds} \gg R_L \)

3.- Demonstrate the following expression for the Noise Factor

\[ F \equiv 1 + \frac{\gamma}{\alpha} \left( \frac{1}{r_{ds}} + \frac{1}{R_L} \right)^2 \geq 1 + \frac{\gamma}{\alpha} \]

\[ \alpha \left( \frac{1}{r_{ds}} + \frac{2}{R_L} \right) \]

• Account only for the thermal noise sources associated to \( R_s \) and channel
• Assume \( r_{ds} \gg \frac{1}{g_m}, R_L \gg \frac{1}{g_m}, R_S = \frac{1}{g_m} \)

2. Basic topologies
2.4 Source degenerated common source amplifier

• Input matching: obtained through inductive source degeneration (only around some frequencies: narrow band LNA)

• No resistive elements in the signal path

• Noise Figure: best noise performance of any previous architecture
3. Source degenerated LNA

3.1 Input impedance

\[ Z_{in}(j\omega) = \frac{1}{j\omega C_{gs}} + \left( \frac{\omega_T}{j\omega} + 1 \right) Z \]

If the degenerated source impedance is inductive:

\[ Z = j\omega L_s \quad \Rightarrow \quad Z_{in}(j\omega) = \frac{1}{j\omega C_{gs}} + L_s \omega_T + j\omega L_s \]

Real term without resistive element!
3. Source degenerated LNA

3.1 Input impedance

\[ Z_{in}(j\omega) = \frac{1}{j\omega C_{gs}} + L_s \omega_T + j\omega L_s \]

Is real when the two imaginary terms resonate

Resonance frequency and input impedance are determined by the same component: \( L_s \)

SOLUTION:

\[ Z_{in}(j\omega) = \frac{1}{j\omega C_{gs}} + L_s \omega_T + j\omega (L_s + L_g) \]

Resonance frequency:

\[ \omega_o = \frac{1}{\sqrt{C_{gs} (L_g + L_s)}} \]

Input impedance at resonance:

\[ Z_{in}(j\omega_o) = L_s \omega_T \]

3.2 Current gain

Input voltage to output current gain at resonance:

\[ |G_m(j\omega_o)| = g_m Q_{in} = \frac{g_m}{\omega_o C_{gs} (R_s + L_s \omega_T)} = \frac{\omega_T}{2 \omega_o R_s} \]

This expression is independent on MOS small signal transconductance!

How to choose the MOS size?

Noise Figure optimization
3. Source degenerated LNA
3.3 LNA Noise figure

Noise factor considering only gate inductor losses and channel thermal noise:

1.- Noise from the generator:

\[
i_o = g_m v_{gs} = g_m \frac{i_{in}}{sC_{gs}} = g_m \frac{1}{sC_{gs}} \frac{\sqrt{v_s^2}}{R_s + R_{Lg} + Z_{in}} = g_m \frac{1}{sC_{gs}} \frac{\sqrt{v_s^2}}{2R_s + R_{Lg}}
\]

\[
v_{out1} = Z_L i_o^2 = Z_L^2 \frac{g_m^2}{\omega_0^2 C_{gs}^2} \left( \sqrt{v_{R_{Lg}}^2} \right)^2
\]

2.- Noise from the \( R_{Lg} \):

\[
i_o = g_m v_{gs} = g_m \frac{i_{in}}{sC_{gs}} = g_m \frac{1}{sC_{gs}} \frac{\sqrt{v_{R_{Lg}}^2}}{R_s + R_{Lg} + Z_{in}} = g_m \frac{1}{sC_{gs}} \frac{\sqrt{v_{R_{Lg}}^2}}{2R_s + R_{Lg}}
\]

\[
v_{out2} = Z_L i_o^2 = Z_L^2 \frac{g_m^2}{\omega_0^2 C_{gs}^2} \left( \sqrt{v_{R_{Lg}}^2} \right)^2
\]
3. Source degenerated LNA
3.3 LNA Noise figure

Noise factor considering only gate inductor losses and channel thermal noise:

\[
\begin{align*}
3.- & \text{ Noise from the channel} \\
\bar{i}_o &= g_m v_{gs} + \sqrt{\bar{i}_n^2} = g_m \frac{i_{in}}{sC_{gs}} + \sqrt{\bar{i}_n^2} = \frac{g_m}{sC_{gs}} \left( \frac{-i_o}{sL_s} + \frac{sL_s}{sC_{gs} + R_{Lg} + R_s + sL_s} \right) + \sqrt{\bar{i}_n^2}
\end{align*}
\]

At resonance:

\[
\begin{align*}
\bar{i}_o &= \frac{g_m}{j\omega o C_{gs}} \left( \frac{-j\omega o L_s i_o}{R_{Lg} + R_s} \right) + \sqrt{\bar{i}_n^2} = \bar{i}_n \left( \frac{-g_m}{C_{gs} R_{Lg} + R_s} \right) + \sqrt{\bar{i}_n^2}
\end{align*}
\]
3. Source degenerated LNA

3.3 LNA Noise figure

Noise factor considering only gate inductor losses and channel thermal noise:

\[
\begin{align*}
F &= 1 + \frac{R_{Lg}}{R_s} + \frac{\gamma}{\alpha} g_m R_s \left( \frac{\omega_o}{\omega_T} \right)^2 \\
\gamma &\sim 2 \text{ (short channel)} \\
\alpha &\sim 0.85 \\
R_s &= 50 \Omega \\
g_m &\sim 1/50 \\
\omega_T/\omega_o &= 5 \text{ to } 20
\end{align*}
\]

\[
F = 1 + \frac{R_{Lg}}{R_s} + 0.094 \\
to \\
F = 1 + \frac{R_{Lg}}{R_s} + 0.0059
\]
3. Source degenerated LNA

3.3 LNA Noise figure

Gate resistance should be reduced by design:

\[ R_g = \frac{R \cdot W}{3n^2L} \]

This resistance is inversely proportional to the square of the number of gate fingers \( n \). If \( n \) is chosen large enough, it is common to ignore the effects and noise introduced by gate resistance.

\[ R_{GAMS0.35} = 8 \, \Omega \]

\[ W = 300 \, \text{um} \]

\[ L = 0.35 \, \text{um} \]

\[ R_g = 6.77 \, \Omega \]

Gate fingers (15 in the figure)

Neglecting gate resistance and noise due to losses in the inductors:

\[ F = 1 + \frac{G_u + \left[ (G_s + G_u)^2 + (B_u + B_s)^2 \right] R_n}{G_s} \]

\[ G_{s_{\text{opt}}} = \sqrt{\frac{G_u}{R_n} + G_C^2} = \frac{\alpha \omega C_{gs} \left( \frac{\delta}{\sqrt{5\gamma(1-|c|^2)}} \right)}{R_s} = \frac{1}{R_s} \]

The width of the MOS transistor can be set to find the \( C_{gs} \) that lead to \( G_{s_{\text{opt}}} = 1/R_s \)

Example:

\[ f = 1.57542 \, \text{GHz}, \quad R_s = 50 \, \Omega, \quad \gamma=2, \quad \delta=4, \quad |c| = 0.395, \quad \alpha = 0.85 \]

\[ C_{gs} = \frac{G_{s_{\text{opt}}}}{\alpha \omega \sqrt{\frac{\delta}{5\gamma(1-|c|^2)}}} \approx 2G_{s_{\text{opt}}} \frac{\omega}{\omega} \approx 4 \, \text{pF} \]

\[ W \approx 4 \, \text{mm}, \quad I_{\text{bias}} = 100 \, \text{mA} \]

Noise Figure - Power Trade-off
3. Source degenerated LNA
3.3 LNA Noise figure

We need an expression of $F$ that includes power!!!

\[
F = 1 + \frac{G_u + \left( (G_c + G_s)^2 + (B_c + B_s)^2 \right) R_n}{G_s} = F_{\text{min}} + \frac{R_n}{G_s} \left[ (G_s - G_{s\text{, opt}})^2 + (B_s - B_{s\text{, opt}})^2 \right]
\]

• Let’s assume $B_s = B_{s\text{, opt}}$ (just to simplify the analysis…)

\[
\Rightarrow \quad F \approx F_{\text{min}} + \frac{R_n}{G_s} \left( G_s - G_{s\text{, opt}} \right)^2
\]

• We define a parameter called quality factor, $Q \equiv \frac{G_s}{\omega C_{gs}}$

• Applied to the optimum $G_s$: $Q_{\text{opt}} = \frac{G_{s\text{, opt}}}{\omega C_{gs}} = \alpha \sqrt{\frac{\delta}{5\gamma}} \left( 1 - |c|^2 \right)$

• Applied to a non-optimum $G_s$: $Q_s = \frac{G_s}{\omega C_{gs}} = \frac{1}{\omega C_{gs} R_s}$

\[
F = F_{\text{min}} + \left[ \frac{\gamma}{\alpha g_m R_s} \right] \left[ 1 - \frac{Q_{\text{opt}}}{Q_s} \right]^2
\]
**MOS transistor**

Large signal model with second order and short channel effects

Carrier velocity saturation due to lateral field:

\[ \text{vel} \neq \mu E, \quad \text{vel} = \text{vel}_{\text{sat}} < \mu E, \quad \text{vel}_{\text{sat}} = \mu E_{\text{sat}} \]

\[
I_D = \frac{\mu_n C_{\text{ox}}}{2} \left( \frac{W}{L} \right) (V_{gs} - V_t) V_{ds,\text{sat}} = \frac{K}{2} (V_{gs} - V_t)(V_{gs} - V_t) \parallel E_{\text{sat}}
\]

\[ I_D = \frac{K}{2} (V_{gs} - V_t) \left( \frac{(V_{gs} - V_t) L E_{\text{sat}}}{(V_{gs} - V_t) + L E_{\text{sat}}} \right) \]

If \( LE_{\text{sat}} \gg (V_{gs} - V_t) \), then we are in long channel regime: \( I_D = \frac{K'}{2} \left( \frac{W}{L} \right) (V_{gs} - V_t)^2 \)

If \( LE_{\text{sat}} \ll (V_{gs} - V_t) \), then we are in short channel regime: \( I_D = \frac{K'}{2} W (V_{gs} - V_t) E_{\text{sat}} \)

---

**MOS transistor**

Small signal model: transconductance

In deep short channel regime:

\[
g_m = \frac{\partial I_D}{\partial V_{gs}} = \frac{\mu_n C_{\text{ox}}}{2} W E_{\text{sat}} \quad \text{It is constant!}
\]

In short channel regime:

\[
g_m = \left[ \frac{1 + \rho/2}{(1 + \rho)^2} \right] \mu_n C_{\text{ox}} \frac{W}{L} (V_{gs} - V_t)
\]

\[ \rho = \frac{V_{gs} - V_t}{L E_{\text{sat}}} \]

(These equations do not include mobility degradation due to normal field)
3. Source degenerated LNA

3.3 LNA Noise figure

We need an expression of $F$ that includes power!!!

$$ F \approx F_{\text{min}} + \frac{R_n}{G_s} (G_s - G_{\text{opt}})^2 $$

$$ F = F_{\text{min}} + \left[ \frac{\gamma}{\alpha s m R_s} \right] \left[ 1 - \frac{Q_{\text{opt}}}{Q_s} \right]^2 $$

- The parameters $\alpha$, $s_m$, $Q_s$, $Q_{\text{opt}}$ depend on power consumption. They can be expressed in function of $P_D$ and $\rho$

$$ P_D = V_{DD}I_D = V_{DD}WLC_{ax}V_{sat}E_{sat} \frac{\rho^2}{1 + \rho} \quad \rho = \frac{V_{gs} - V_t}{L E_{sat}} $$

Low Noise Amplifiers
3. Source degenerated LNA

3.3 LNA Noise figure

But a closed-form solution is possible if \( \rho << 1 \)

\[
\rho^2 = \frac{P_D}{P_0} \sqrt{\frac{\delta}{5\gamma} \left(1 - |c|^2\right)} \left[1 + \sqrt{\frac{7}{4}}\right] \Rightarrow Q_{sp} = |c| \sqrt{\frac{5\gamma}{\delta} \left[1 + \sqrt{1 + \frac{3}{5|c|^2} \left(1 + \frac{\delta}{5\gamma}\right)}\right]} = \frac{1}{\omega C_{gs} R_s}
\]

\[
F_{\text{min}P} \approx 1 + 2.4 \frac{\gamma}{\alpha} \left[\frac{\omega_o}{\omega_T}\right]
\]

\[
W_{\text{opt}P} = \frac{3}{2} \frac{1}{\omega_o L C_{ox} R_s Q_{sp}}
\]

A typical value for \( Q_{sp} \) is 4.5

\( f \) is little sensitive to variations of \( Q_{sp} \) around this value

---

From the \( F_{\text{min}} \) expression:

\[
F_{\text{min}} = 1 + 2R_n \left(G_{opt} + G_c\right) = 1 + \frac{2}{\sqrt{5}} \frac{\omega_o}{\omega_T} \sqrt{\gamma \delta \left(1 - |c|^2\right)}
\]

\( \gamma = 2, \delta = 4, |c| = 0.395, \alpha = 0.85 \)

\[
F_{\text{min}} \approx 1 + 2.3 \left[\frac{\omega_o}{\omega_T}\right]
\]
3. Source degenerated LNA

3.3 LNA Noise figure

With $W_{opt}$ the noise figure yields:

$$F_{\text{min}P} \approx 1 + 2.4 \frac{\gamma}{\alpha} \left[ \frac{\omega_o}{\omega_T} \right]$$

Whereas the absolute minimum noise figure is:

$$F_{\text{min}} \approx 1 + 2.3 \left[ \frac{\omega_o}{\omega_T} \right]$$

Comparison:

<table>
<thead>
<tr>
<th>$\omega_T/\omega$</th>
<th>$F_{\text{min}}$ (dB)</th>
<th>$F_{\text{min}P}$ (dB)</th>
</tr>
</thead>
<tbody>
<tr>
<td>20</td>
<td>0.5</td>
<td>1.1</td>
</tr>
<tr>
<td>15</td>
<td>0.6</td>
<td>1.4</td>
</tr>
<tr>
<td>10</td>
<td>0.9</td>
<td>1.9</td>
</tr>
<tr>
<td>5</td>
<td>1.6</td>
<td>3.3</td>
</tr>
</tbody>
</table>


Considerations about input matching and noise figure:

Minimum noise figure is achieved with:

$$B_{s_{\text{opt}}} = \omega_o C_{gs} \left( 1 + \alpha \left| c \right| \sqrt{\frac{\delta}{5\gamma}} \right)$$

This is implemented with a series inductance composed by the gate inductor and the input equivalent source degenerated inductor, that for moderate values of $Q$ preserves the value of the inductor

$$B_s = \frac{1}{\omega_o (L_g + L_s)} = \omega_o C_{gs}$$

For usual parameter values $B_{s_{\text{opt}}} = 1.25 \omega_o C_{gs}$ and $B_s$ is a 15% lower than required.
3. Source degenerated LNA

3.4 Design procedure

**Power optimization based design procedure:**

1. Find the optimum device width:
   \[ W_{\text{opt}} = \frac{3}{2} \frac{1}{\omega_o LC_{\text{ox}} R_s Q_{SP}} \]

2. Calculate \( V_{\text{od}} = V_{gs_{\text{bias}}} - V_T \) to bias the device with the constrained \( I_{D_{\text{bias}}} \)

3. Select the desired \( L_s \) to match the generator impedance with the \( \omega_T \) corresponding to the bias point
   \[
   Z_{\text{in}}(j\omega) = \frac{1}{j\omega C_{gs}} + L_s\omega_T + j\omega(L_s + L_g)
   \]

4. The expected noise figure can be computed with:
   \[
   F_{\text{minP}} = 1 + 2.4 \frac{\gamma}{\alpha} \left[ \frac{\omega_o}{\omega_T} \right]
   \]

5. Add sufficient series inductance \( L_g \) to resonate the input loop at the desired operating frequency

**Possible problem:** *inductor values too low to be easily integrated!!*

---

**Inductor and power constrained design procedure:**

1. Select \( L_s \) as the lower inductor value in the inductors library of the technology or realizable (1 - 3 nH)

2. Find the transistor unity gain frequency \( \omega_T \) with the condition (input matching)

3. Find the parameter \( p = \frac{\delta \alpha^2}{5\gamma} \) and determine the optimal value of \( Q_{SP,L} = \sqrt{1 + \frac{1}{p}} \)

4. Calculate the series inductance \( L_g \) to resonate the input loop at the desired operating frequency
   \[
   Q_s = \frac{1}{\omega_o C_{gs} R_s} \frac{\omega_o(L_s + L_g)}{R_s}
   \]
3. Source degenerated LNA

3.4 Design procedure

Inductor and power constrained design procedure:

5. Find \( C_{gs} = \frac{1}{\omega_0^2 (L_g + L_s)} \) and, using minimum length devices, calculate \( W = \frac{3}{2} \frac{C_{gs}}{LC_{ox}} \)

6. Find the device transconductance \( g_m \)

7. Calculate \( V_{od} = V_{gs\_bias} - V_T \) to bias the device and obtain the necessary \( g_m \)

8. Calculate the bias current for that biasing \( g_m = C_{gs} \omega_T \)

9. The expected noise figure can be computed with:

\[
F_{\text{min},L} \approx 1 + \frac{2\gamma}{\alpha} \left( \frac{\omega_p}{\omega_T} \right) \sqrt{p} \left( \sqrt{|c|} + \sqrt{p} + \sqrt{1+p} \right)
\]
4. LNA implementations

4.1 Single ended topologies

Single ended with biasing, cascode transistor and output matching inductor:

- Cascode transistor helps to increase output gain
- Cascode transistor helps to reduce $S_{21}$, and reduce $C_{gd1}$ Miller effect
- Output Inductor resonates with output load to maximize output power transfer and gain at resonance frequency

NOTE: for input matching, a cascoded stage has

$$\text{Re}\{Z_{\text{in}}\} = \frac{\omega_l L_s}{1 + 2C_{gd1}/C_{gs1}}$$

- DC blocking capacitor modifies slightly effective series capacitance (in the example, it changes $\omega_o$ a 3%)
- The width of the cascoded transistor must be sized to trade-off common source gain reduction and increase of parasitic source capacitance of M2 (both are consequence of a wider M2).

---

4. LNA implementations

4.1 Single ended topologies

Two stage LNA:

---

4. LNA implementations

4.1 Single ended topologies

**Dual band two stage LNA:**


**Figure 8:** LNA circuit layout.

**Figure 6:** Simulated power gain of the LNA.

---

4.2 Differential topologies

- Insensitive to ground inductance value
- Common mode noise rejection (NOTE: don’t mirror inductors!). Large CMRR, PSSR
- More linearity, higher dynamic range.

<table>
<thead>
<tr>
<th>Benefits</th>
<th>Drawbacks</th>
</tr>
</thead>
<tbody>
<tr>
<td>• More power for the same noise figure</td>
<td>• Stacking of devices (I_{BIAS}) problematic for low-voltage</td>
</tr>
<tr>
<td>• Stacking of devices (I_{BIAS}) problematic for low-voltage</td>
<td></td>
</tr>
</tbody>
</table>
4. LNA implementations
4.2 Differential topologies

Page(s): 12 -17
4. LNA implementations
4.2 Differential topologies

Differential topology for low-voltage:

- No tail current source
- Negative Gm cell to compensate inductors low Q

<table>
<thead>
<tr>
<th>Supply voltage</th>
<th>1V</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process</td>
<td>0.35-um CMOS</td>
</tr>
<tr>
<td>RF frequency</td>
<td>2.4 GHz - 2.48 GHz</td>
</tr>
<tr>
<td>IF</td>
<td>10.7 MHz</td>
</tr>
<tr>
<td>LNA Gain</td>
<td>18 dB</td>
</tr>
<tr>
<td>NF</td>
<td>5.7 dB</td>
</tr>
<tr>
<td>IIP3</td>
<td>-10 dBm</td>
</tr>
<tr>
<td>S11</td>
<td>-19 dB</td>
</tr>
<tr>
<td>S12</td>
<td>-48 dB</td>
</tr>
<tr>
<td>Power</td>
<td>8.5 mW</td>
</tr>
</tbody>
</table>


Differential topology with notch filter for low-voltage:

- Notch filter implemented in the second stage
- Negative Gm cells to compensate inductors low Q
- On-chip calibration of L value

4. LNA implementations

4.2 Differential topologies

Differential topology with notch filter for low-voltage:

- Example of effects of low Q inductors:

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Simulation results (Q = 4)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency (GHz)</td>
<td>2.4</td>
</tr>
<tr>
<td>IF (MHz)</td>
<td>200</td>
</tr>
<tr>
<td>Gain (dB)</td>
<td>18</td>
</tr>
<tr>
<td>Maximum IR (dB)</td>
<td>80</td>
</tr>
<tr>
<td>Supply Voltage (V)</td>
<td>1</td>
</tr>
<tr>
<td>Power dissipation (mW)</td>
<td>32</td>
</tr>
<tr>
<td>NF (dB)</td>
<td>4.6</td>
</tr>
<tr>
<td>S11 (dB)</td>
<td>-8</td>
</tr>
<tr>
<td>IIP3 (dBm)</td>
<td>-7</td>
</tr>
<tr>
<td>Area (mm$^2$)</td>
<td>1</td>
</tr>
</tbody>
</table>

Table 1. Simulated performance of LNA with source degeneration image-rejection filter with Q = 4

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Measurement results</th>
<th>Re-simulation results (Q = 1.5)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency (GHz)</td>
<td>2.4</td>
<td>2.4</td>
</tr>
<tr>
<td>IF (MHz)</td>
<td>200</td>
<td>200</td>
</tr>
<tr>
<td>Gain (dB)</td>
<td>-7</td>
<td>-5</td>
</tr>
<tr>
<td>IR (dB)</td>
<td>3</td>
<td>5</td>
</tr>
<tr>
<td>Supply Voltage (V)</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>Power dissipation (mW)</td>
<td>35</td>
<td>32</td>
</tr>
<tr>
<td>NF (dB)</td>
<td>14</td>
<td>12</td>
</tr>
<tr>
<td>S11 (dB)</td>
<td>-12</td>
<td>-11</td>
</tr>
<tr>
<td>IIP3 (dBm)</td>
<td>25.8</td>
<td>21</td>
</tr>
</tbody>
</table>

Table 2. Performance summary from both measurement and simulation with inductor Q of 1.5


4.3 Very high RF LNA

Tri-stage LNA with common gate inductive feedback input stage

4. LNA implementations

4.3 Very high RF LNA

Tri-stage LNA with common gate inductive feedback input stage

0.18 µm CMOS process
First IF of 5 GHz

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Measurement</th>
</tr>
</thead>
<tbody>
<tr>
<td>$S_{11}$</td>
<td>-21dB</td>
</tr>
<tr>
<td>$S_{22}$</td>
<td>-10dB</td>
</tr>
<tr>
<td>Frequency of Maximum Power Gain</td>
<td>21.8GHz</td>
</tr>
<tr>
<td>Maximum Power Gain</td>
<td>27.5dB</td>
</tr>
<tr>
<td>Maximum Voltage Gain</td>
<td>35.7dB</td>
</tr>
<tr>
<td>Maximum Voltage Gain of LNA</td>
<td>22dB</td>
</tr>
<tr>
<td>LNA Noise Figure</td>
<td>6.0dB</td>
</tr>
<tr>
<td>Overall Noise Figure</td>
<td>7.7dB</td>
</tr>
<tr>
<td>LNA Power Consumption</td>
<td>24mW</td>
</tr>
<tr>
<td>Total Power Consumption</td>
<td>64.5mW</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td>1.5V</td>
</tr>
<tr>
<td>Chip Area</td>
<td>$0.8 \times 0.9\text{mm}^2$</td>
</tr>
</tbody>
</table>


Summary

- Source degenerated topology best suited for normal $\omega_T / \omega_o$ ratios (10..5). For smaller ratios and higher frequencies, common gate with inductive feedback can be better.

- Trade-off between Noise-Figure - Power Consumption - Input Matching

- Basic performance limited by the quality factor of passives (inductors):

$$F = 1 + \frac{R_L}{R_s} + \frac{R_T}{R_x} + \frac{\gamma X}{Q_o} \left( \frac{\omega_o}{\omega_T} \right)$$

$$|G_m(j\omega_o)| = g_m Q_{in}$$

$$P_D = \frac{P_0}{Q_o} \frac{\rho^2}{1 + \rho}$$

- Differential topologies alleviate some of the problems of integration (ground inductance dependence and noise couplings) at the expenses of power consumption.